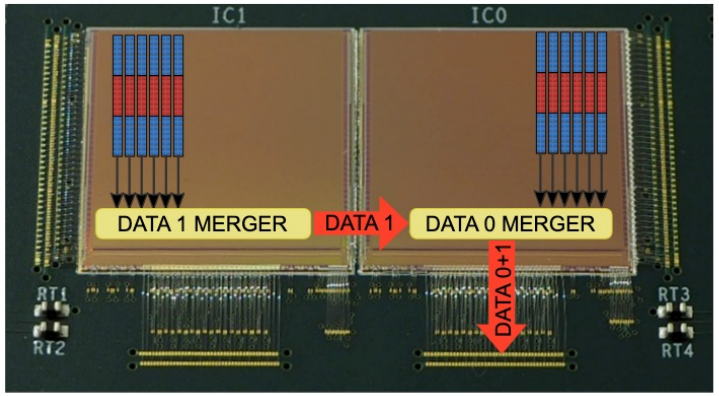
Quad Module – MALTA2 V1

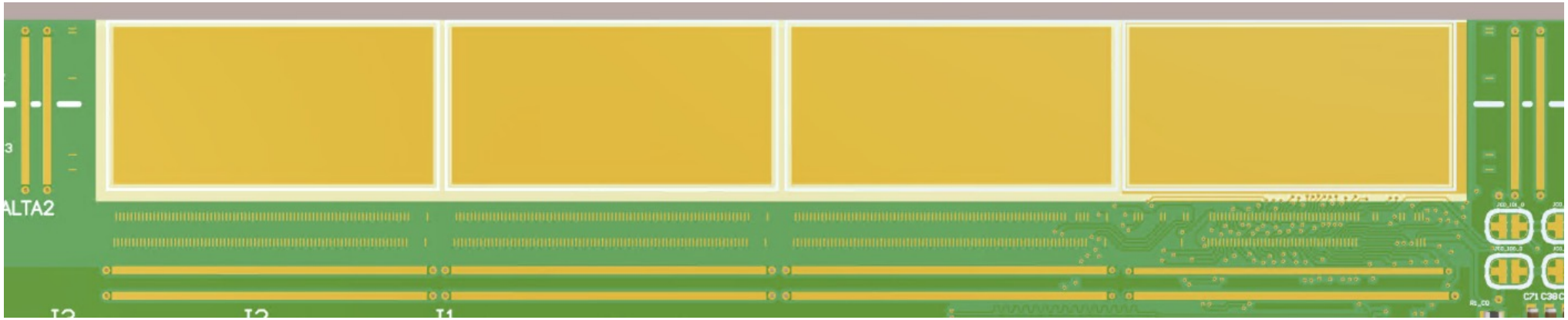
Marcos Vázquez Núñez

Carlos Solans Sánchez

Introduction

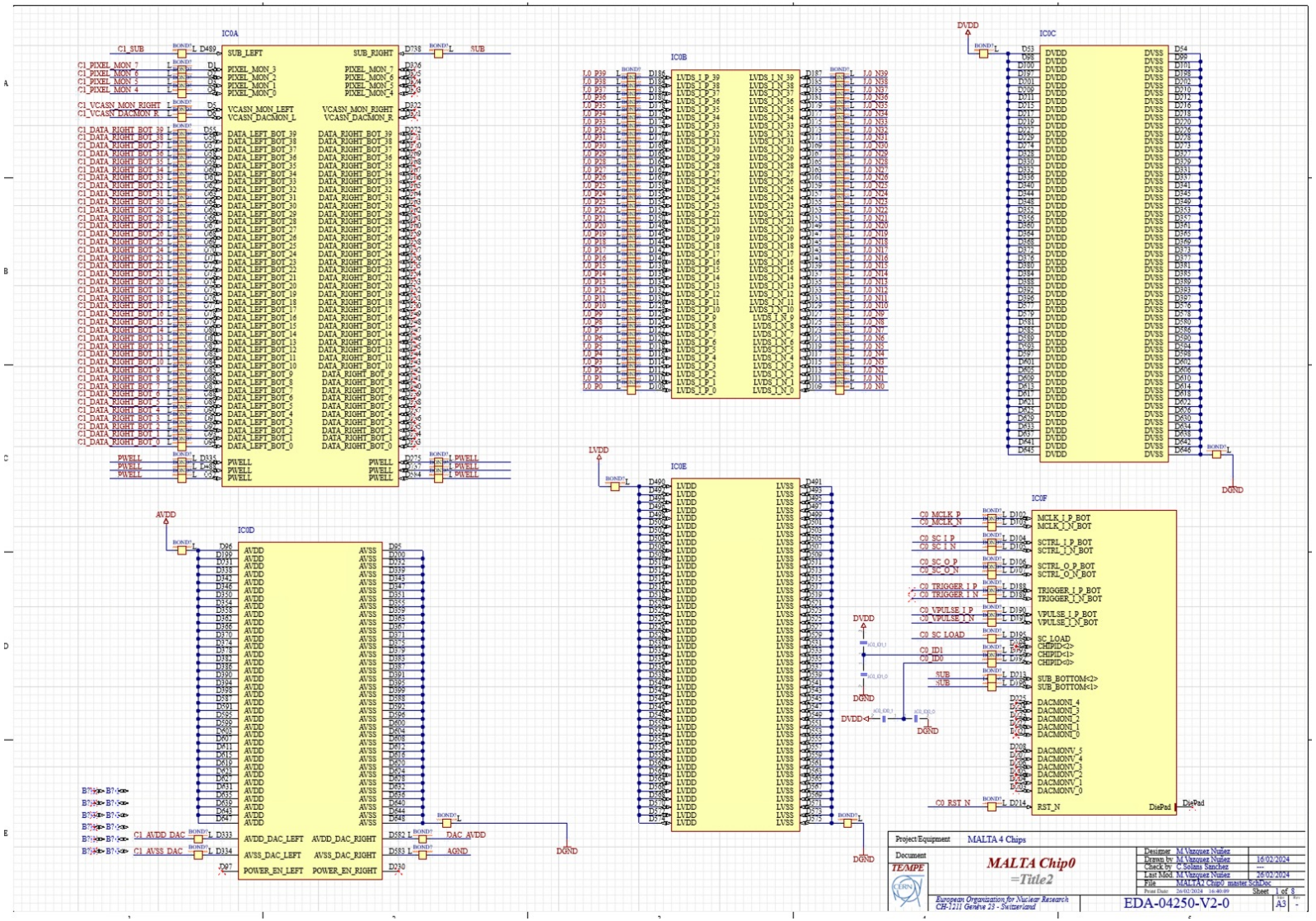


(a) IC0 Master; IC1 Slave

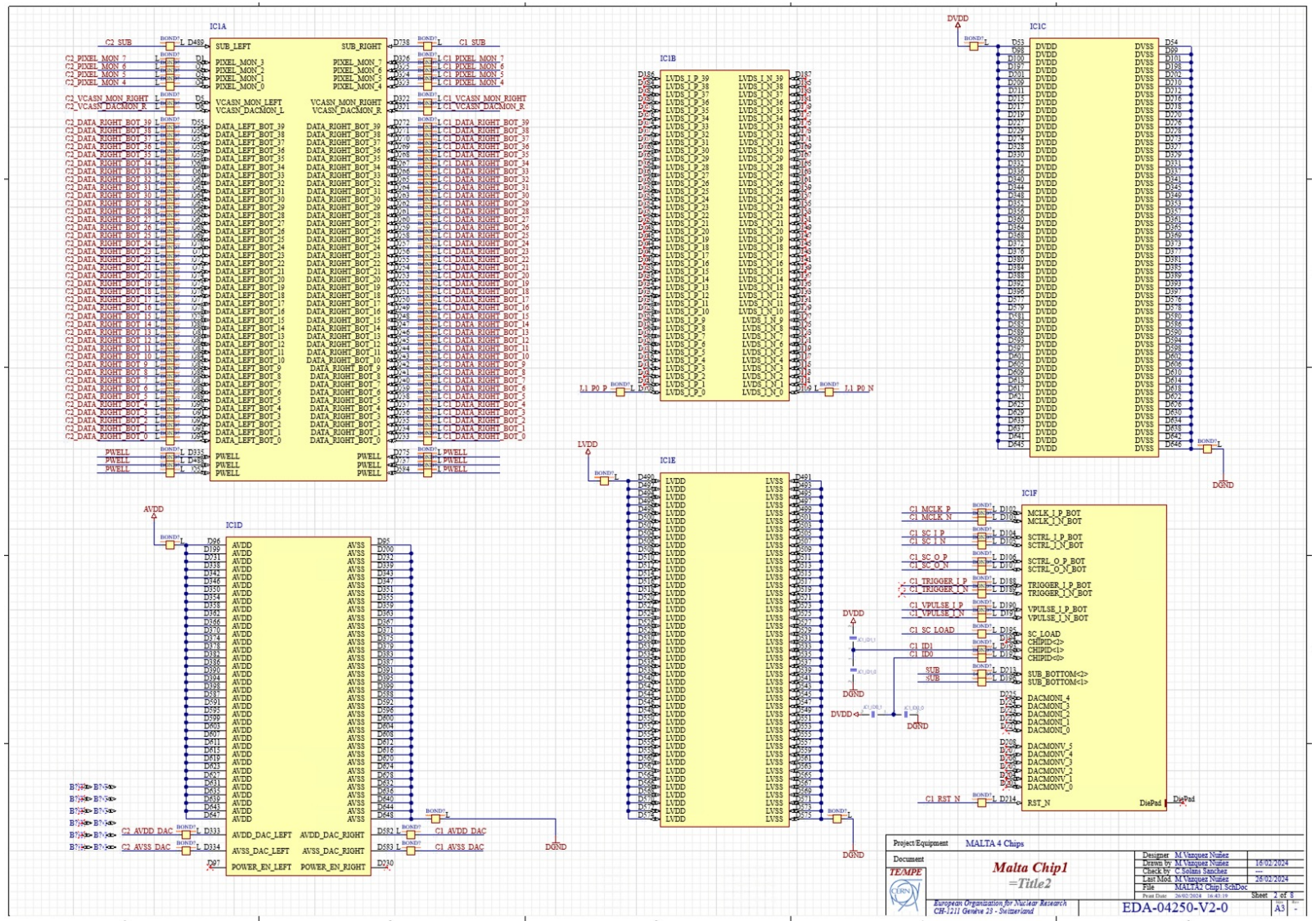


IC3 Master | IC2 Master | IC1 Master | IC0 Master

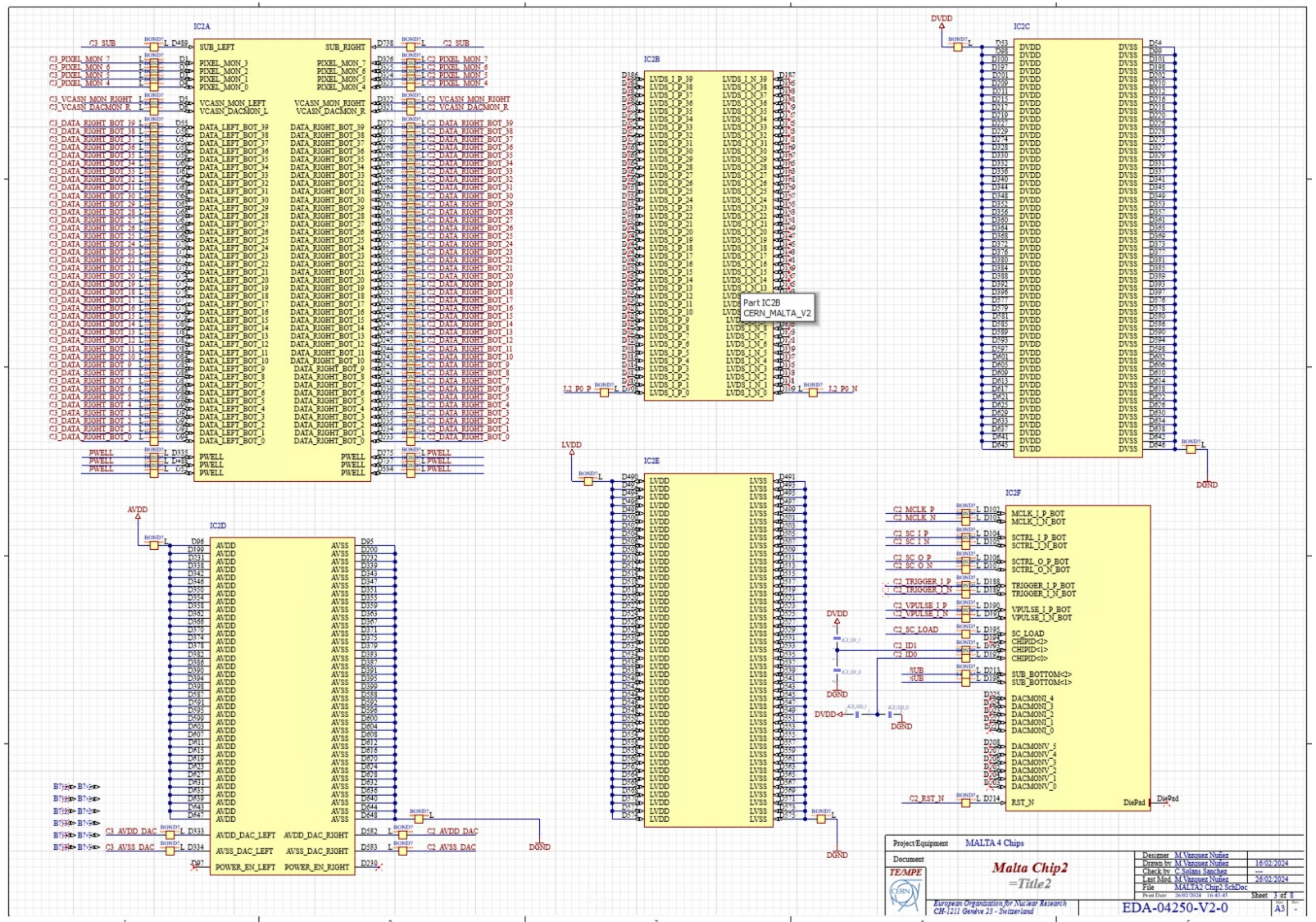
CHIP 0 - MASTER



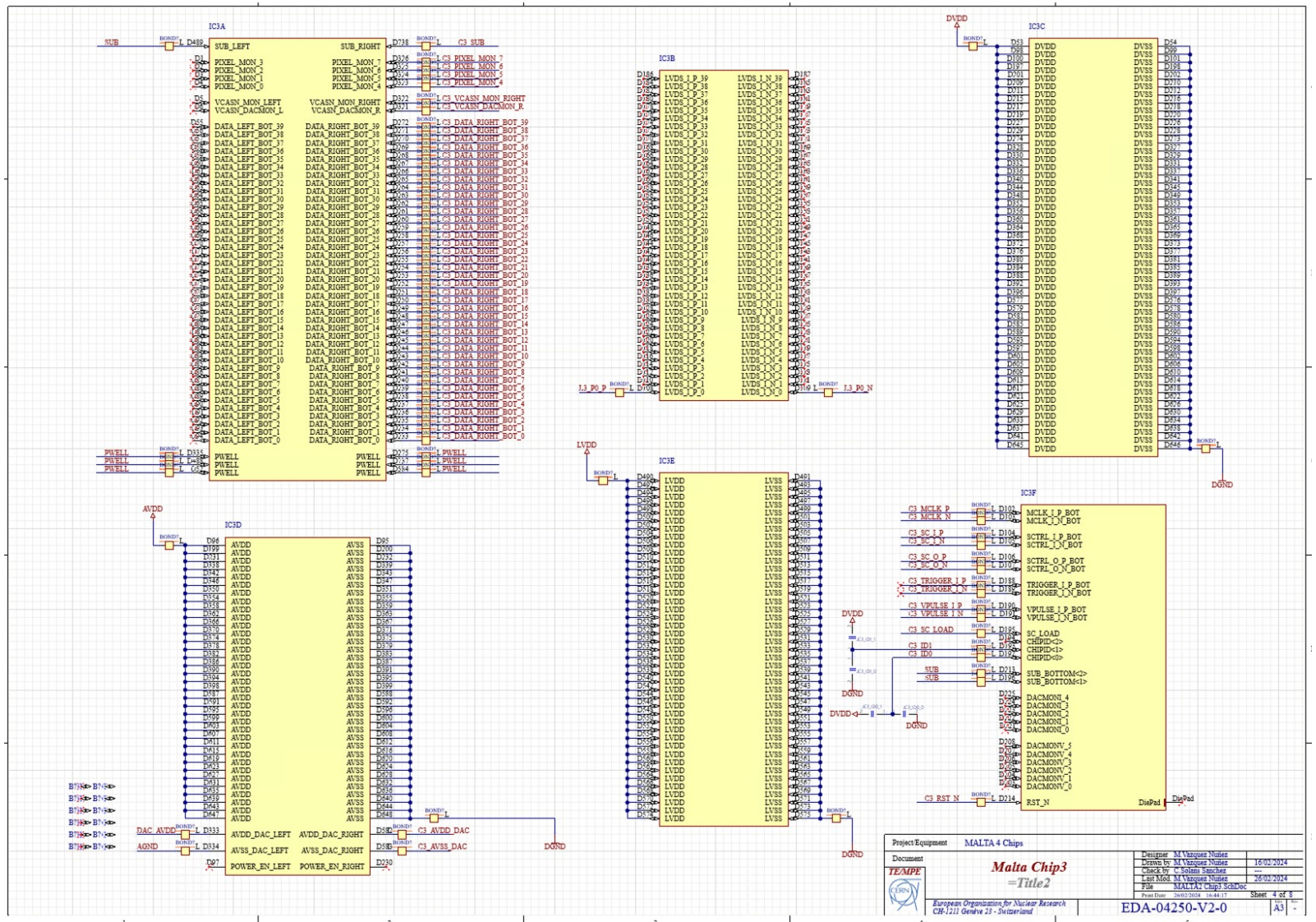
CHIP 1 - Slave


IC1A
IC1B
IC1C
IC1D
IC1E
IC1F
SUB_LEFT
SUB_RIGHT
DVDD
DVSS
AVDD
AVSS
LVDD
LVSS
DGND
Malta Chip1
=Title2
EDA-04250-V2-0

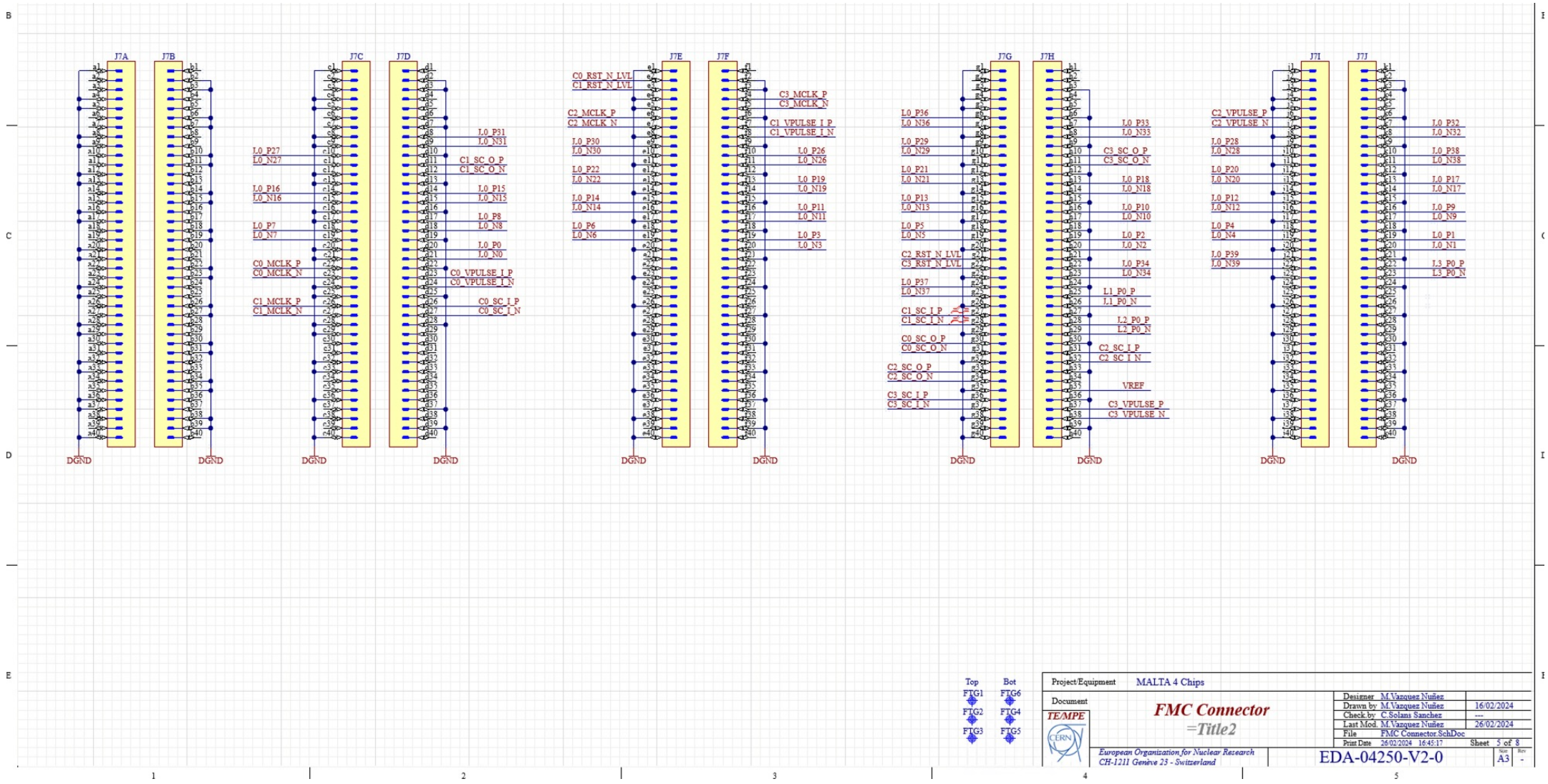
CHIP 2 - Slave


IC2A
IC2B
IC2C
IC2D
IC2E
IC2F
Part IC2B
CERN_MALTA_V2
Project/Equipment MALTA 4 Chips
Document
Malta Chip2
=Title2
TEMPE
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland
EDA-04250-V2-0

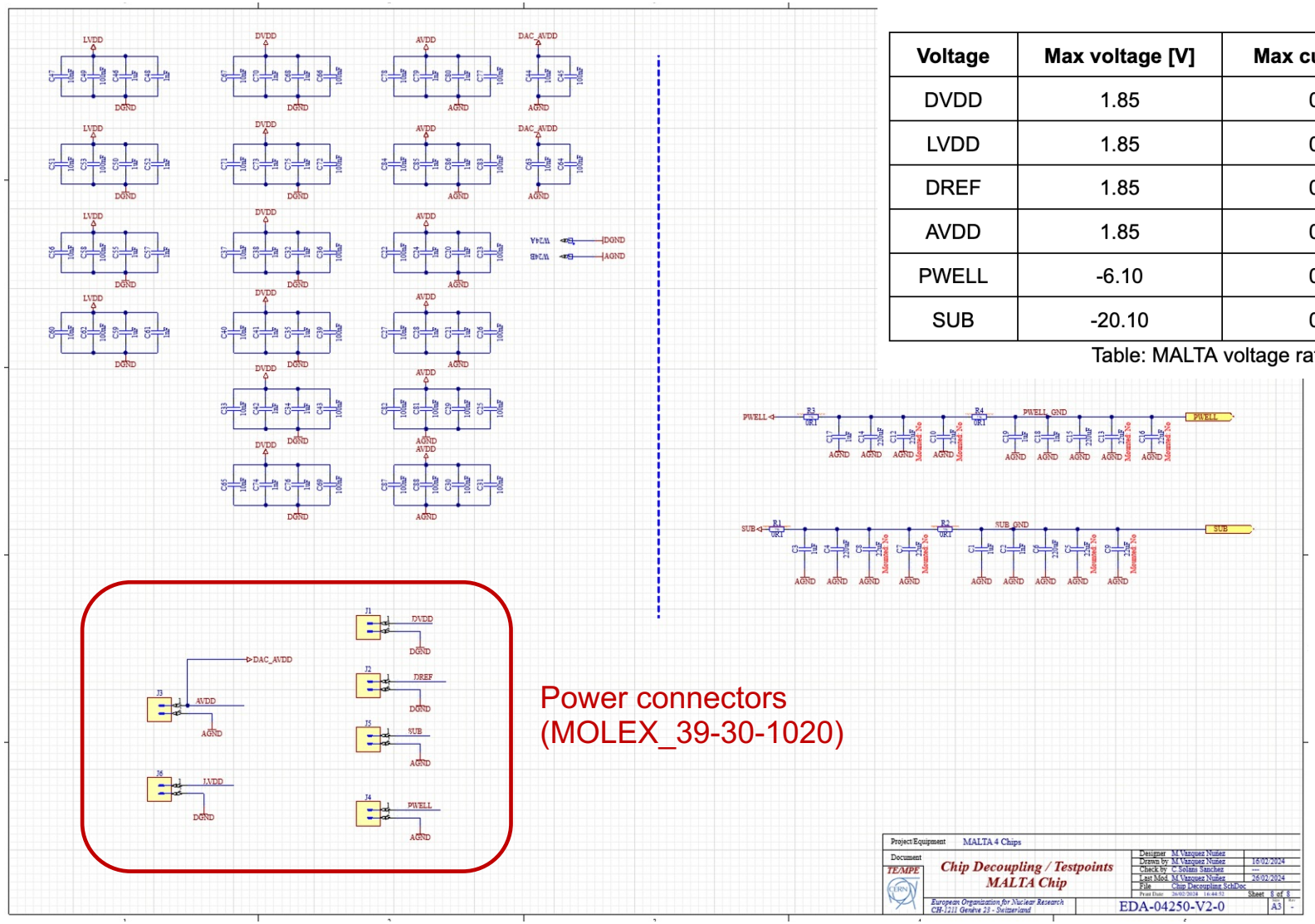
CHIP 3 - Slave


IC3A
IC3B
IC3C
IC3D
IC3E
IC3F
SUB_LEFT
SUB_RIGHT
PIXEL_MON_3
PIXEL_MON_2
PIXEL_MON_1
PIXEL_MON_0
PIXEL_MON_7
PIXEL_MON_6
PIXEL_MON_5
PIXEL_MON_4
VCASN_MON_LEFT
VCASN_DACMON_L
VCASN_MON_RIGHT
VCASN_DACMON_R
PWELL
AVDD_DAC_LEFT
AVDD_DAC_RIGHT
AVSS_DAC_LEFT
AVSS_DAC_RIGHT
POWER_EN_LEFT
POWER_EN_RIGHT
C3_AVDD_DAC
C3_AVSS_DAC
DVDD
DVSS
LVDD
LVSS
DGND
AVDD
AGND
MCLK_I_P_BOT
MCLK_I_N_BOT
SCTRL_I_P_BOT
SCTRL_I_N_BOT
SCTRL_O_P_BOT
SCTRL_O_N_BOT
TRIGGER_I_P_BOT
TRIGGER_I_N_BOT
VPULSE_I_P_BOT
VPULSE_I_N_BOT
SC_LOAD
CHIPID<2>
CHIPID<1>
CHIPID<0>
SUB_BOTTOM<2>
SUB_BOTTOM<1>
DACMONI_4
DACMONI_3
DACMONI_2
DACMONI_1
DACMONI_0
DACMONV_5
DACMONV_4
DACMONV_3
DACMONV_2
DACMONV_1
DACMONV_0
RST_N
DiePad
Project/Equipment
MALTA 4 Chips
Document
Malta Chip3
=Title2
TE/MPE
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland
EDA-04250-V2-0
Designer M.Vazquez Nuñez
Drawn by M.Vazquez Nuñez
Check by C.Solans Sanchez
Last Mod. M.Vazquez Nuñez
File MALTA2 Chip3.SchDoc
Sheet 4 of 8
A3

FMC Connector - HPC



Power connectors & decoupling capacitors

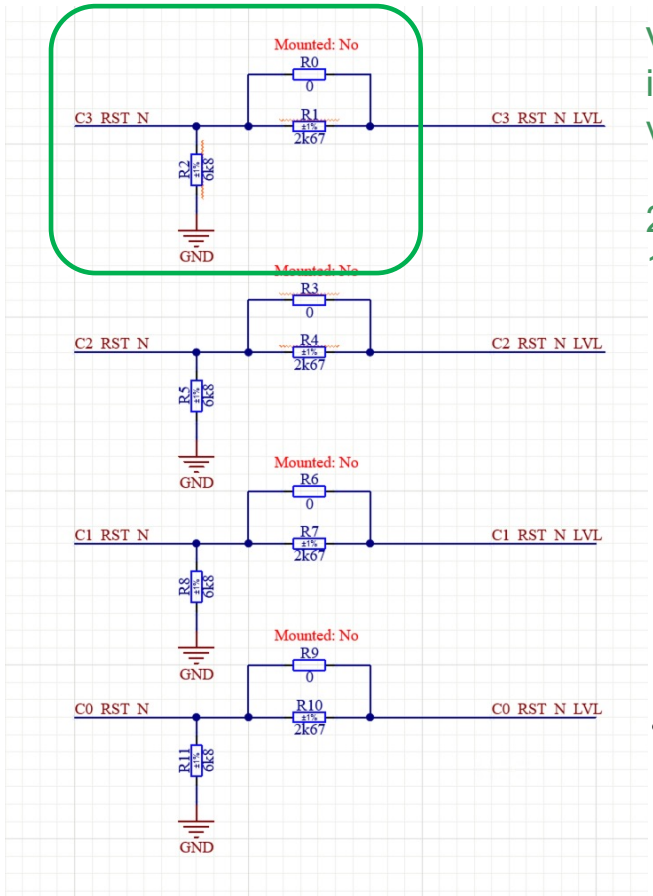


Voltage	Max voltage [V]	Max current [A]	Voltage range [V]
DVDD	1.85	0.50	1.80
LVDD	1.85	0.10	1.80
DREF	1.85	0.10	1.80
AVDD	1.85	0.70	1.80
PWELL	-6.10	0.05	-6.00 - 0.00
SUB	-20.10	0.05	-20.00 - 0.00

Table: MALTA voltage ratings and ranges

Waiting for other power connectors

Reset & chip ID



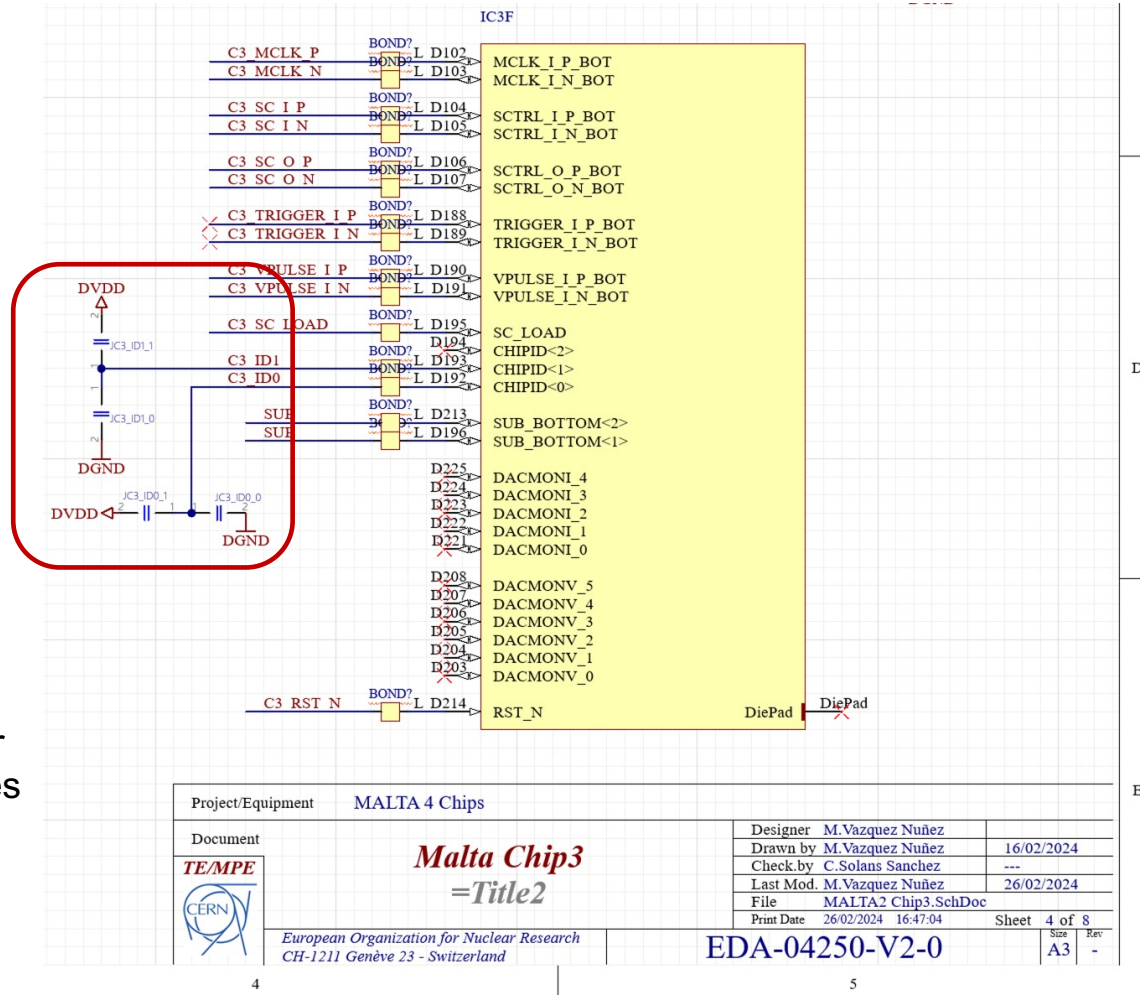
Reset signals

Voltage dividers were implemented to reduce the voltage from 2.5V to 1.8 V.

2.5V → comes from FPGA
1.8V → goes to the chip

Solder jumpers were implemented like switches (easier to solder and unsolder) to choose in between '1' and '0'

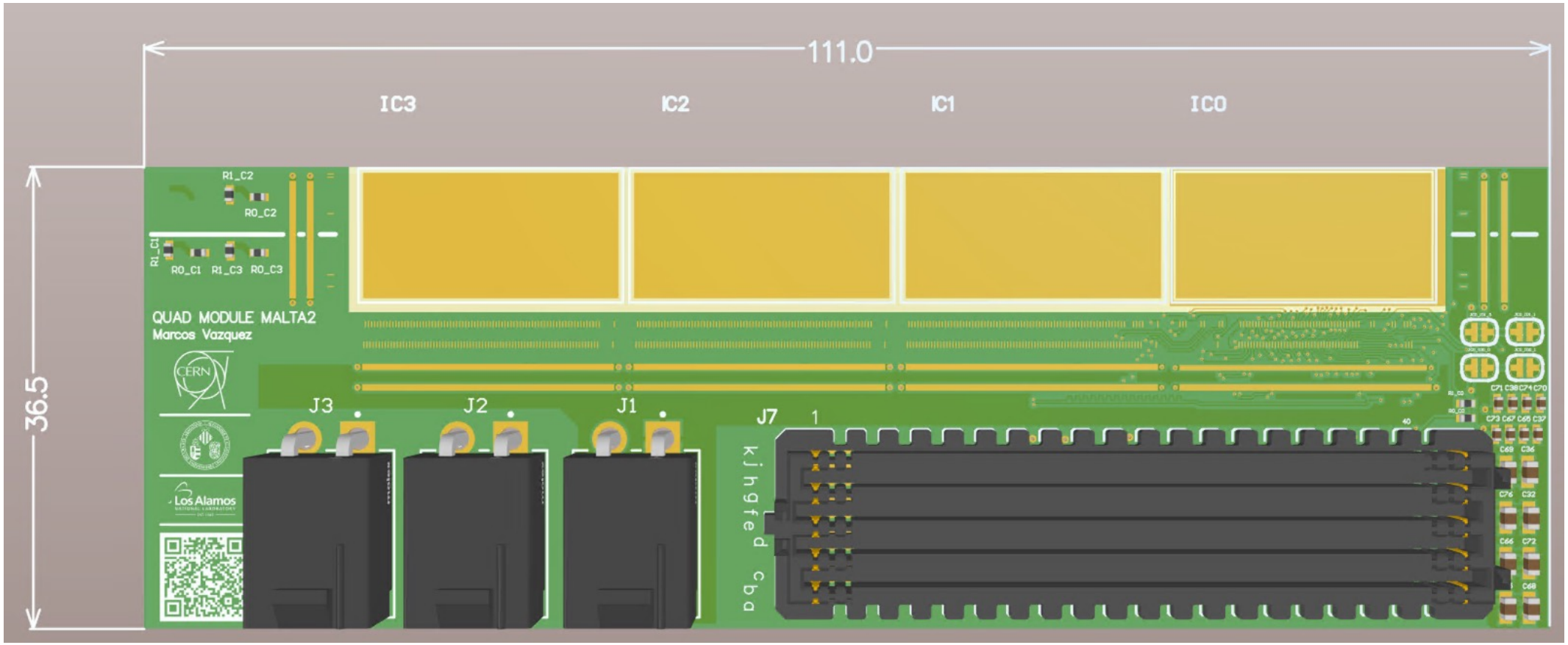
- Chip ID has two bits, because four chips will be implemented (3 slaves + 1 master chips).
  - "00" → CHIP 3 (slave)
  - "01" → CHIP 2 (slave)
  - "10" → CHIP 1 (slave)
  - "11" → CHIP 0 (master)



Chip ID (Chip 3 in this picture)

3D view – Front side

- Minimal distance required from bonding lab to do wirebonding in between MALTA2 chips is at least 800 microns
- Distance in between chips will be 900 µm for this first version



PCB details

- MALTA2 quad module PCB V1 will have the following dimensions:
  - 111 mm x 36.5 mm x 0.4 mm

- Material for high-speed signals: I-Tera MT40
  - https://www.isola-group.com/pcb-laminates-prepreg/i-tera-mt40/

- Thickness: ~ 400 µm for 4 layers in stack-up
  - Advantage against MALTA QUAD module (12 layers used). Minimal thickness can be 1.3 - 1.5 mm
  - Minimal thickness of MALTA2 QUAD module has been divided by 3 compared to MALTA QUAD, thus less dead material in the PCB.

- FMC pinout was changed for PCB routing optimisation
  - HPC FMC connector used. Module cannot be tested with LPC connector, due to both banks of the connector are used (A and B).

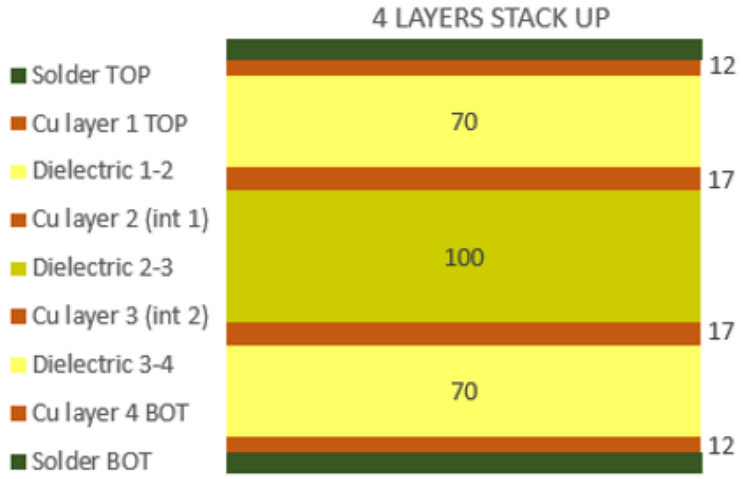
- 460 CHF/unit

Stack-up

- Total thickness will be ~ 400 µm in this version (398 µm)
  - Soldermask thick → 25 µm
  - Top and bottom copper layers → 12 µm
  - Core → 100 µm (I-Terra MT40 material)
  - Prepreg → 70 µm (1067H of I-Tera MT40 material)
  - Metallisation drilled layer → 25 – 25 = 50 µm

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.025mm	3.5	0
1	Top Layer		Signal	1/2oz	0.012mm		
	Dielectric 1		Prepreg		0.07mm	3.08	0.002
2	GND		Plane	1oz	0.017mm		
	Dielectric 11		Core		0.1mm	3.26	0.0025
3	Internal layer		Signal	1oz	0.017mm		
	Dielectric 2		Prepreg		0.07mm	3.08	0.002
4	Bottom Layer		Signal	1/2oz	0.012mm		
	Bottom Solder	Solder Resist	Solder Mask		0.025mm	3.5	0
	Bottom Overlay		Overlay				

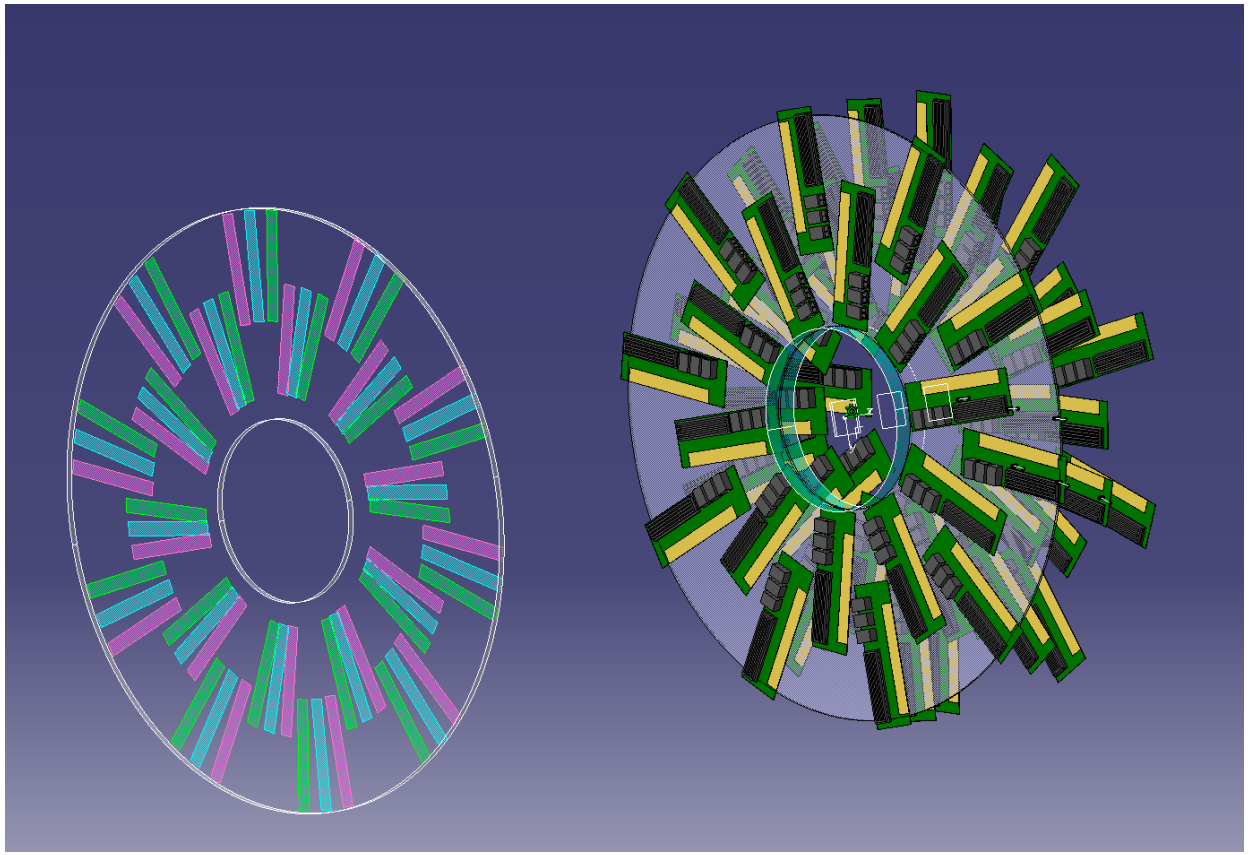
Altium stack-up

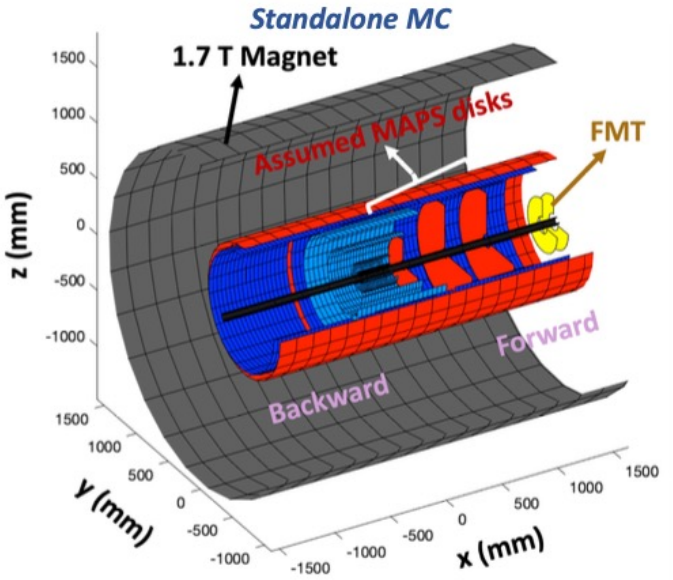


Manufacturer stack-up

Mechanical studies of the detector disk for FMT

- Regarding the dimensions provided, our mechanicals engineers were simulating a disk with 3 different modules layers (pink, blue and green) to cover the dead material as efficiently as possible.



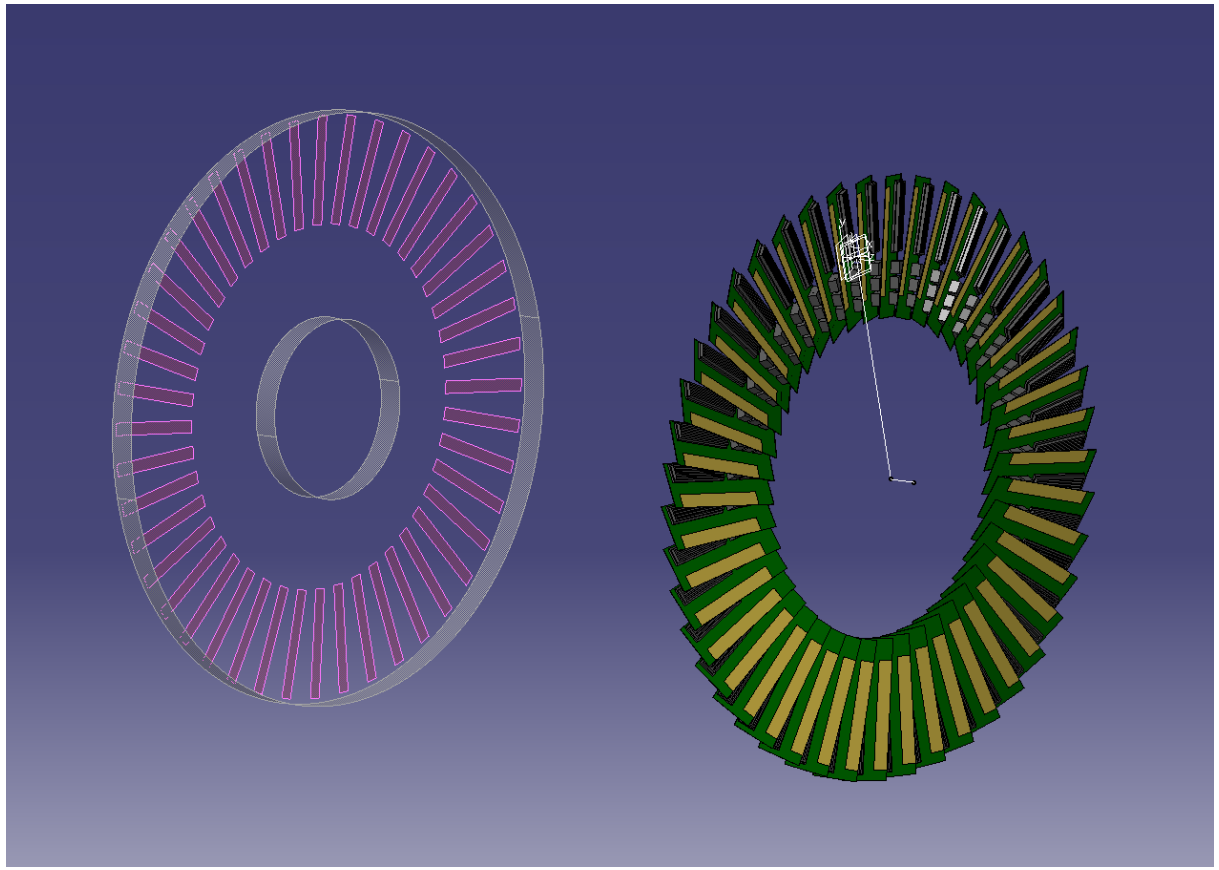


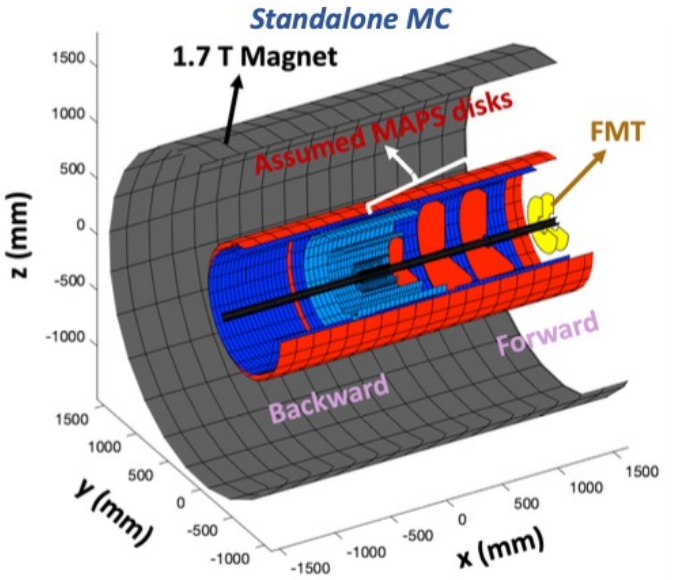
Hadron endcap FMT geometry (config 2)

Parameter	Disk 1	Disk 2
Inner Radius	7.014 cm	7.014 cm
Outer Radius	23.095 cm	23.095 cm
z location	145 cm	165 cm
Material budget	0.74%X/X_0	0.74%X/X_0
Average hit efficiency	98%	98%

Mechanical studies of the detector disk for FMT

- Regarding the dimensions provided, our mechanicals engineers were simulating a disk with 2 different modules layers (pink) to cover the dead material as efficiently as possible.





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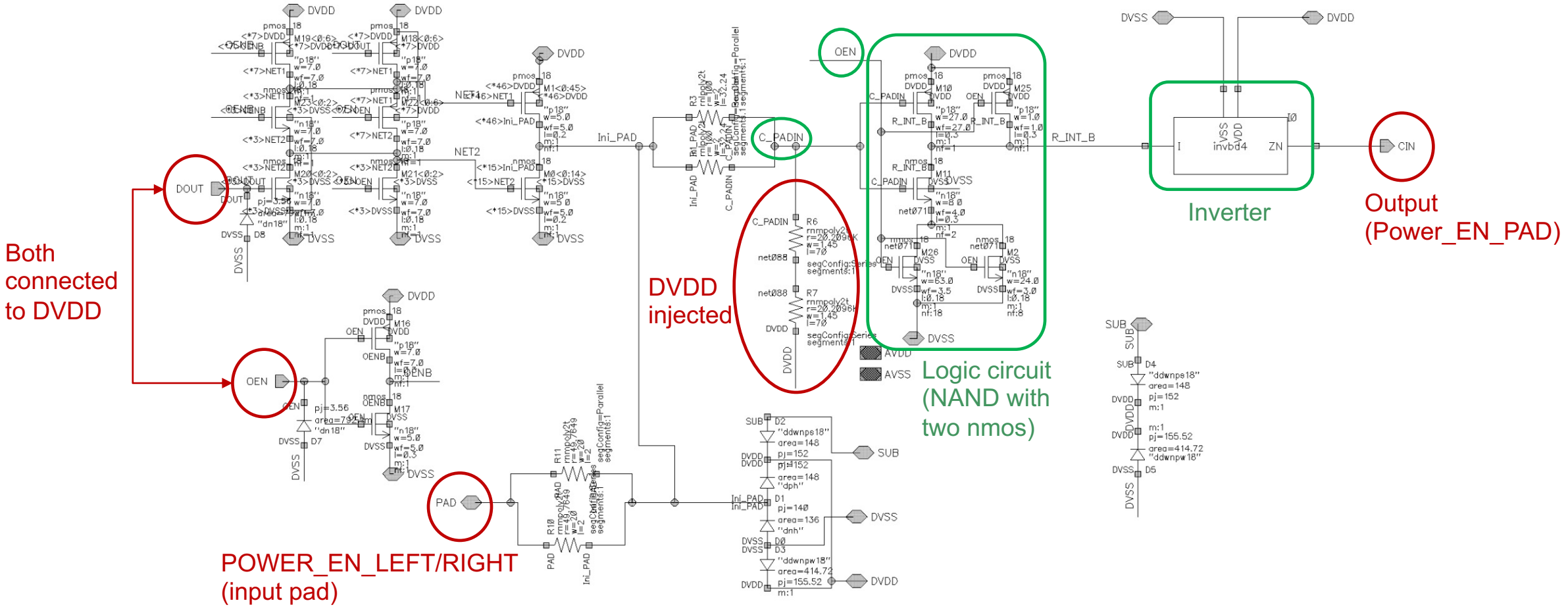
BACKUP

17/06/24

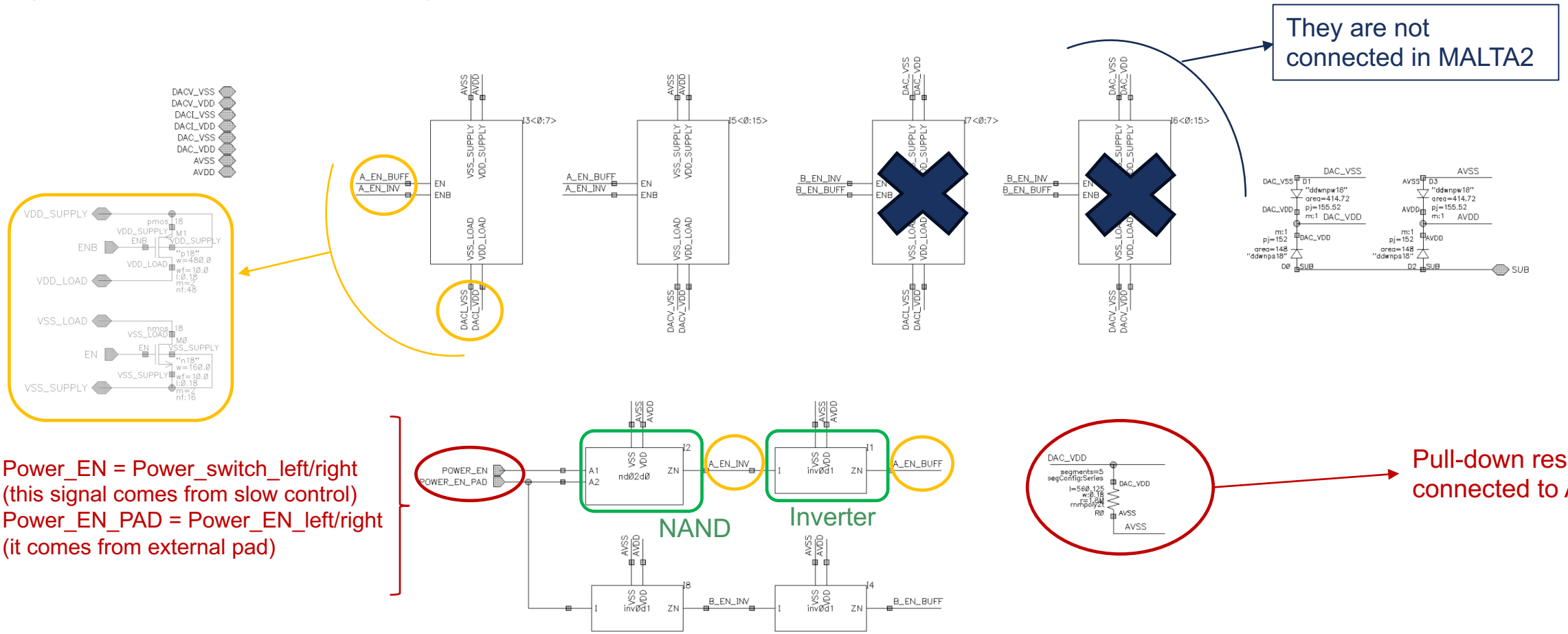
Pull-up in POWER_EN_LEFT/RIGHT by default

- Power_EN signal does not need to be connected, it is configurated in ‘1’ by default, with OEN = DVDD = ‘1’ and C_PADIN = ‘1’ at the NAND input, CIN = ‘1’ (output)



Pull-down resistor in DAC_VDD

- Every left and right DAC power (DAC_VDD) has a pull down resistor implemented in MALTA2 chip (AVDD_DAC_LEFT/RIGHT)



3D view– Back side