Quad Module – MALTA2 V1

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Introduction

(a) IC0 Master; IC1 Slave
CHIP 1 - Slave
CHIP 2 - Slave
Power connectors & decoupling capacitors

Waiting for other power connectors

Table: MALTA voltage ratings and ranges

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Max voltage [V]</th>
<th>Max current [A]</th>
<th>Voltage range [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVDD</td>
<td>1.85</td>
<td>0.50</td>
<td>1.80</td>
</tr>
<tr>
<td>LVDD</td>
<td>1.85</td>
<td>0.10</td>
<td>1.80</td>
</tr>
<tr>
<td>DREF</td>
<td>1.85</td>
<td>0.10</td>
<td>1.80</td>
</tr>
<tr>
<td>AVDD</td>
<td>1.85</td>
<td>0.70</td>
<td>1.80</td>
</tr>
<tr>
<td>PWELL</td>
<td>-6.10</td>
<td>0.05</td>
<td>-6.00 - 0.00</td>
</tr>
<tr>
<td>SUB</td>
<td>-20.10</td>
<td>0.05</td>
<td>-20.00 - 0.00</td>
</tr>
</tbody>
</table>

Power connectors (MOLEX_39-30-1020)
Reset & chip ID

Voltage dividers were implemented to reduce the voltage from 2.5V to 1.8 V.

2.5V → comes from FPGA
1.8V → goes to the chip

Solder jumpers were implemented like switches (easier to solder and unsolder) to choose in between ‘1’ and ‘0’

- Chip ID has two bits, because four chips will be implemented (3 slaves + 1 master chip).
  - “00” → CHIP 3 (slave)
  - “01” → CHIP 2 (slave)
  - “10” → CHIP 1 (slave)
  - “11” → CHIP 0 (master)
• Minimal distance required from bonding lab to do wirebonding in between MALTA2 chips is at least 800 microns
• Distance in between chips will be 900 µm for this first version
PCB details

- MALTA2 quad module PCB V1 will have the following dimensions:
  - 111 mm x 36.5 mm x 0.4 mm

- Material for high-speed signals: I-Tera MT40

- Thickness: ~ 400 µm for 4 layers in stack-up
  - Advantage against MALTA QUAD module (12 layers used). Minimal thickness can be 1.3 - 1.5 mm
  - Minimal thickness of MALTA2 QUAD module has been divided by 3 compared to MALTA QUAD, thus less dead material in the PCB.

- FMC pinout was changed for PCB routing optimisation
  - HPC FMC connector used. Module cannot be tested with LPC connector, due to both banks of the connector are used (A and B).

- 460 CHF/unit
Stack-up

- Total thickness will be ~ 400 µm in this version (398 µm)
- Soldermask thick → 25 µm
- Top and bottom copper layers → 12 µm
- Core → 100 µm (I-Terra MT40 material)
- Prepreg → 70 µm (1067H of I-Tera MT40 material)
- Metallisation drilled layer → 25 – 25 = 50 µm

### Altium stack-up

<table>
<thead>
<tr>
<th>#</th>
<th>Name</th>
<th>Material</th>
<th>Type</th>
<th>Weight</th>
<th>Thickness</th>
<th>Dk</th>
<th>Df</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Top Overlay</td>
<td>Overlay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Top Solder</td>
<td>Solder Resist</td>
<td>Solder Mask</td>
<td>0.025mm</td>
<td>3.5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Top Layer</td>
<td>Signal</td>
<td>1/2oz</td>
<td>0.012mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Dielectric 1</td>
<td>Prepreg</td>
<td></td>
<td>0.07mm</td>
<td>3.08</td>
<td>0.002</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Plane</td>
<td>1oz</td>
<td>0.017mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Dielectric 11</td>
<td>Core</td>
<td></td>
<td>0.1mm</td>
<td>3.26</td>
<td>0.0025</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Internal layer</td>
<td>Signal</td>
<td>1oz</td>
<td>0.017mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Dielectric 2</td>
<td>Prepreg</td>
<td></td>
<td>0.07mm</td>
<td>3.08</td>
<td>0.002</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Bottom Layer</td>
<td>Signal</td>
<td>1/2oz</td>
<td>0.012mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Bottom Solder</td>
<td>Solder Resist</td>
<td>Solder Mask</td>
<td>0.025mm</td>
<td>3.5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Bottom Overlay</td>
<td>Overlay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Manufacturer stack-up

- 4 LAYERS STACK UP

- Solder TOP
- Cu layer 1 TOP
- Dielectric 1-2
- Cu layer 2 (Int 1)
- Dielectric 2-3
- Cu layer 3 (Int 2)
- Dielectric 3-4
- Cu layer 4 BOT
- Solder BOT

- Total thickness: 12 + 70 + 100 + 70 = 352 µm
Mechanical studies of the detector disk for FMT

- Regarding the dimensions provided, our mechanicals engineers were simulating a disk with 3 different modules layers (pink, blue and green) to cover the dead material as efficiently as possible.
Mechanical studies of the detector disk for FMT

- Regarding the dimensions provided, our mechanicals engineers were simulating a disk with 2 different modules layers (pink) to cover the dead material as efficiently as possible.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Disk 1</th>
<th>Disk 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Radius</td>
<td>7.014 cm</td>
<td>7.014 cm</td>
</tr>
<tr>
<td>Outer Radius</td>
<td>23.095 cm</td>
<td>23.095 cm</td>
</tr>
<tr>
<td>z location</td>
<td>145 cm</td>
<td>165 cm</td>
</tr>
<tr>
<td>Material budget</td>
<td>0.74%X/X₀</td>
<td>0.74%X/X₀</td>
</tr>
<tr>
<td>Average hit efficiency</td>
<td>98%</td>
<td>98%</td>
</tr>
</tbody>
</table>
BACKUP
17/06/24
Pull-up in POWER_EN_LEFT/RIGHT by default

- Power_EN signal does not need to be connected, it is configured in ‘1’ by default, with OEN = DVDD = ‘1’ and C_PADIN = ‘1’ at the NAND input, CIN = ‘1’ (output)
Pull-down resistor in DAC_VDD

- Every left and right DAC power (DAC_VDD) has a pull down resistor implemented in MALTA2 chip (AVDD_DAC_LEFT/RIGHT)

Power_EN = Power_switch_left/right (this signal comes from slow control)
Power_EN_PAD = Power_EN_left/right (it comes from external pad)

Pull-down resistor connected to AVSS