A TDC for characterization of KM3NeT PMTs

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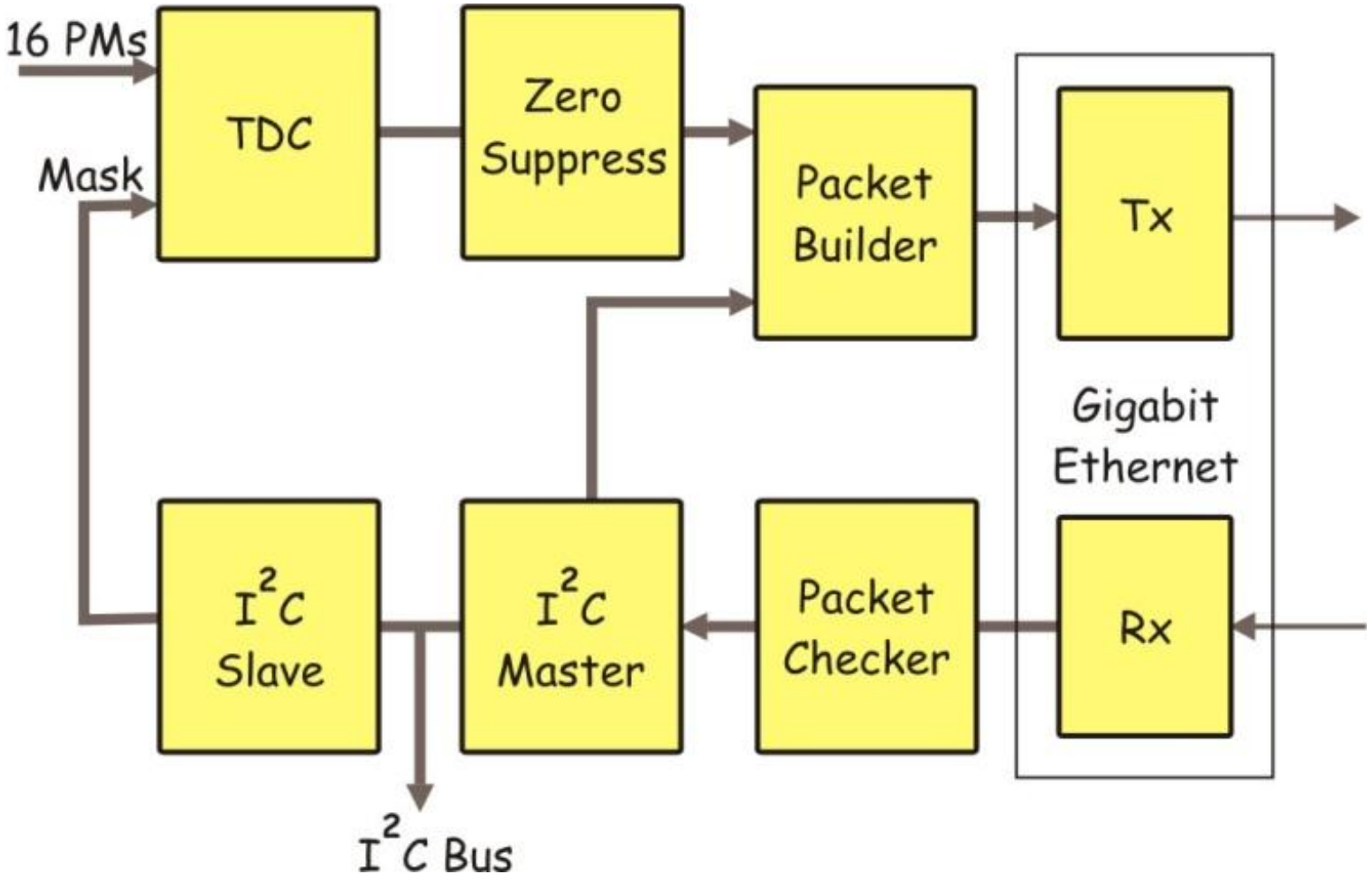
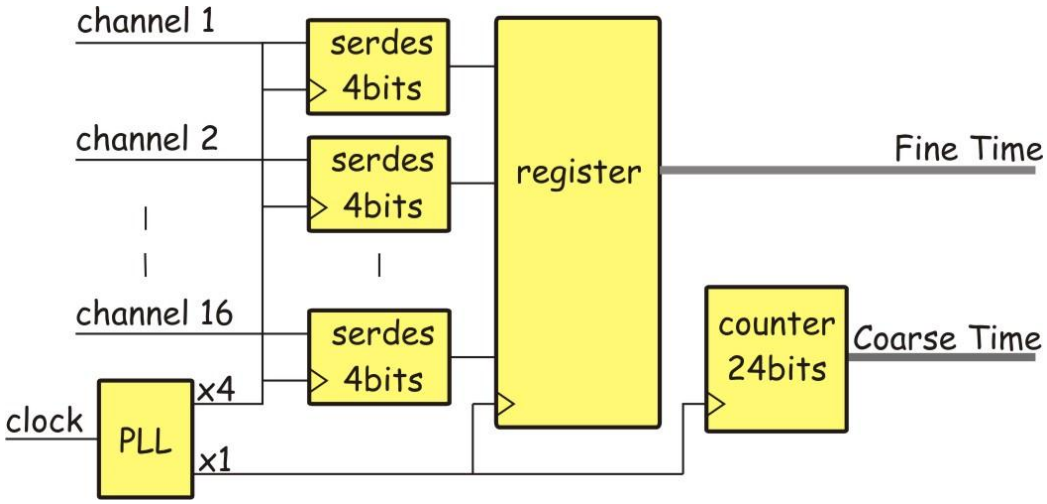
KM3NeT

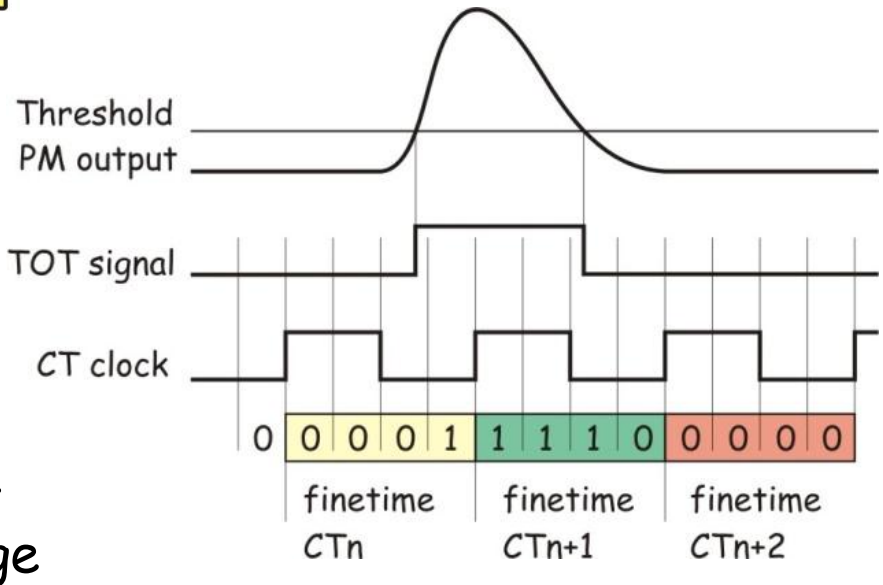
NIKHEF

Architecture



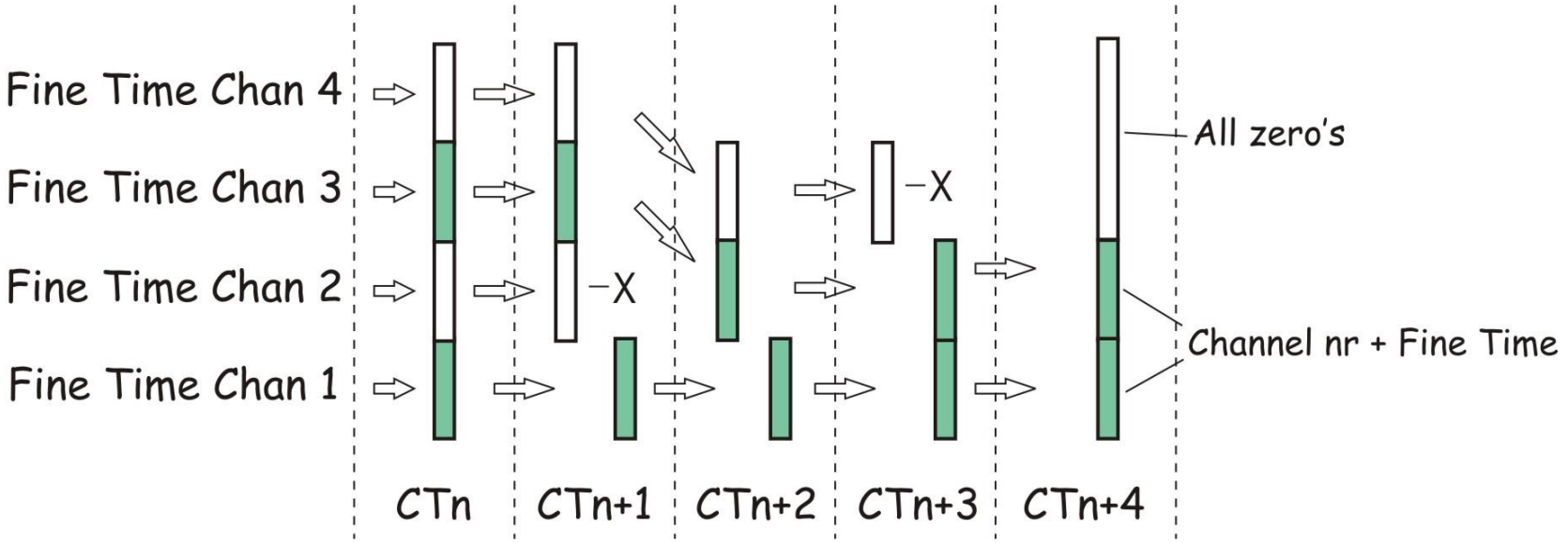
TDC





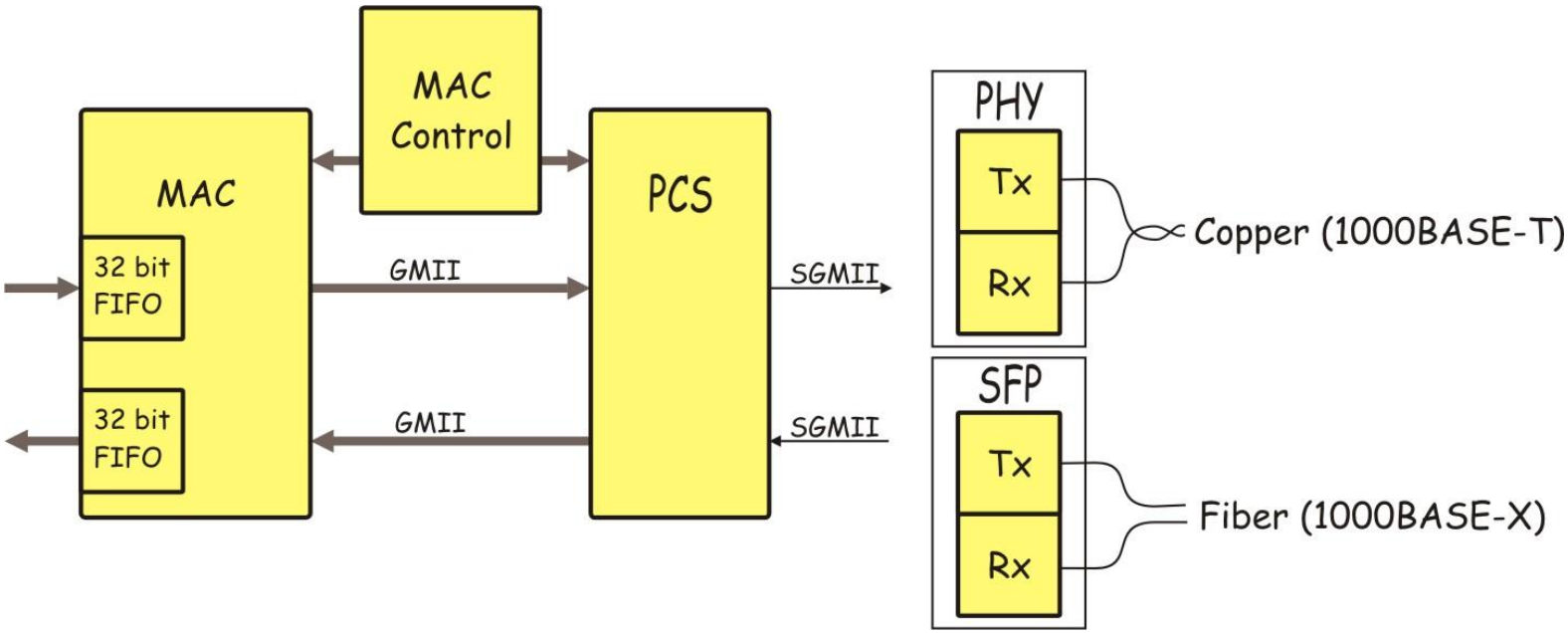
- Samples TOT signal with 4x Coarse Time Clock frequency of 100 MHz (Bin size = 2.5 ns)
- Phase Fine Time Clock and Coarse Time Clock is fixed by PLL
- Only the Fine Time of leading edge and trailing edge appears in the event data

Zero Suppress



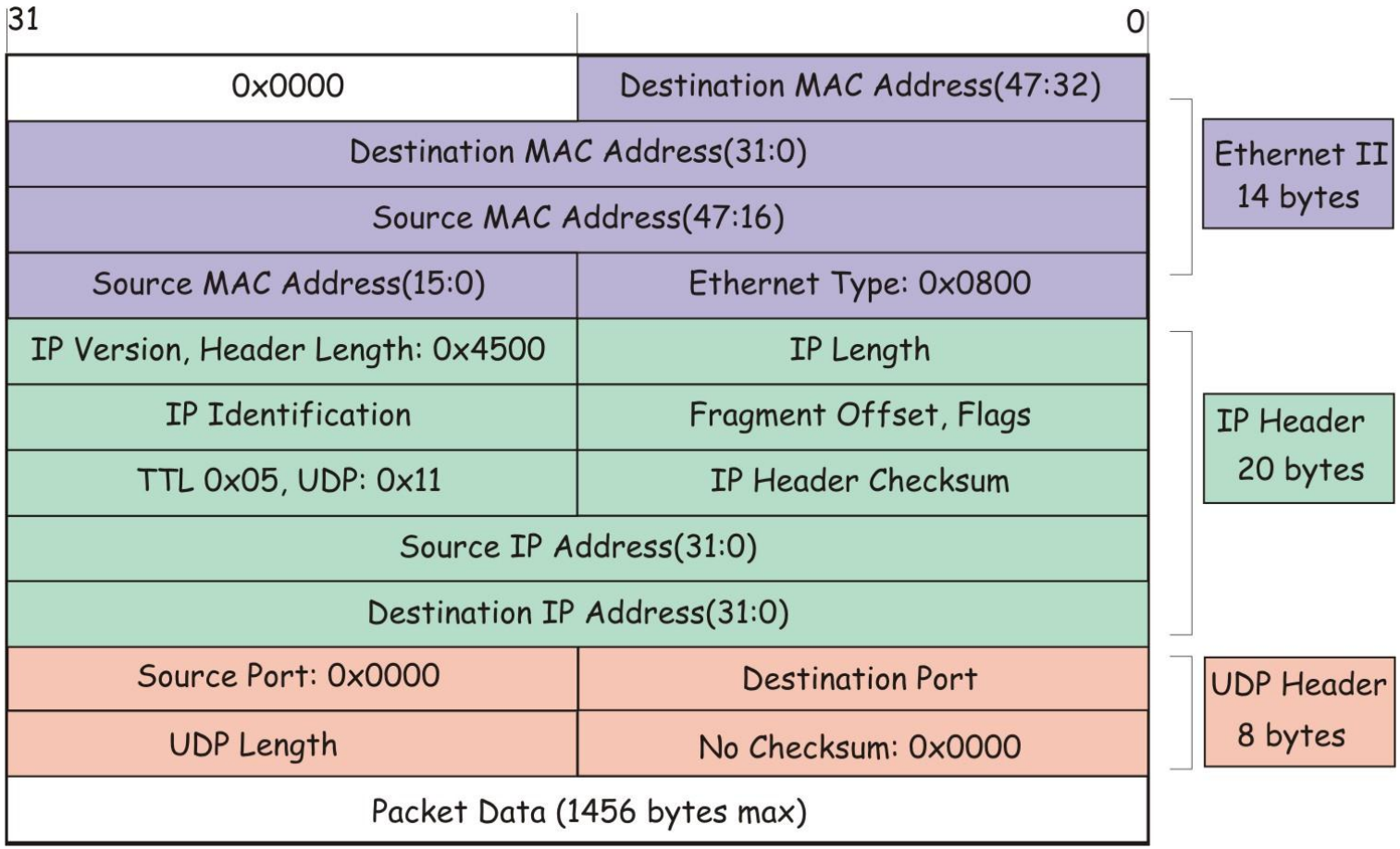
- Example of a 4 channel zero suppression mechanism:
  Two registers per pipeline stage one with only valid data and the second with data to be checked
  After 4 Coarse Time periods only the TDC channels with valid data are left
- 16 Coarse Time periods are needed for 16 channels
- Only the Channel Number with Fine Time of leading edge and trailing edge appear in the event data

Gigabit Ethernet

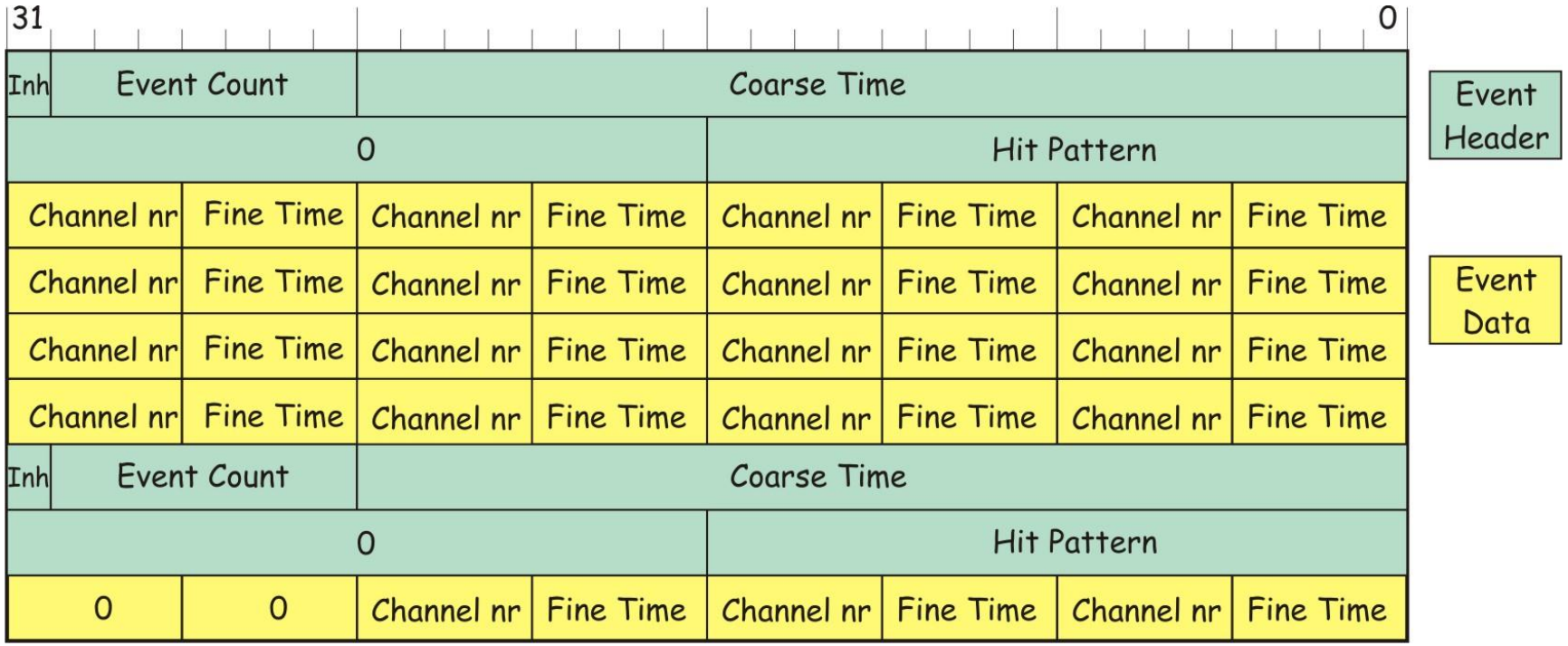


- MAC and PCS are IP-cores from Altera
- Interface to the MAC is 32 bit wide FIFO
- MAC Control initializes MAC and PCS at Reset
- SGMII interface to a PHY for 1000BASE-T or to a SFP module for 1000BASE-X connection

Event Packet



Event Format



- Data consistency checks possible with Event Count and Hit Pattern.
- The inhibit flag (Inh) indicates that events are missing due to high input rate.

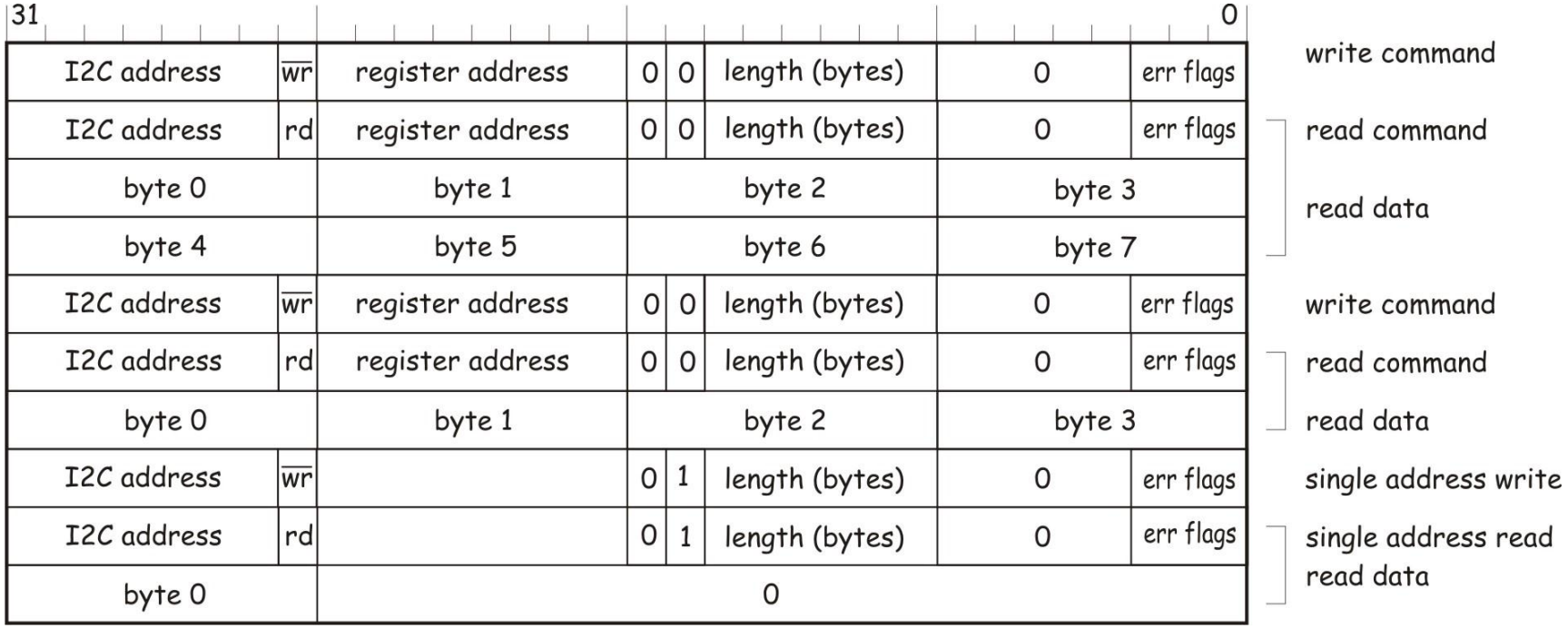
I2C Master

- Receives a command message from Ethernet
- Executes the I2C commands and checks acknowledges

31						0	
I2C address	$\overline{wr}$	register address	0	0	length (bytes)	0	write command
byte 0		byte 1		byte 2		byte 3	data to be written
byte 4		byte 5		byte 6		byte 7	
I2C address	rd	register address	0	0	length (bytes)	0	read command
I2C address	$\overline{wr}$	register address	0	0	length (bytes)	0	write command
byte 0		byte 1		byte 2		byte 3	data to be written
I2C address	rd	register address	0	0	length (bytes)	0	read command
I2C address	$\overline{wr}$		0	1	length (bytes)	0	single address write
byte 0		0					data
I2C address	rd		0	1	length (bytes)	0	single address read
end of I2C command (0xFFFFFFFF)							

I2C Master

- Returns an Ethernet message with the executed commands and read data

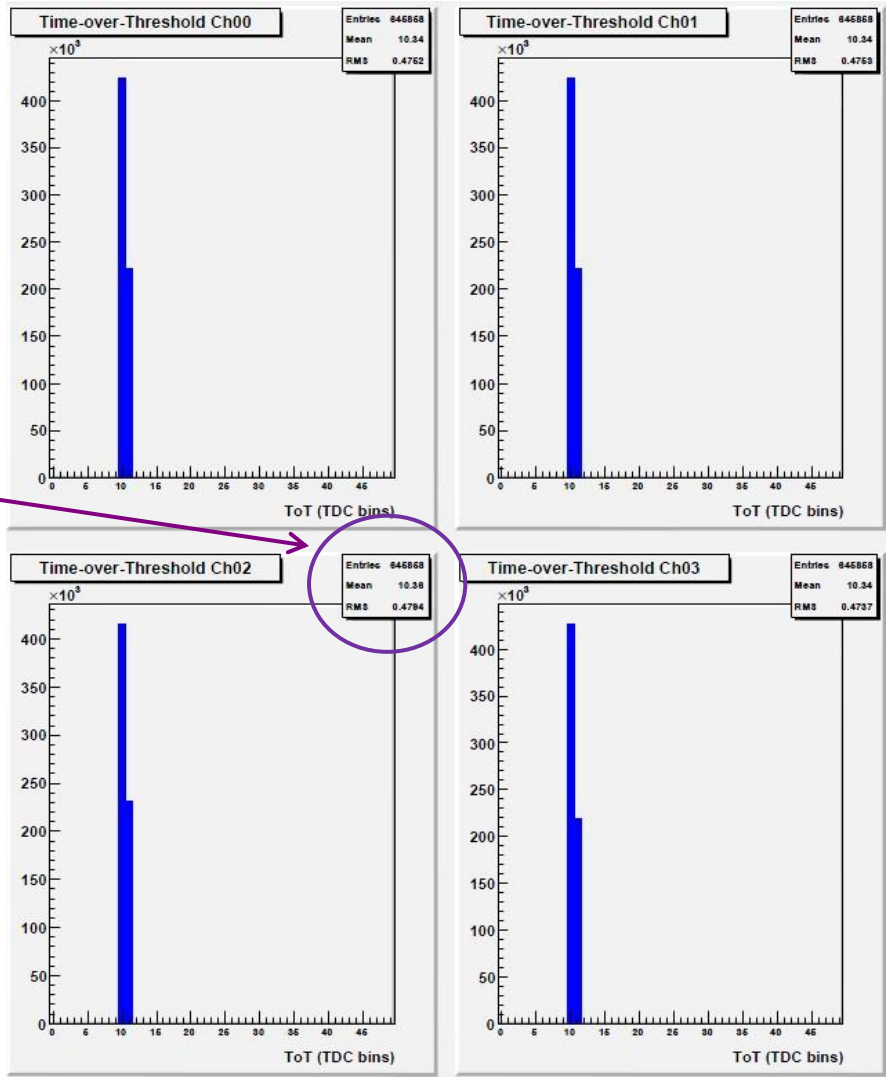


I2C Slave

register	nr	R/W	length	default value
revision number	0	RO	4 bytes	none
coarse time init value	1	R/W	3 bytes	0
channel mask	2	R/W	2 bytes	0xFFFF
status	3	RO	1 byte	none
i2c clock divider	4	R/W	1 byte	0x1F
destination MAC address	5	R/W	6 bytes	0x0060CF2026FB
source IP address	6	R/W	4 bytes	0xC0A80000
destination IP address	7	R/W	4 bytes	0xC0A8000A
destination control port	8	R/W	2 bytes	0x1389 (5001)
destination data port	9	R/W	2 bytes	0x1388 (5000)

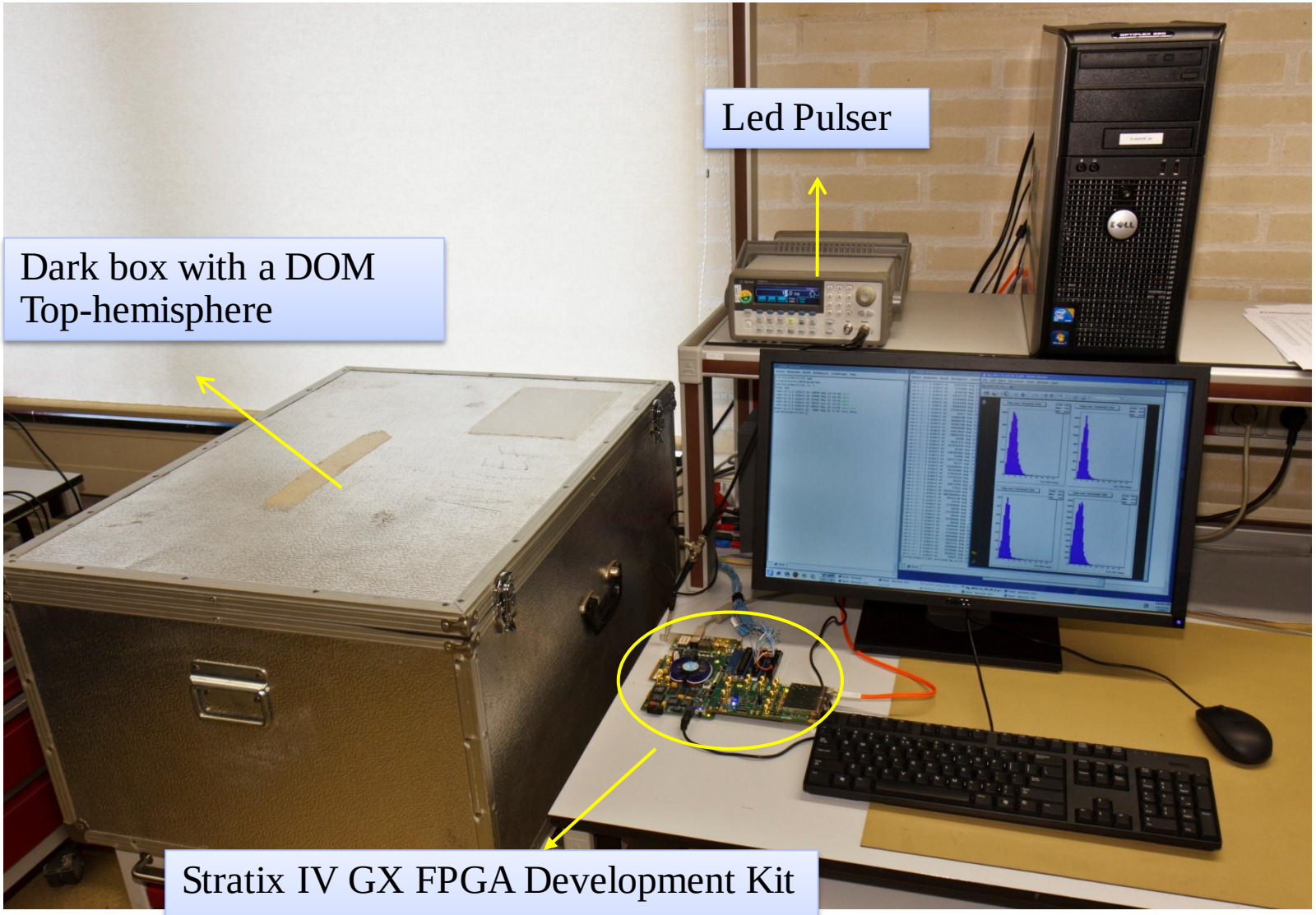
25 ns Pulse from Pulse Generator

Entries	645858
Mean	10.34
RMS	0.4752

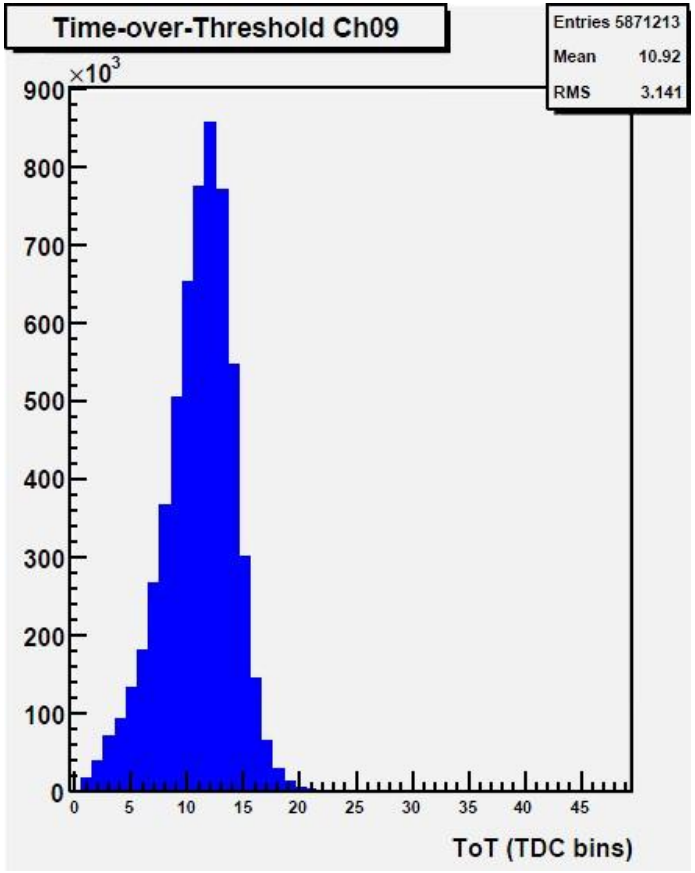


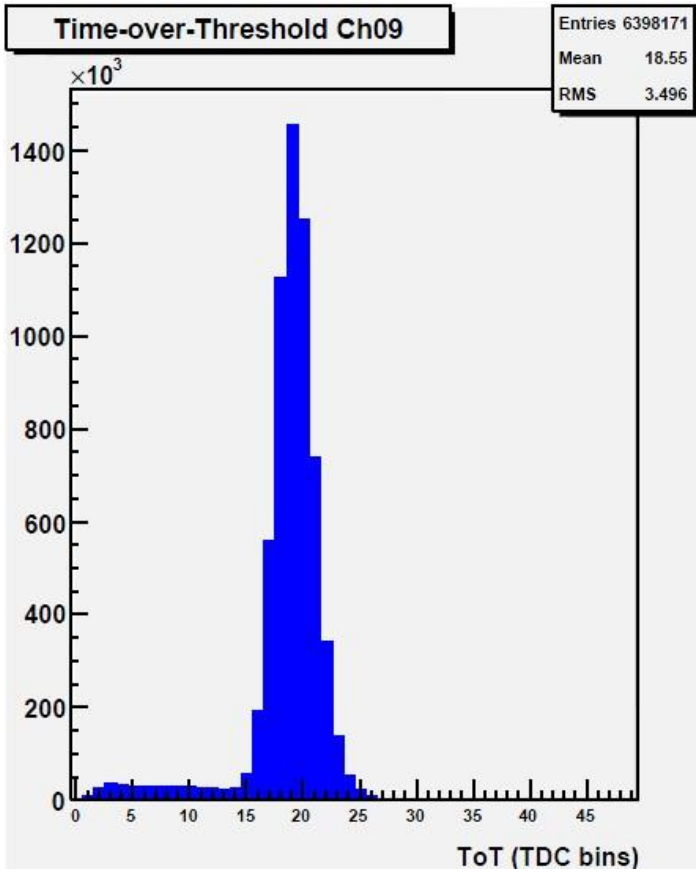
- Pulse width:
  10.34 x 2.5 ns = 25.85 ns

Setup


Led Pulser
Dark box with a DOM
Top-hemisphere
Stratix IV GX FPGA Development Kit
With SFP Mezzannine Board

First results: Led Flasher





- Plots of a PMT with led-flasher
  - Right plot: led pulse of 30 ns (mean = 10.92 bin)
  - Left plot: led pulse of 40 ns (mean = 18.55 bin)

Conclusions and Outlook

- A 16 Channel ToT TDC with Ethernet Readout/Control is realized in an Altera StratixIV GX FPGA:
- Device ; EP4SGX230KF40C2
  Logic utilization ; 3 %
  Total pins ; 84 / 888 (9 %)
  Total block memory bits ; 198,720 / 14,625,792 (1 %)
  Total PLLs ; 2 / 8 (25 %)

- TO DO:
  - Coding of the Fine Time can lower coarse clock keeping the same Bin Size resulting in less Ethernet Packages
  - Check Led – PMT response
  - Characterize single- Photon / multi-Photon response