Reconfigurable hardware applications on NetFPGA for network monitoring in large area sensor networks

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Introduction

- Advent of high bandwidth networks
  - remote sensors distributed over large areas send raw data to a single point of acquisition
- We propose a data aggregation system for:
  - Data inspection at network line speeds
  - Real-time triggers of multiple & diverse sensors
  - Reconfigurable hardware with programmable flexibility

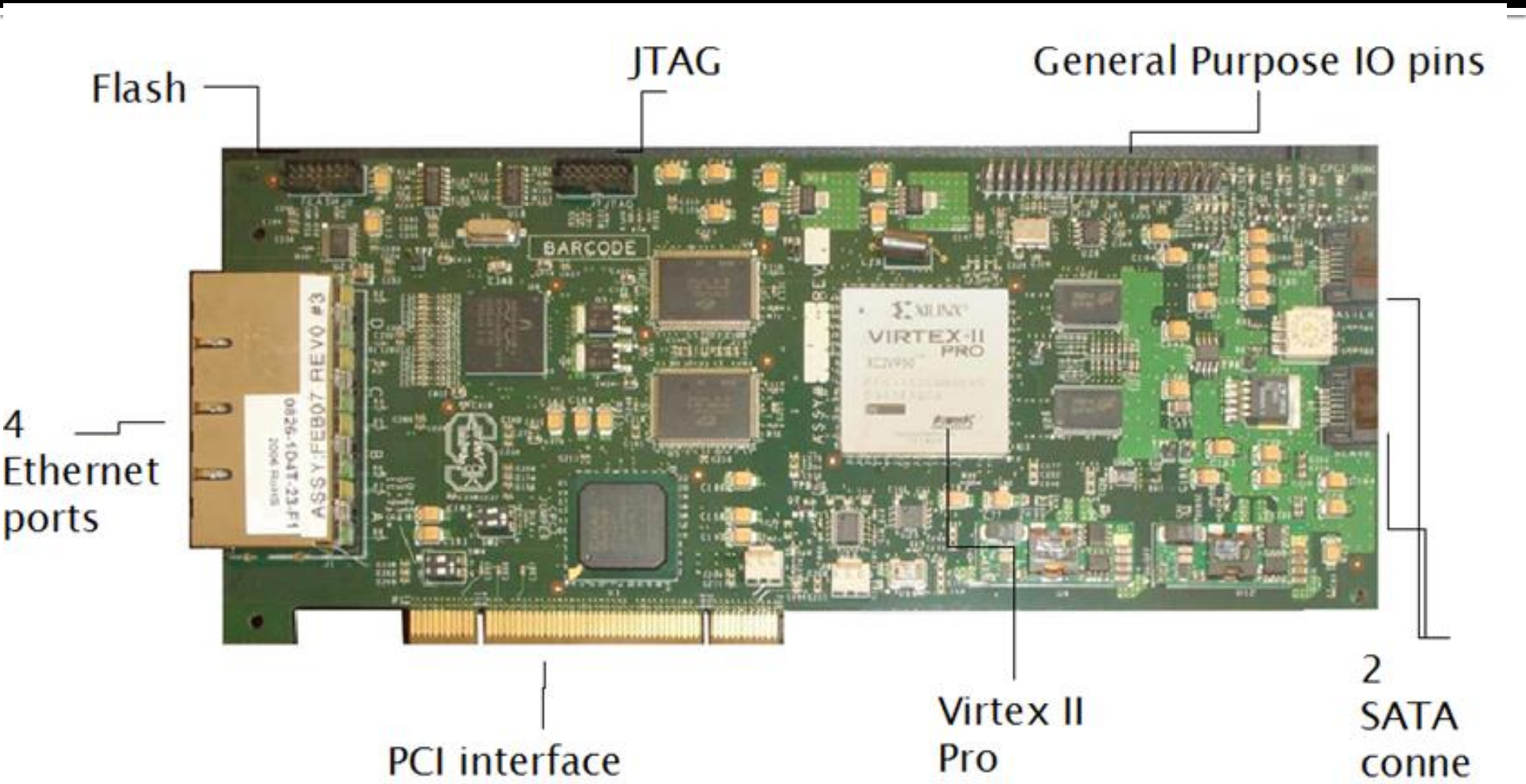
NetFPGA overview

- Open, multipurpose platform
- Provides a complete development tool chain:
  - Open-source, hardware-accelerated Packet Processing
  - Modular interfaces arranged in reference pipeline
  - Extensible platform
  - Large library of core packet processing functions
  - Scripts and GUI for simulation and system operation

NetFPGA overview

- Implemented with the cooperation of Stanford University and Xilinx.
- Low-cost reconfigurable hardware platform optimized for high-speed networking.
- Entire data path implemented in hardware
  - Supports back-to-back packets at full Gigabit line rates.
  - Processing latency measured in only a few cycles.

NetFPGA 1G (4x 1G)



NetFPGA (1G) Characteristics

- Virtex II PRO
- Embedded PowerPC – 2x PowerPC cores
- Gigabit Ethernet
  - 4 RJ45 ports
  - Broadcom PHY
- PCI
  - Memory Mapped registers
  - DMA Packet Transferring

Network Traffic monitor on NetFPGA

- Design a hardware accelerated Network Analyzer
  - implemented on **NetFPGA** platform
  - monitor network traffic
  - perform traffic filtering
- Compare our design to **AppMon**
  - AppMon: software application for monitoring network traffic

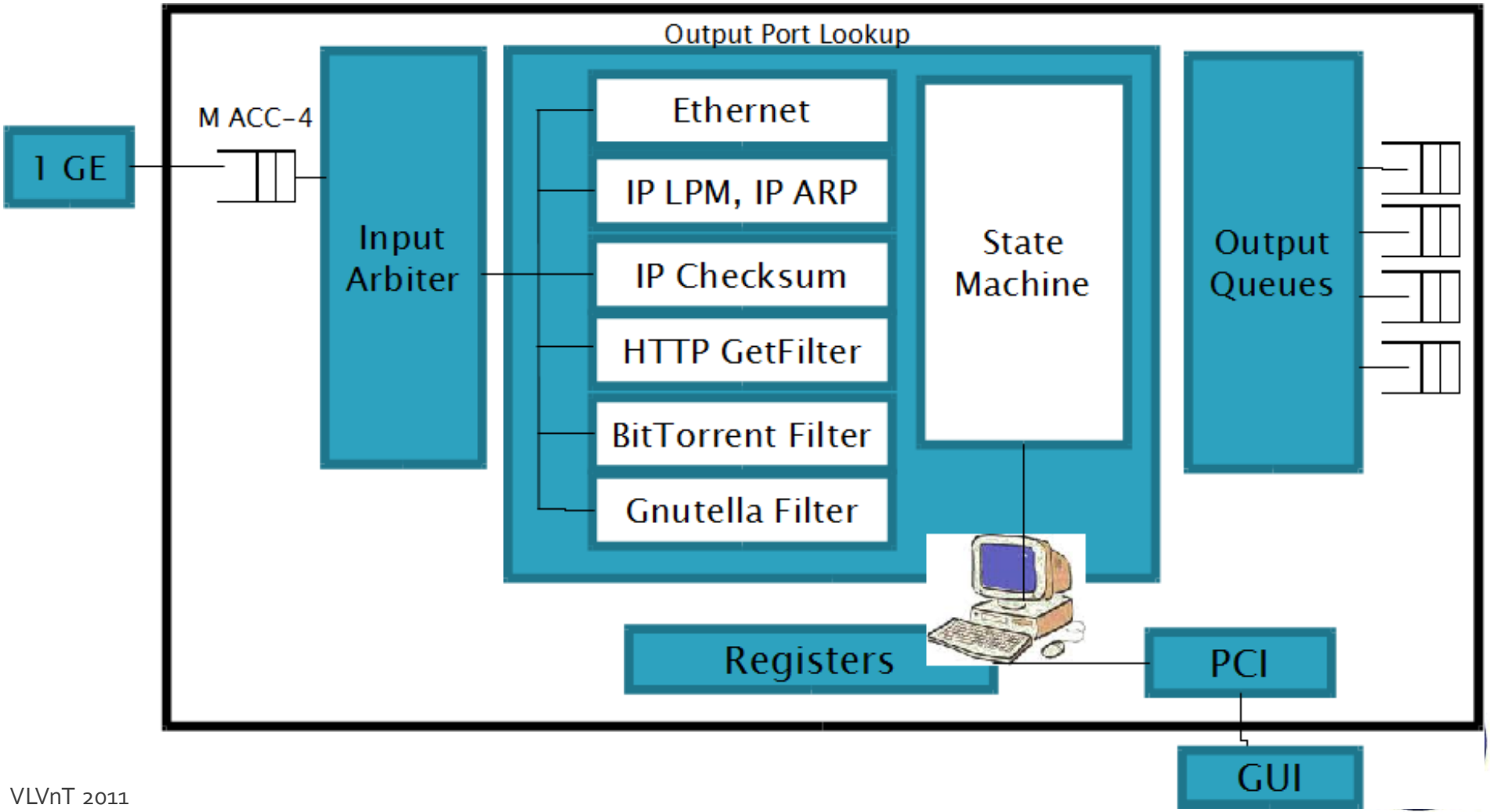
Network Traffic monitor on NetFPGA

- Both applications tested on same packets, using the same host computer
- Implemented protocols
  - HTTP
  - BitTorrent
  - Gnutella
  - Easily extensible to other protocols

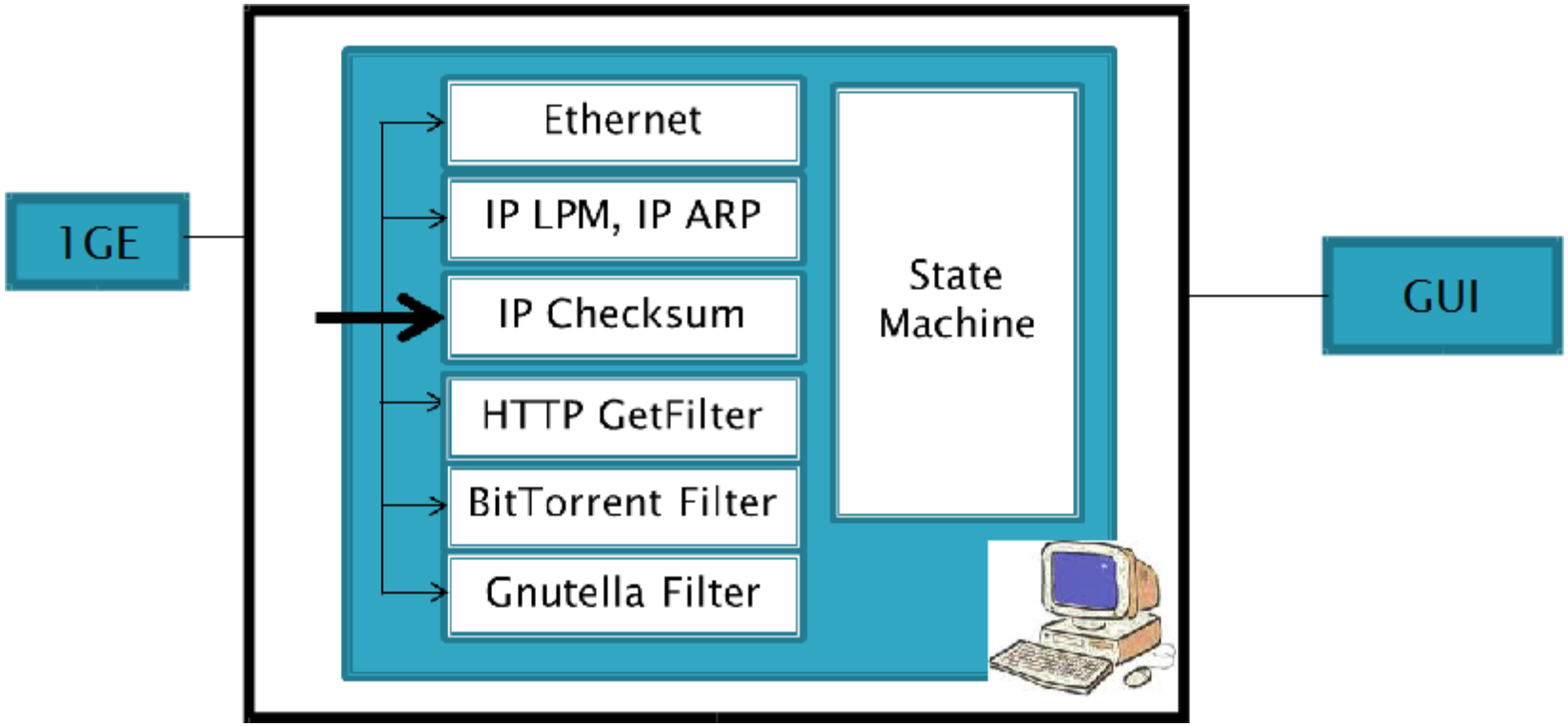
Network Traffic monitor on NetFPGA

- Upon packet arrival at an Ethernet port
  - perform a content-based inspection
  - identify the protocol that each packet uses
  - keep data in a hash table
- Deep-packet inspection completed
  - send the data to host via PCI interface.
- GUI at host displays data based on hash table

NetFPGA Network monitor block diagram

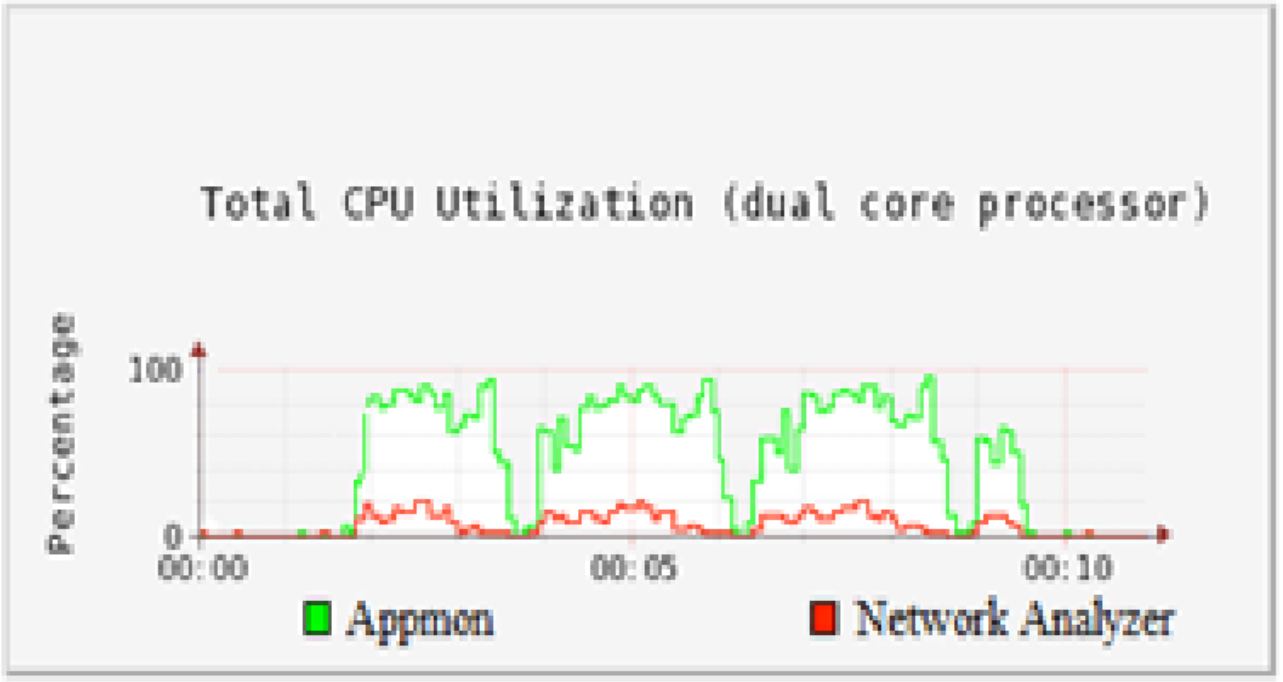


AppMon Block Diagram



Comparison Results

CPU utilization



Power Consumption

Implementation	Throughput (Mbps)	Power (W)	Power per BW (W/Gbps)
APPMON	500	130	260
NetFPGA	1000	14.4	14.4

Logic Resources utilization

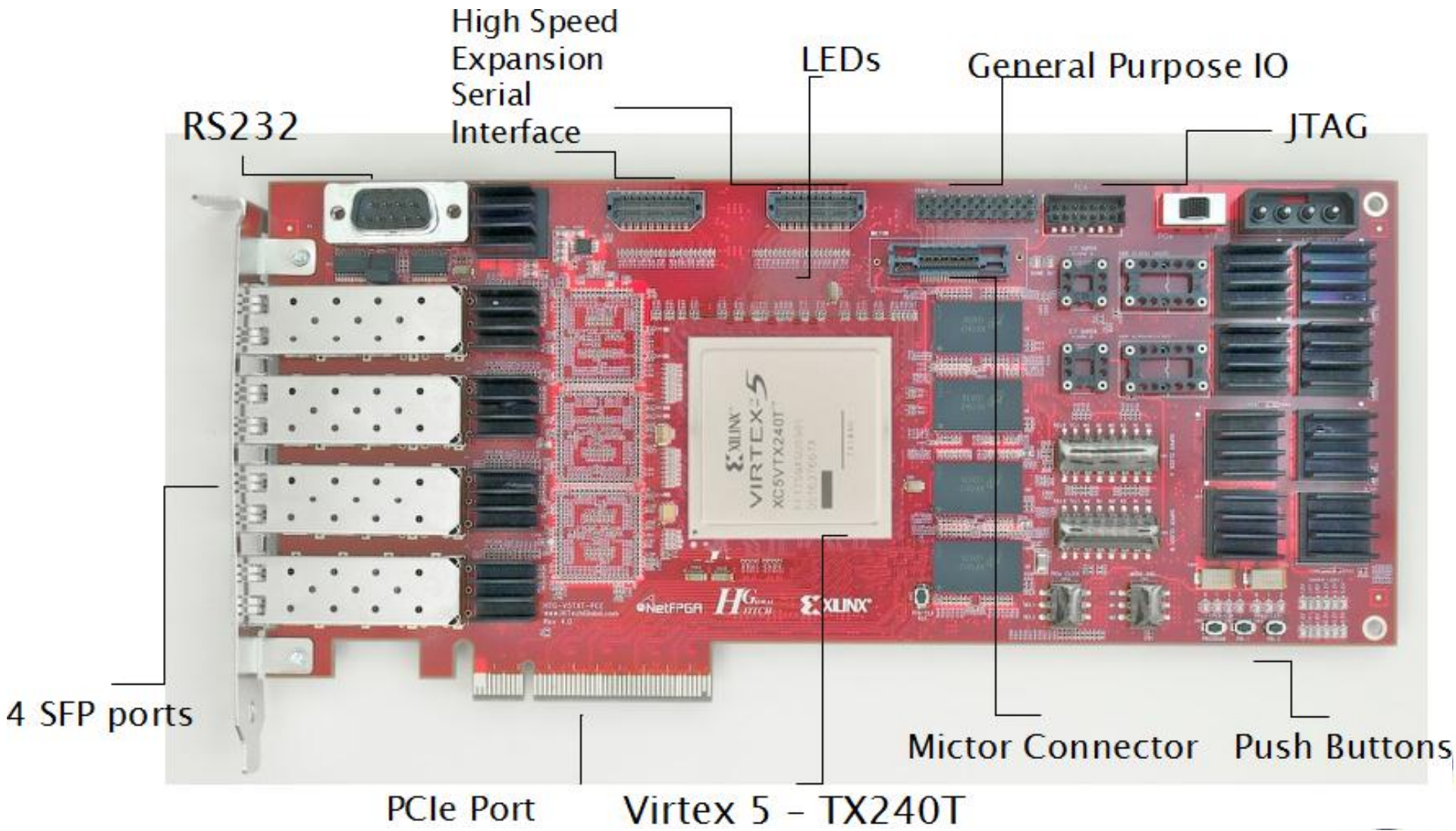
Type	Number	Percentage
Number of Slices	11.131	47%
Number of slice FF	9.387	19%
Number of 4-input LUT	16.547	35%
Number of BRAM	27	11%

- Minimum clock period : 5.51 ns (181 MHz)

Conclusions

- Efficient traffic monitoring application
  - implemented on NetFPGA
  - supports up to 4Gbps
  - compared to an existing application as proof of concept
- Next step: upscale our design to a throughput of 10Gbps
  - use the NetFPGA 10G (4 x 10G)

Towards… NetFPGA 10G



Thank you for your attention !!

Questions?

NetFPGA 10G characteristics

- Xilinx Virtex – 5
- 4 SFP+ interfaces
  - using 16 RocketIO GTX transceivers
  - 4 PHY devices
- X8 PCIe slot
- 20 Configurable GTX serial Transceivers
- 1Xilinx XC2C256 CPLD