Data readout system utilizing photonic integrated circuit

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Abstract

We describe a novel optical solution for data readout systems. The core of the system is an Indium-Phoshpide photonic integrated circuit performing as a front-end readout unit. It functions as an optical serializer in which the serialization of the input signal is provided by means of on-chip optical delay lines. The circuit employs electro-optic phase shifters to build amplitude modulators, power splitters for signal distribution, semiconductor optical amplifiers for signal amplification as well as on-chip reflectors. We present the concept of the system, the design and first characterization results of the devices that were fabricated in a multi-project wafer run.

Keywords: photonic integration, indium-phosphide, serialization, OTDM

1. Introduction

Recent high-energy physics experiments aim to build large-volume detectors. The principle of operation is dependent on the specific application, however all of them tend to generate huge amounts of output data. Generally, the scale of the project requires from the constructors extreme performance of the whole system, from the mechanics, electronics, data transfer and software point of view. A very important part of the detector is the data readout system, which has to be robust and reliable. This task is typically done by means of an optical core network in which the photonic devices (transmitters, modulators, receivers) are driven by electrical circuits [1-4]. The front-end readout is performed by electrical devices. However, none of the systems presented so far makes use of a complex photonic integrated circuit (PIC) in which a high number of optical functions have been combined.

In the coming years photonic ICs are believed to play an increasing role in many fields, especially in telecommunications, but also in datacommunications, medicine, metrology, sensing and others. In comparison to bulk fiber-optic or electrical equivalents, photonic integrated circuits offer advantageous performance in terms of size and weight, energy consumption, operational speed and bit-rate. Furthermore, photonic integration will also help to reduce the packaging cost of the devices as several functionalities (light generation, modulation, multiplexing) will be integrated on a single chip.

There are several technologies in which one can design and fabricate a photonic IC. The most important two are the Indium-Phosphide (InP)-based and Silicon (Si)-based technologies. The big advantage of the latter is that the technology is very mature and offers low-cost and large-scale fabrication of devices. However, due to the fundamental problem of the indirect bandgap of Silicon, efficient light generation is not possible, and Si-based circuits are limited to using passive components, modulators and detectors. On the other hand, InP-based materials, such as the quaternary alloy InGaAsP have a direct bandgap and are used for light generation and detection in the 900 nm - 1650 nm window. This enables the monolithic integration of passive components (waveguides, splitters, filters) with amplifiers, detectors and phase modulators. With these components, more complex circuits containing laser light sources, receivers, switches and routers can be fabricated.

InP-based photonics technology is increasingly mature and nowadays chips consisting of hundreds of components have been fabricated [5]. In addition, a radically new way to fabricate photonic ICs is being explored. Instead of developing a new technology almost for each new component or circuit, this new fabrication technology is standardizing on a few basic building blocks from which larger components and complex circuits can be synthesized. This new concept is being developed within the framework of European FP7 Projects EuroPIC [6] and PARADIGM [6]. The generic integration technology is based on the ideas taken from the silicon microelectronics approach. CMOS technology makes use of transistors, resistors and capacitors to build circuits that can be used for a very wide variety of applications. In InP photonics these basic building blocks can be a waveguide, a phase modulator, a semiconductor optical amplifier (SOA) and a polarization converter. More complicated components, such as power couplers and splitters, (de)multiplexers, on-chip reflectors, amplitude modulators, space-switches, various types of laser light sources, detectors and polarization independent de-

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vices may be built by using such building blocks. As a result, even highly complex circuits dedicated for different application fields may be designed and fabricated in a single technology process. We believe that once the generic model is established and fixed, it will reduce the cost of fabrication of a single chip by more than an order of magnitude. It will enable the access to cutting edge technology for small and medium enterprises as they will be able to apply photonic ICs in their devices and systems without the necessity of large investments in cleanroom facilities or technology development.

Another important idea which origins from the silicon microelectronics is the concept of a multi project wafer (MPW) run. This helps to reduce the cost of fabrication of photonic ICs as the area of the wafer is divided among many users, who pay for the chips proportionally to the occupied space. The MPW concept helps in reduction of research and development costs, as it enables low-cost prototyping. However, as such a run should be application blind, there has to be a fixed technology process in which the users design their circuits. Additionally, there have to be strict design-rule checks as the designs should not affect the neighboring cells. At present, the application of the concept of MPW runs in InP in photonics is being investigated. The COBRA Research Institute in Eindhoven (The Netherlands) already offers a small-scale access to MPW runs [6] and first trials have been performed at Oclaro in Caswell (UK) and Heinrich-Hertz Institut in Berlin (Germany). All involved parties are members of JePPIX, the Joint European Platform for InP-based Photonic Integrated Components and Circuits [6-8].

In this paper we present the concept of a readout system architecture, implemented in an InP-based photonic IC. This application specific photonic integrated circuit (ASPIC) is dedicated for use in a large-volume detector. We also present the first characterization results of the ASPICs that were designed in a generic approach and fabricated in MPW runs at Oclaro, within the framework of EuroPIC and the Dutch smartmix project Memphis [8].

2. EuroPIC Project

The European FP7 Project EuroPIC (European Manufacturing Platform for Photonic Integrated Circuits, europic.jeppix.eu) started in August 2009. It is a collaboration of key players in the European InP photonics - chip and packaging foundries, software companies, R&D companies, universities and also application users of the photonic devices.

The main objective of the project is to establish a standard production chain based on the generic technology approach. The concept of such a chain is shown in Figure 1. When a user has a concept of an application for a photonic IC, he can do the design by himself or ask a design house to do it for him. Once the design is complete, the resulting mask layout is sent to the foundry where the chip is fabricated. If the user wants to have the ASPIC packaged, the fabricated chips are sent to the packaging foundry. Eventually, the user receives the packaged devices for characterization and testing.

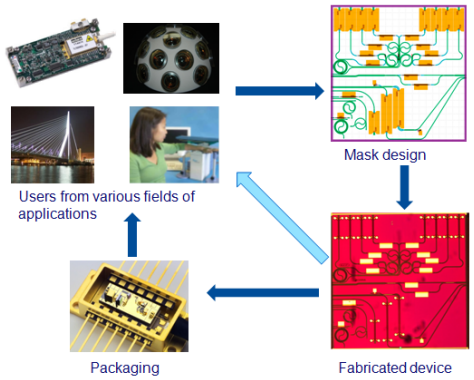

Figure 1: Concept of the generic technology production chain.

To establish such a chain, several objectives have to be reached. First of all, the foundry has to determine and describe the properties and the performance of the available building blocks in a design manual. Secondly, for an effective design process, there has to exist some dedicated software which has to enable simulations of basic and complex components, and eventually even full circuits. Additionally, it has to provide the possibility of making a mask layout and implement automated checks for violation of the foundry design rules. Furthermore, a standard for packaging has to be developed. This includes specification of the chip dimensions and of the number and the position of the optical and electrical interfaces to and from the chip. Finally, the foundry has to elaborate the validation process of the fabricated devices. The partners of EuroPIC are currently working to reach these objectives and the first results are very promising [9,10].

Additionally, EuroPIC aims to prove that chips fabricated in the very same technology process can be successfully used in various fields of application, such as telecommunications (access networks, Radio-over-Fiber systems), medicine, data read-out and sensing. On an early run, ten ASPICs were simultaneously designed and the mask layouts have been combined in a MPW run. This was the first of two planned runs at Oclaro and Heinrich-Hertz Institut each, and the chips are now being characterized. The second run is currently under way. Two of the fabricated ASPICs will be used to test a generic packaging scheme, developed by CIP Photonics (Ipswich, UK).

3. System architecture and the serializer concept

One of the EuroPIC pilot applications is the front-end readout unit for a neutrino telescope. Atlhough for this application the specifications have been taken from the KM3NeT project [11], the proposed solution is sufficiently general to make it suitable for use in other experiments.

KM3NeT aims at development and deployment of a cubic kilometer size neutrino telescope. The idea is to

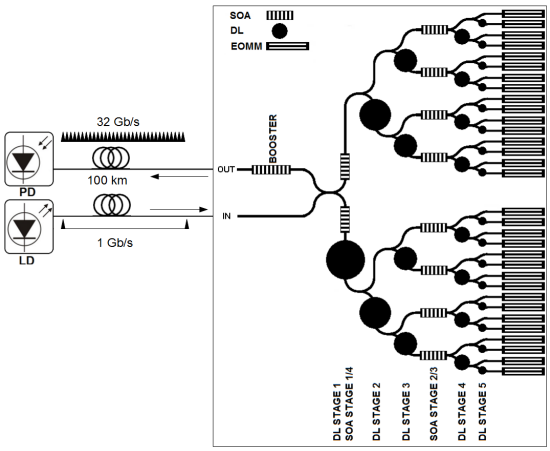

Figure 2: Schematic of the read-out system utilizing 32:1 integrated optical serializer

place hundreds of thousands of photomultipliers at the bottom of the Mediterranean Sea. They will be housed in optical modules (glass spheres), 31 photomultipliers in each. The output data from the photomultipliers has to be read out with a frequency of 333 MHz, the transmission bit-error rate (BER) should be kept below 10^{-9} and the power consumption inside a single module should not exceed 7 W. The concept of the readout system proposed for the KM3NeT detector by NIKHEF, the Dutch National Institute for Subatomic Physics, makes use of continuous wave lasers and receivers in the shore station, a fiber link with inline erbium-doped fiber amplifiers between the station and optical modules, a reflective electro-absorption modulator and an electrical serializer inside an optical module [4]. The modification we propose is to replace the electrical serializer with a photonic integrated circuit, simultaneously increasing the sampling frequency up to 1 GHz and keeping the BER coefficient unchanged.

The novel idea makes use of a fiber link between the shore station and the ASPIC assembled inside the optical module. One of the fibers will be used for downstream while the other one is used for the upstream data, and the ASPIC will perform the front-end readout. Figure 2 presents the schematic of the proposed system. An optical pulse train with a 1 GHz repetition rate and time duration of pulses of 30 ps is transmitted from the shore station to the ASPIC. Inside the ASPIC the signal is split by five stages of 3-dB power splitters among 32 waveguide channels. Simultaneously it is gradually delayed by five stages of optical delay lines. At the end of the circuit there are 32 Michelson amplitude modulators in a reflecting configuration. Assuming all modulators are in "on" state, the pulses are reflected and propagate back through the very same splitting and delaying network. The modulators are on-off driven by the digital data coming from the photomultipliers. As a result, the pulses appear at the output of the circuit, serialized one after another with a properly designed delay. Semiconductor optical amplifiers (SOAs) are used to compensate the splitting and component losses, as well as attenuation of the signal in the waveguides. Finally, the multiplexed signal exits the chip and goes back through the second fiber to the shore station, where it is detected and analyzed.

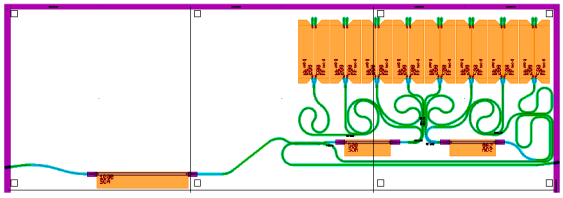

Figure 3: Mask layout of the 8:1 serializer chip

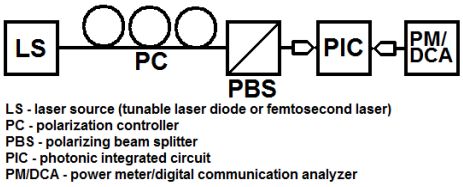

Figure 4: Schematic of the measurement setup

The system presented in Figure 2 is for 32 data channels. However, as a proof-of-concept, an 8-channel integrated optical serializer has been designed and fabricated in an MPW run at Oclaro. The circuit has been designed in a compliance with the EuroPIC generic packaging scheme proposed by CIP Photonics. The total size of the chip is 2×6 mm^2, which can be reduced to 2×3.5 mm^2 when the input and output are positioned on the same side of the chip. Positioning of the input and output on separate sides was done for making the characterization of the unpackaged chip easier. Figure 3 presents the designed mask layout of the ASPIC.

4. Measurement results

The characterization of the fabricated chips has been performed at the Optical Measurement Laboratory of the COBRA Research Institute. The schematic of the measurement setup is shown in Figure 4.

The time domain response of the 8:1 serializer circuit has been measured by launching light from a pulse laser source (150 ps time duration of the pulses, 80 MHz repetition rate, $\lambda_c = 1550$ nm) into the chip and measuring the outgoing signal with a digital communication analyzer (DCA). Figure 5 presents the time traces, when all of the SOAs are biased and all of the channels are activated. From the measurement it is not possible to extract the exact delay between the adjacent channels, due to the limited bandwidth of the DCA (30 GHz) resulting in the broadening of the pulses. However, from the coarse estimation it is 32-33 ps which is slightly larger than the design value of 31.25 ps. The experimental results show that the device works as intended.

The SOA gain has been optimized by tuning the injection current so that the pulses of the first and fifth channels have the same power. However, the power of the pulses depends as well on the transmission of the Michelson modulators. Even though during the measurement no

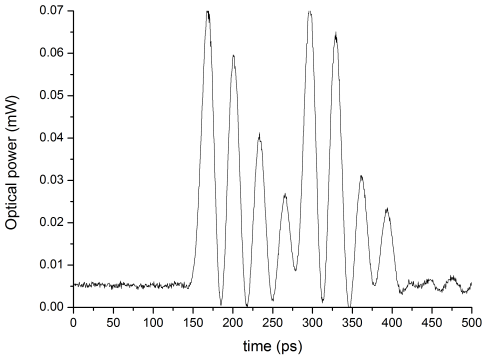

Figure 5: Pulse response of the 8:1 serializer circuit

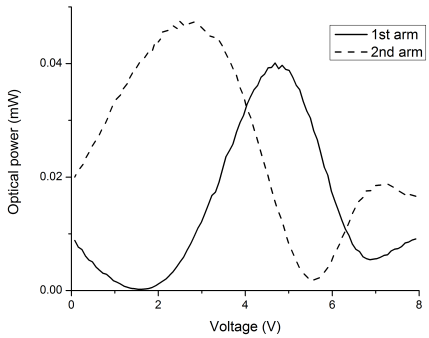

Figure 6: Transmission characteristic of the Michelson modulator

voltage has been applied to the modulators, the transmission is not uniform for all of the channels. In spite of the fully symmetric structure, there is an asymmetry in the transmission characteristics of the modulators. Figure 6 presents an example of such a characteristic while driving independently the two interferometer arms, measured for the same type of modulators on a different chip. We believe that the asymmetry is the effect of unwanted excitation of higher order waveguide modes, which results in the asymmetric power split by the 3-dB power splitter. The measured extinction ratio is good, 23 dB and modulation voltage $v_\pi = 3$ V.

To observe the performance of the circuit when one of the channels is modulated, we coupled light from the pulse laser and drove one of the modulator arms with an increasing voltage. Figure 7 shows time traces, when only two SOAs, the booster and one of the inline amplifiers, are activated and the second inline amplifier is off. We have performed the measurement for a reverse bias voltage applied to the modulators ranging from 0 V up to 6 V with a 0.5 V step. The figure presents the output signal when the first channel is modulated. The results prove that it is possible to modulate one of the channels while not affecting the others. The extinction of the pulses is not complete, due to the broad wavelength spectrum of the input femtosecond laser signal. The value of the phase shift in the electro-optical modulators is wavelength dependent so it is different for each wavelength component. This results in non-complete destructive interference at the output of the modulator.

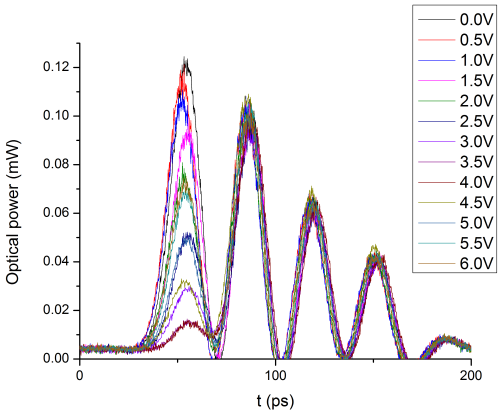

Figure 7: Independent modulation of the first channel

5. Summary and conclusions

We have designed an integrated optical serializer in a generic technology approach. The chips have been fabricated together with other devices in a multi-project wafer run in an InP foundry.

Time domain multiplexing of independent data channels is observed as a result of the power split of the input signal and increasing delay applied to the consecutive channels. The output bit-rate is as high as 32 Gb/s. We have also shown the possibility of modulation of each of the channels independently. The extinction ratio of the modulators is good, exceeding 20 dB and the low driving voltage enables high-frequency modulation. In the coming months the serializer will be characterized in terms of digital transmission parameters, such as BER coefficient and eye-diagrams. Altogether, the first characterization results of the 8:1 serializer chip look promising and show good performance of the devices. We believe, that such a circuit could find its applications in data readout systems of newly designed physics experiments where there is a need of transmission of a huge amount of data to a central station.

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