A large surface photomultiplier based on SiPMs

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Abstract

Light detection through photosensitive devices represents one of the key issues for a large variety of experiments.
In the recent years, Silicon PhotoMultipliers (SiPMs) based on limited Geiger-mode avalanche have been extensively studied in view of their future applications. However, their use is strongly limited by their small sensitive surfaces and by the fact that any increment in the surface turns out into an increase of the dark count rate.
In the present work we describe the dark count rate reduction obtained by using a FPGA-based logical circuit for fast pre-processing of pulses from a 3×3 matrix of SiPMs. The prototype we developed supports two SiPMs: we show that a rate reduction from 6.6 Mcps (Mega counts per second) down to 0.436 Mcps at the lowest threshold (0.5 photon-equivalent) and from 1.2 kcps down to 0.02 cps for the highest threshold (3.5 photon-equivalent) is obtainable.

1. INTRODUCTION

Photon detectors play a crucial role in many areas of fundamental physics research, such as particle astrophysics and nuclear physics. Indeed, most of future experiments aimed at the study of very high-energy (Gamma-Ray Bursts (GRB), Active Galactic Nuclei (AGN), Super-Novae Remnants (SNR)) or extremely rare phenomena are based on photon detection [1-5]. The requirement of higher sensitivities will call for detectors whose size should greatly exceed the dimensions of the largest current installations. To date, in this kind of experiments the photon detection capabilities of the PhotoMultiplier Tubes (PMTs) seem to be unrivalled. However they suffer of the following drawbacks:

- fluctuations in the first dynode gain make single photon counting difficult;
- the linearity is strongly related to the gain, in particular it decreases as the latter increases;
- the transit time spreads over large fluctuations;
- the mechanical structure is complex and expensive;
- they are sensitive to magnetic fields;
- the need of voltage dividers increases failure risks, complexity in the design and power consumption.

In the past years alternatives to PMTs, mainly based on solid-state detectors, have been pursued. After about one century of standard technology (photocathode and dynode electron multiplication chain) the recent strong developments of modern silicon devices have the potential to boost a new generation of photodetectors, based on an innovative inverse pn junction: PN or PIN photodiodes, Avalanche PhotoDiodes (APDs) and avalanche photodiodes in Geiger-Mode (GM-APDs)[6-13]. These solid-state devices show important advantages over PMTs, namely:

- higher quantum efficiency;
- lower operating voltages;
- insensitivity to magnetic fields;
- robustness and compactness.

The step-by-step evolution of solid state photon detectors has been mainly determined by their internal gain: a PIN has no gain, an APD can reach a gain of few hundreds, while the GM-APD has a gain comparable with that of PMTs; this would allow GM-APDs to achieve single-photon detection. In recent years have become commercially available some devices made of arrays of GM-APD cells (pixels) connected in parallel, sometimes under the name of SiPM or Multi Pixel Photon Counter (MPPC by Hamamatsu). If the number of fired pixels is below 13-15% of the total, the output signal depends linearly on the number of fired cells, i.e. directly on the number of detected photons.
Unfortunately SiPMs have small sensitive surfaces (currently between 1 and 9 mm^2) and high dark count rates (tens of kcps up to few Mcps for 3×3 mm^2). A solution to increase the SiPM field of view could be the use of optical concentrators with adequate refraction index, characteristics and geometry [14]. However, due to optical and geometrical limits, a single SiPM+light concentrator

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system cannot reach a large detection surface: calculations and measurements show that the detection surface could be reasonably increased only by a factor four [14].

A 3×3 matrix of SiPMs equipped with light concentrators and including a digital circuit for fast data processing has been designed. The goal was to find a simple and efficient way to significantly increase the sensitive surface. The circuit, based on a FPGA (Field Programmable Gate Array) logic, is able to process information previously digitized by an ADC and to sum the contributions of all photon detections. A digital discriminator with variable threshold has been embedded into the logic on each channel for dark count reduction.

2. DIGITAL CIRCUIT DEVELOPMENT

The circuit consists of an array of ADCs that digitizes the amplified and conditioned signals coming from the matrix of SiPMs. Amplification and conditioning are obtained through a National Semiconductor LMH6624 ultra low noise, wideband Op-Amp (figure 1). It is important to remind that the whole matrix of pixels is internally parallelized: in our case this means that physically 14,400 pixels are put together giving their signals to the above-mentioned amplifier [15]. Digitized data are sent to the FPGA logic (figure 2). Due to the characteristics of the amplified signals (rise time$\sim$ 5 ns, FWHM$\sim$ 20 ns) and to the ADC sampling frequency (200 MHz), at least four samples are generated for each detected signal. As the signal goes under threshold, the FPGA takes the maximum of the samples. The number of photoelectrons for the acquired level is determined using a look-up table. Figure 3 shows the scheme of the circuit.

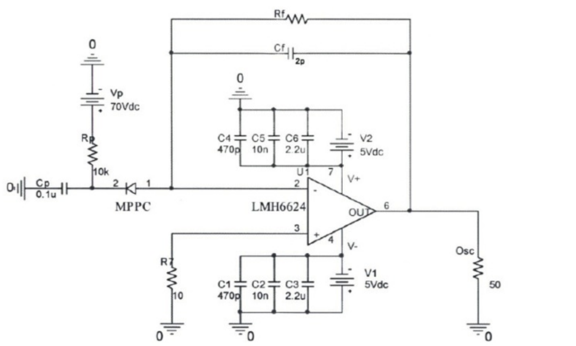

Figure 1: Scheme of the amplifier circuit based on the LMH6624 Op-Amp.

The embedded discriminator eliminates the samples corresponding to signals under threshold, mainly due to dark counts. Then, the circuit performs a coincidence between samples coming from the two channels. Since the typical duration of the amplified signals has a FWHM of 20 ns the coincidence window is set to 40 ns. The first

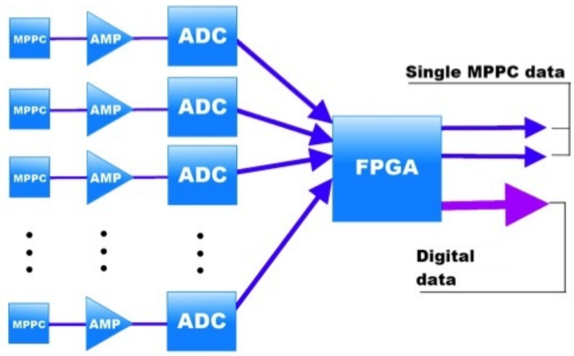

Figure 2: Scheme of the SiPM matrix equipped with the FPGA logic.

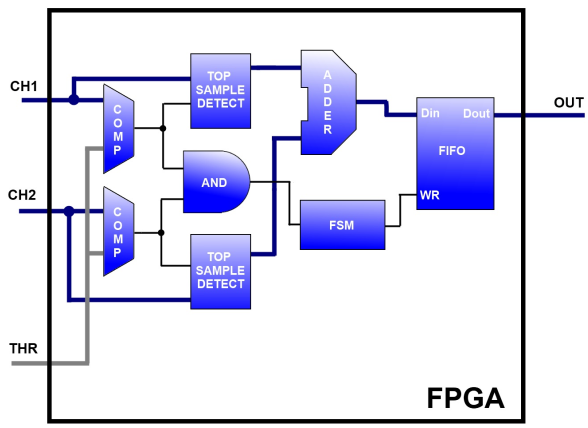

Figure 3: Simplified scheme of the FPGA built in circuit.

prototype has only two input channels (two SiPMs) but this approach can be generalized to the final version containing 9 (3×3) SiPMs. Indeed, the 3×3 matrix will be simply treated by considering all the possible 1-to-1 coincidences (for commutation without repetition it is equal to $9\times8/2$=36 pairs). The outputs from the 36 coincidences will be added together into the FPGA. Starting from this principle the calculation of the expected dark count rates is easy: it is just equal to 36 times the dark count rate for the single pair coincidence.

A Finite State Machine (FSM) is used to control the writing process of data into the FIFO. The prototypal simplified 2×1 matrix is represented in figure 3. The logic reads data from the individual SiPMs and sums samples from both channels at the same time. The availability of data from the single SiPMs allows for checking for possible SiPM or amplifier malfunctioning and/or for any ADC failure.

3. IMPLEMENTATION ON FPGA

As stated, the first prototype has been developed only on two input channels (two SiPMs), using an FPGA evaluation board by AGE Scientific. The circuit scheme is shown in figure 4. It has two differential amplifiers that convert the input signals into two differential signals. The ADC is a KAD5612P by Kennet, a dual channel pipelined architecture with 250 MHz maximum sampling frequency [16]. The FPGA is a Spartan 3E by Xilinx [17], supported by an USB controller (Cypress CY7C68013A) [18] for communication with the PC. Figure 5 shows the evaluation board.

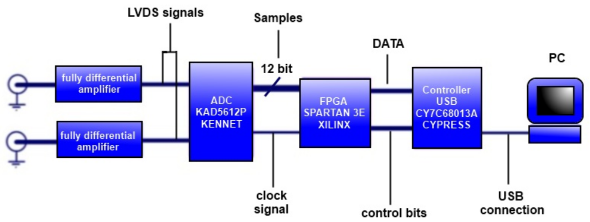

Figure 4: Evaluation board scheme and USB connection.

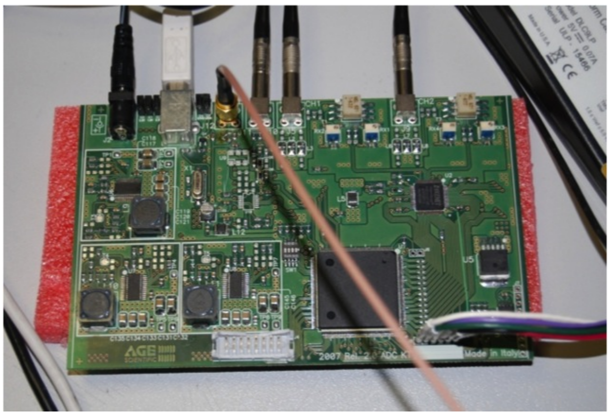

Figure 5: Evaluation board used for this work.

Due to the ADC conversion time (the Latency is of 7.5 clock cycles as from the data-sheet) and to the process time of the logic (Latency = 5 clock cycles) data are available after 65 ns (13 clock cycles @ 200 MHz). In order to verify the proper functioning of each component, several simulations of the circuit have been performed using ModelSim software (by Mentor Graphics). After all logical behavioral simulations, we performed timing simulations of the circuit in order to verify the correct timing of the whole system. The FPGA has been finally configured and the system has been tested. We connected the two SiPMs to the system and we found a dark count rate in accordance with the expected value of $rate1 \times rate2 \times (2 \times GateTime)$. We also calculated the reduction factor (RF), defined as:

$$RF = \frac{rate1 + rate2}{rate1 \times rate2 \times (2 \times GateTime)} \quad (1)$$

4. CONCLUSIONS

After verifying that a simple 2×1 matrix works according to our expectations, we are realizing a 3×3 matrix of SiPMs with 9 ADC modules. In parallel, we are designing the FPGA circuit required to process data from 9 modules.

This new detector will have a total sensitive area of $22.5 \times 22.5\ mm^2$ and a low dark count rate (~ 10 cps for each pair with a threshold of 2.5 p.e. @ 22°C). The exploited light concentrators have an input surface of $7.5 \times 7.5\ mm^2$, an output surface of $2.5 \times 2.5\ mm^2$ and a length of 50 mm. One SiPM equipped with the light concentrator described above is shown in Figure 6.

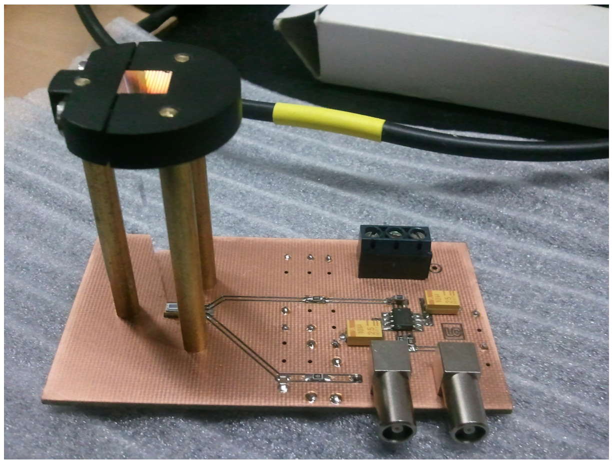

Figure 6: Picture of one SiPM equipped with a light concentrator. It is also possible to see the amplifier circuit.

In order to further enhance the sensitive surface and finally to realize a new complete detector, 3×3 SiPM matrices can be arranged together by using several FPGA circuits. The results obtained for the prototype, based on a single pair of SiPMs, are extremely significant to assess the final performances of the 3×3 version. Therefore, due to the repeatability of the effect, any detector made of N single pairs of SiPMs will have a performance that is simply the multiplication by N of the results obtained for the prototype.

Finally, we want to make some considerations about the temperature dependence of the effect. We have made several dark count rate measurements on a $3 \times 3\ mm^2$ SiPM (S10931-025P MPPC by Hamamatsu, containing 14,400 sensitive pixels): at 22 degrees Celsius we measured the reduction factors (for one SiPM pair) shown in table 1.

The dark count rate decreases almost linearly with the temperature: in particular it decreases of a factor 2 as the

Threshold set	Dark Counts reduction factor
0.5 p.e.	15 (from 6.6 Mcps to 435 kcps)
1.5 p.e.	172 (from 580 kcps to 3.4 kcps)
2.5 p.e.	3125 (from 32kcps to 10 cps)
3.5 p.e.	75000 (from 1.2 kcps to 0.02 cps)

Table 1: Dark count rate reduction factor for different thresholds at T=22°C.

temperature decreases of 8°C, so at 14°C the dark count rate halves and the reduction factor doubles. The last data could be very interesting, for example, to develop underwater Cherenkov detectors using photomultiplier systems based on SiPMs.

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