FPGA Shore Station demonstrator for KM3NeT

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For the KM3NeT consortium

Abstract

The KM3NeT readout concept is based on a point-to-point optical network connecting the ten thousand optical modules in the deep-sea neutrino telescope with the shore station. The numerous fibre optic channels arriving at the shore station will be concentrated on the shore electronics systems, which will receive, merge and time order the data, and send them to the DAQ system. Although the network functionality is bi-directional, the physical channel allocation is asymmetric; most channels are assigned to the data reception and only a few channels are used for control with data transport from shore to the telescope. We will discuss the FPGA based platform systems for the shore station and the appropriate firmware implementation for the data gathering and broadcast demands of a neutrino telescope. We will present our experiences based on FPGA evaluation platforms suitable to build a demonstrator of the KM3NeT shore station.

Keywords: Neutrino Telescope, DAQ, FPGA architecture

1. Introduction

The main objective of the KM3NeT collaboration [1] is the design, construction and operation of a deep-sea research infrastructure in the Mediterranean Sea including a very large volume Neutrino Telescope using Cherenkov light detectors. Those detectors, the Digital Optical Modules (DOM), [2] are constructed with Photomultiplier tubes inside a pressure resistant glass sphere housing, along with a hydrophone, an inclinometer, a compass and a LED beacon. A power converter board, for the power, and the central logic board [3] and readout system of each DOM is also included. When immersed in the deep-sea, the ten-thousand DOMs will be operated and their digitized data will be transmitted to the shore station on land.

The control and readout of all DOMs from the shore station will be realised through an asymmetric wavelength photonic network downstream and upstream data transmission [4] based on the implementation of Gbit Ethernet with TCP/IP protocol. Earlier studies [5], [6] have highlighted the use of general purpose FPGA systems in the KM3NeT and its shore station.

In this paper, we describe the KM3NeT shore station electronics requirements and present the design for the tasks of Data Gathering and Data Broadcasting with an on-shore FPGA prototype system. First tests with this design are also reported.

Section 2 describes the KM3NeT Readout Scheme and the on-shore system requirements and section 3 presents the Shore Station Scheme and analyses the FPGA architecture. Section 4 shows the implementation and testsbench results while section 5 concludes the paper.

2. KM3NeT Readout Scheme

Figure 1 depicts the overall readout scheme. The submarine infrastructure consists of numerous vertical structures that suspend the Digital Optical Modules in the water column, connected to a number of Secondary with interlink electro-optical cables. The Secondary Junction boxes are connected to a primary junction box; the latter being connected to the shore station with a long multifibre electro-optical cable.

The link between each DOM with the shore station is established by utilizing an optical network that is based on DWDM technology. All DOMs digitized data are send to the shore with an expected rate greater than 100 Gbps. As a result, real time processing is necessary in order to store only the data of interest at a few Gbps.

Although the network functionality is bi-directional, the physical channel allocation is not symmetric. The bulk of the data are sent from the deep-sea to shore, whereas only a small data flow is required to be send from the shore to the deep-sea for control, calibration and operational commands. Therefore, for the upstream link, a point-to-point link is realised by assigning a unique wavelength for each DOM for the transmission of data to the shore. For the downstream link however, a single wavelength is used to communicate with multiple DOMs. This asymmetry

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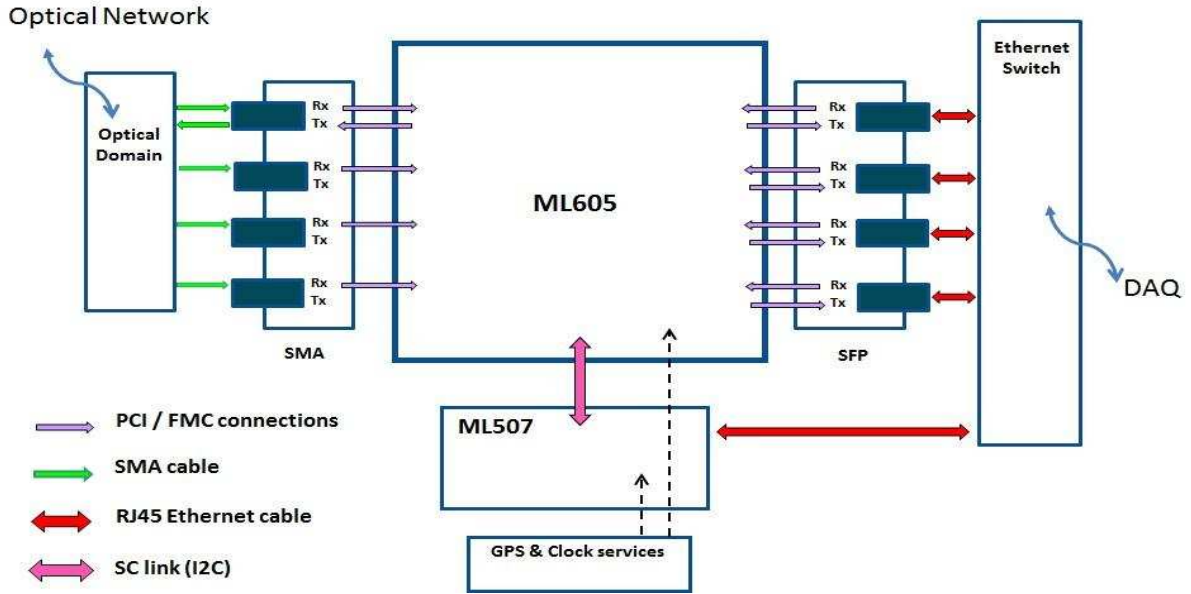Email address: kmanolo@phys.uoa.gr (K. Manolopoulos).

Figure 2: Shore station functional diagram

requires an intervention at the link-level layer to ensure that all broadcasting data reach the DOMs.
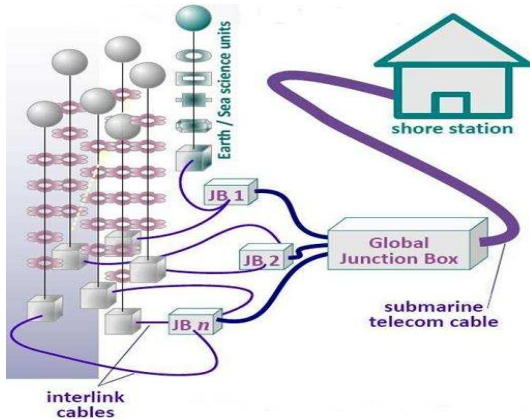

Figure 1: The overall readout scheme

2.1. On-shore requirements for the KM3NeT demonstrator

The KM3NeT demonstrator is a small scale prototype realisation that consists of 4 Digital Optical Modules (DOMs). Each DOM converts its measurements to digitized data, then embeds them in an Ethernet frame and transmits that frame to the shore station. The shore station receives the incoming data, performs merging and time ordering and sends them to the Data Acquisition system (DAQ). At the same time it will have to transmit all the necessary commands to the optical modules.

Specifically, the main functions of the readout electronics on shore are the following:

1. Establish an Ethernet point-to-point data reception: each DOM utilizes a dedicated link to transmit Ethernet frames to the shore station.
2. Broadcasting control data distribution: a single link is used to broadcast data from the shore station to all DOMs.
3. Distribute the experiment clock and synchronous commands to all DOMs.
4. Perform calibration and time measurements of each DOM over the optical network.
5. Use a central GPS reference clock.

3. FPGA system On-shore prototype

The shore station scheme of the KM3NeT demonstrator consists of two FPGA platforms, the Xilinx ML605 [7] and Xilinx ML507 [8] Evaluation boards, a GPS clock unit [9] and a standard Gbit Ethernet switch.

Figure 2 presents a functionality diagram of the shore station. The Xilinx ML605 evaluation board has a fundamental importance in the entire scheme, since it handles all the incoming and outgoing data traffic, and it performs the main functions that were mentioned in the previous section.

The left side of the ML605 board, as shown in figure 2, represents the connection to the optical network, using SMA connectors. Each SMA connection serve a unique channel that connects a particular DOM with the shore station; all four channels transport data from the optical modules to the shore while one channel is used also bi-directionally to transfer data from the shore to the DOMs. Hence, in the ML605 that specific channel has both the Rx

and Tx parts enabled, while the rest of the channels utilize only the Rx part.

At the right side of the ML605 board, we use SFP connectors to connect the board through an Ethernet switch, to the DAQ system. Since all SFP connections are bidirectional, we use a typical RJ45 Ethernet cable.

The Xilinx ML507 evaluation board is connected with the ML605 board, through an *I2C* link for control and monitoring using the DAQ software framework. The ML507 board contains a Virtex-5 FPGA that includes an embedded processor. The latter is used to run the DAQ software on a PPC core under the VxWorks OS.

Finally, an external GPS receiver is utilized to provide a reference clock for the entire system.

3.1. FPGA architecture

The Xilinx ML605 evaluation board includes a Virtex 6 FPGA. Figure 3 depicts the block diagram of the FPGA architecture that we develop for KM3NeT.

The black arrows at the right and left side of the picture represent the incoming and outgoing ports of the board. The left side arrows correspond to the connections with the optical network and the DOMs, as described above, while the right side arrows represent the connections of the ML605 to the Gbit Ethernet switch. As mentioned previously, all the right-side connections are bidirectional in order to achieve the simultaneous transfer of data to-and-from the shore station, while, the left side, all four connections are used to transfer data from the DOMs to the shore station; only one link is bidirectional (upper left corner of the picture) in order to broadcast also data from the shore to the DOMs.

Each ports utilizes a GTX gigabit transceiver [10] and an Tri-Mode Ethernet MAC (TEMAC) core [10]. The Virtex-6 FPGA GTX transceiver is a highly configurable Serializer/Deserializer (SerDes) integrated with the programmable resources of the FPGA. The GTX transceiver can operate at line rates up to 6.6 Gb/s and it includes features such as 8B/10B encoding, comma alignment, channel bonding and clock correction. The Tri-Mode Ethernet MAC core is a Xilinx core used in designs that require Ethernet connectivity; it is designed according to the IEEE Std 802.3-2005 specification, providing a fully integrated 10/100/1000 Mb/s Ethernet MAC. Moreover, it includes a 1000BASE-X Physical Coding Sublayer (PCS) and a Physical Medium Attachment (PMA) sublayer that is used with the Virtex-6 serial transceivers to provide a complete on-chip 1000BASE-X implementation.

In order to broadcast data from the shore station to the DOMs, we send an Ethernet frame through the switch to one of the 4 right-side ports. The frame passes through the GTX transceiver and enters the TEMAC core. Each TEMAC core has been assigned a unique MAC address which corresponds to a specific DOM. The core performs address filtering to any incoming frame by checking if the destination MAC address of the frame matches the assigned one. If the address match, then the frame is allowed to proceed, else it is dropped. Thus, we reduce the broadcasting traffic and ensure that only valid frames will reach the DOMs. Finally, the core asserts the frames' quality and sends it to be stored into a buffer.

When multiple frames enter the board in parallel, they are stored temporarily into buffers to be transmitted successively using a multiplexer. A control unit, handling the select signal of the multiplexer and the read operations of the buffers, ensures that all frames will be broadcasted.

Next, the selected frame enters the left-side corresponding TEMAC core, which prepares the frame transmission to the DOM. Before passing the frame to the left-side GTX transceiver, to exit the board and enter the optical network, the *Clock and Command Insertion* [11], [12] takes place.

The *Clock and Command Insertion* module intervenes between the TEMAC core and the GTX transceiver and inserts into the frame the system clock and any necessary commands. When the frame reaches the DOM, the system clock will be used as an operational clock by the off-shore electronics, the commands will be read and executed accordingly and, finally, the clock will be send back again to the shore station in order to perform phase measurement and to establish the round-trip time delay.

The presented design, in parallel with the data broadcasting, performs also data reception. The 4 left-side ports of figure 3 receive continuously data from the DOMs of the KM3NeT demonstrator. The incoming frames follow a path similar to the one described above; a frame will enter the GTX transceiver, the *Clock and Command Insertion* module will extract the commands and the clock that was sent back from the DOMs and then proceeds to the TEMAC core and continues its route uninterrupted leaving the board and reaching the DAQ system.

4. Implementation analysis and test-bench results

The presented design has been implemented in VHDL using the Xilinx 13.1 software tool. Timing simulation analysis was initially performed to ensure the designs' functionality. Then the design was tested at a hardware level using the ML605 board and an additional FMC card that provided us with the additional SFP cages (Fig. 4). These tests were performed using only the first two points of connectivity (the two upper ports of each side of figure 3). Instead of using the actual optical network, each left-side port was connected to a computer with a gigabit Ethernet card. Ethernet frames were send from both sides to the board and, using a software tool for Ethernet packet inspection [13], we were able to verify that all frames arrived to their destination successfully.

5. Conclusions

An FPGA based platform system for the KM3NeT demonstrator has been produced and tested. The systems'
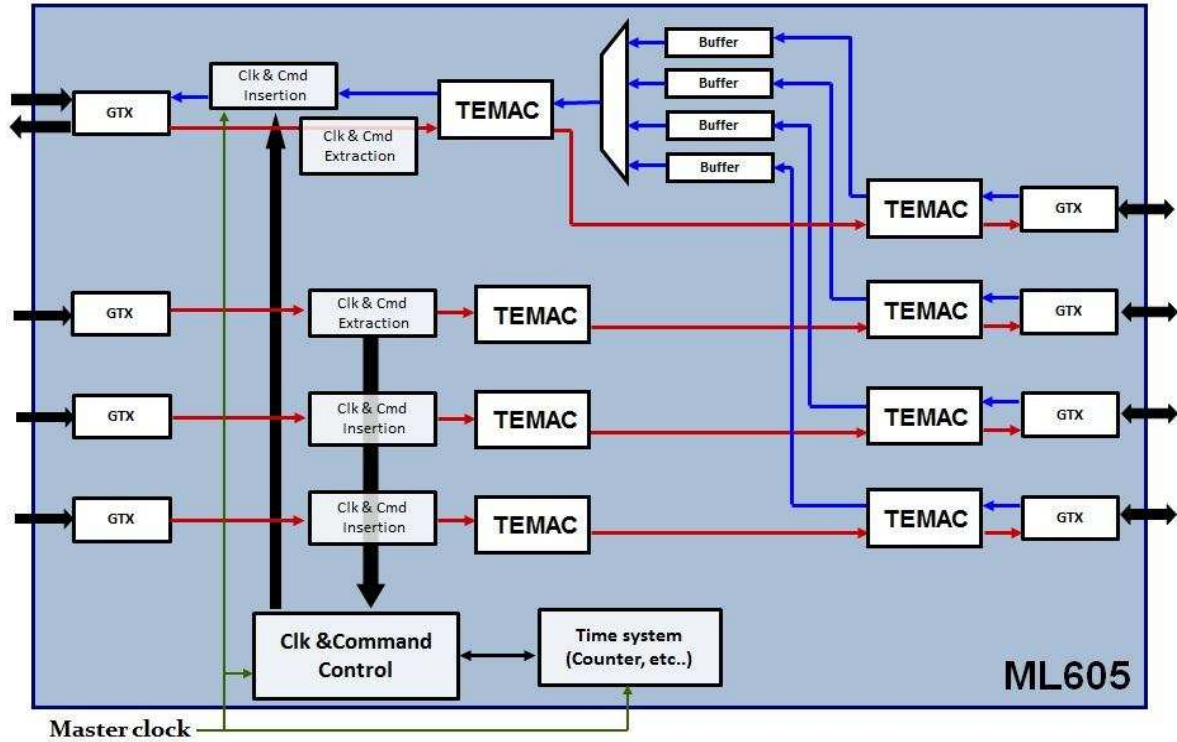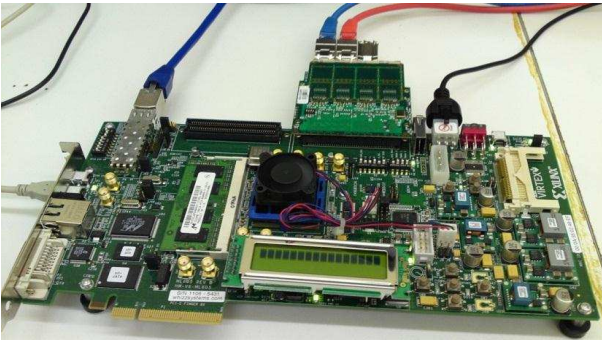
Figure 3: The ML605 block diagram

Figure 4: The ML605 evaluation platform

functionality is based on utilizing two Xilinx evaluation boards; the ML605, to manage the data traffic and, the ML507, for control and monitoring. The effort is ongoing to expand the data gathering and broadcasting design to support multiple DOMs with the same ML605 board. In addition, tests will be conducted to emulate the optical broadcast using physical link-level splitters. The tests reported so far, show that the design is adequate to meet the requirements for the KM3NeT demonstrator.

6. Acknowledgements

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