DRD7.6a – Update September 2024

Marlon Barbero, Jerome Baudot, Manuel Rolo, Iain Sedgwick, Walter Snoeys

ECFA
European Committee for Future Accelerators

DRD7.6

Project Name	Common Access to Selected Imaging Technologies (WP7.6a)
Project Description	Provide common access and centralized support for selected CMOS imaging technologies, including specific IP development to accelerate the design effort. Duration 3 years, expected to be extended.
Innovative/strategic vision	Potential of monolithic technologies, confirmed by successful ALICE ITS2 tracker and the widespread community interest. Efficient and affordable technology access requires concentration of the resources in the community.
Performance Target	Organize common runs and efficient and cost-effective access to selected technologies.
Multi-disciplinary, cross-WP content	Concerns several detectors types, calorimeters, tracking, etc. Serves other DRDs like DRD3 and DRD6, experiments and projects in HEP. Strong connection with 7.6b (e.g. 3D integration of chiplets). Requires expertise in analog and digital IC design, device design and technology, and significant testing effort.
Contributors	CH: CERN FR: IN2P3: CPPM, IPHC, IP2I + others IT: INFN(TO, TIFPA, MI, BO, PD, PV, PG, PI) NL: NIKHEF NO: UiB, UiO and USN UK: STFC US: TBC, SLAC already doing effort

Technologies targeted initially: TPSCo 65nm ISC, TJ 180nm, LF 110nm IS

TPSCo 65nm

Marlon Barbero, Jerome Baudot, Manuel Rolo, Iain Sedgwick, Walter Snoeys

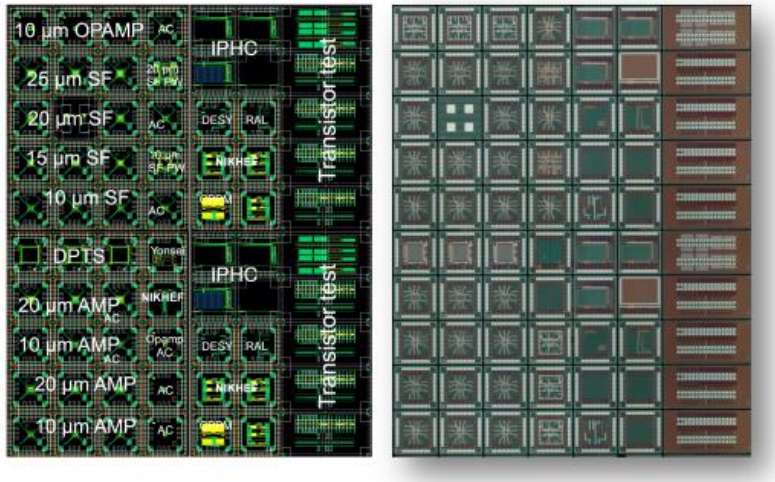
TPSCo 65nm ISC

In parallel with the design of the MOSAIX, work applicable to DRD7.6a is being done in collaboration with ALICE but also with other groups

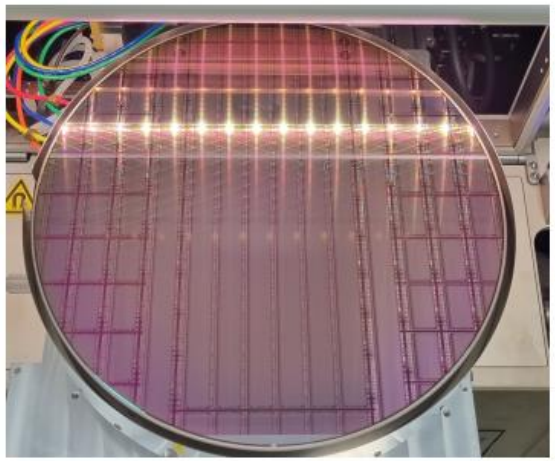
- Technology has been qualified for high energy physics after first run (MLR1)
- Stitching has been studied on a second run (ER1)

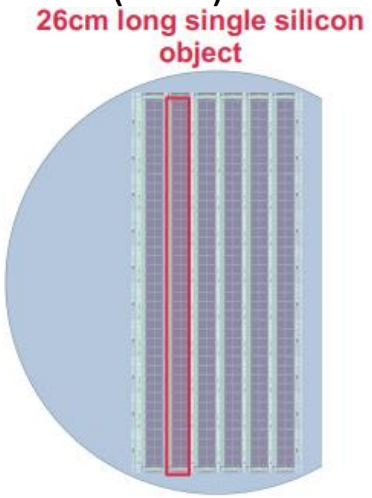
Technology Developments

- New PDK has been acquired with a new metal stack allowing lower supply voltage drops.
- Custom design rules for high yield design in stitched sensors developed.
- Further process optimisation is being carried out to improve sensor radiation tolerance (NIEL)



MLR1





ER1

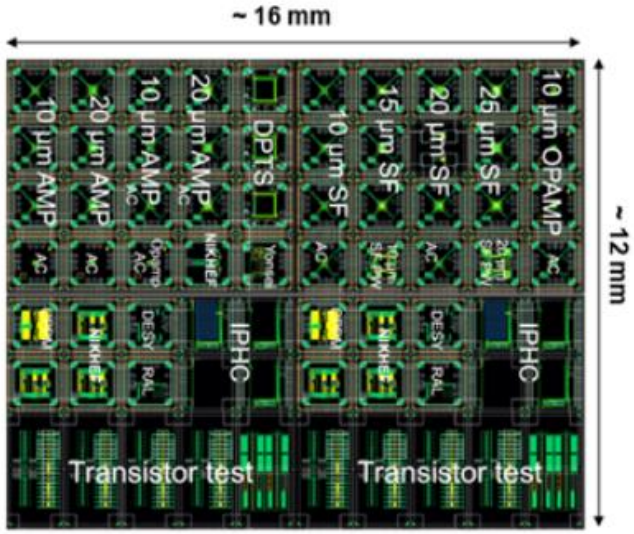
DRD7.6

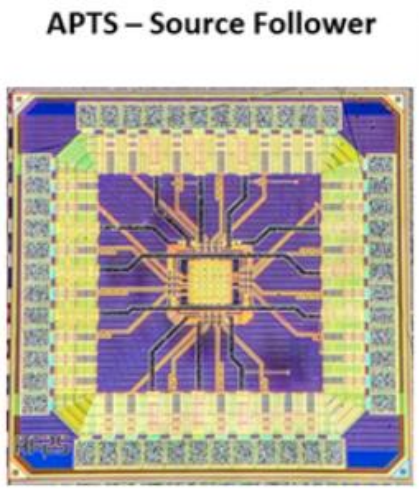
TPSCo 65nm ISC

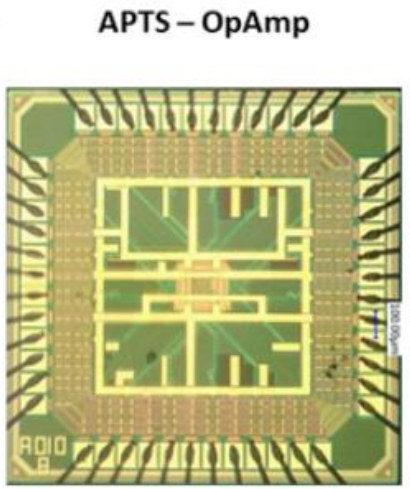
IP Developments
Several blocks under development, either directly integrated in the MOSAIX, included in test chips, or both.

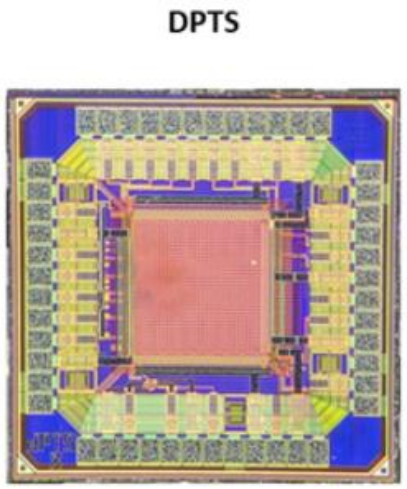
- Logic libraries for DFM and in-pixel logic.
- Bandgap and Temperature Sensor
- LDOs (used in serialiser)
- High speed transmission unit with serialiser
- Monitoring ADCs
- Biasing DACs
- Long distance (~10 cm or more) on-chip data transmission.
- TDCs

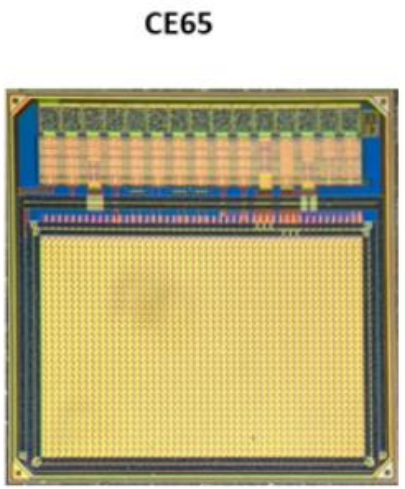
New groups have expressed interest in joining. Framework for signing NDA well established. Work still to be done on legal aspects of IP sharing.







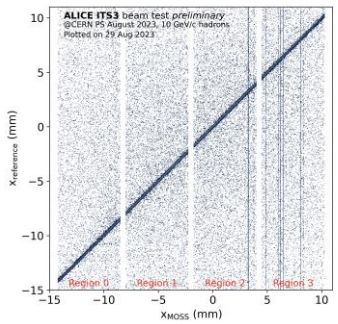


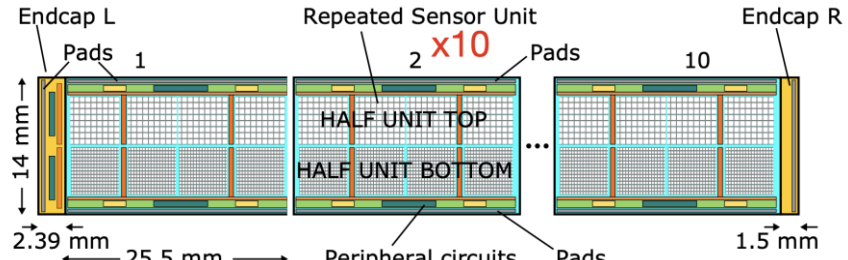


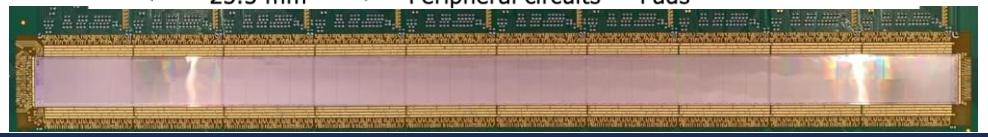
DRD7.6 Stitched sensors in ER1

MOSS (25.9 cm x 1.4 cm)

- 10 repeated sensor units:
  - top half at 22.5 um pitch and bottom half at 18 um pitch,
  - each half powered completely independently with 4 conservatively designed submatrices -> many power domains
  - synchronous readout
- First operation in beam in August (D. Colella TIPP2023)
- Detection efficiencies and fake hit rates (M. Mager HSTD 2023)
- Intense effort on performance and yield characterization

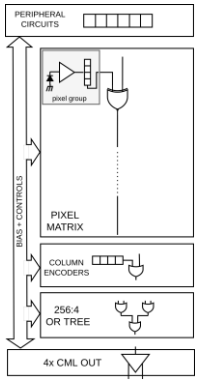


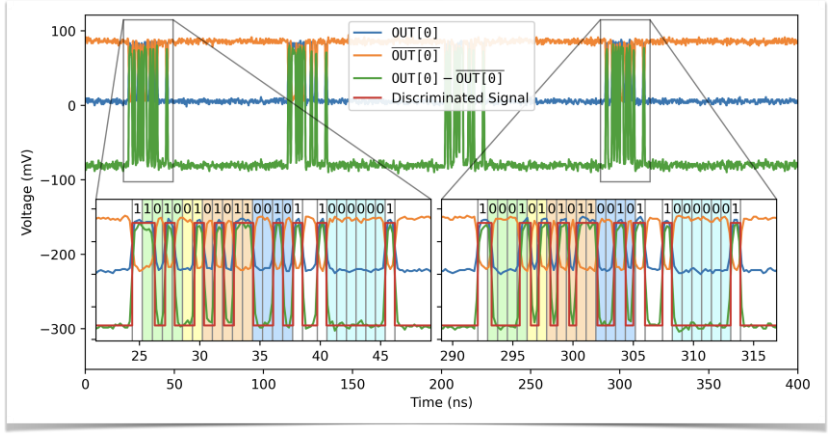




MOST (25.9 cm x 0.25 cm)

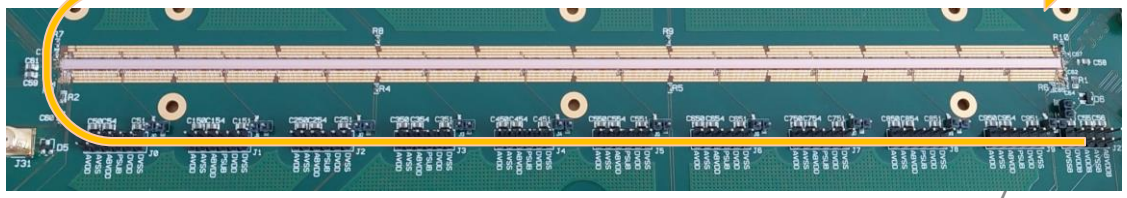
- 10 repeated sensor units:
  - 18 um pitch, very densely designed pixel matrix
  - Global power distribution + conservatively designed highly granular power switches to switch off faulty parts
  - Asynchronous, hit-driven readout, low power consumption + timing
- Basic functionality established, detailed characterization ongoing.
- Pulsing signal and output signals at the end of the chip, round trip more than 50 cm, ~ 200 ns, with ~800 repeaters, all 256 signal lines functional.





(M. Mager HSTD 2023)

50 cm, ~ 300 ns



TPSCo 65nm ISC

Selected Publications and Presentations

TWEPP 2022

[Digital cells radiation hardness study of TPSCo 65nm ISC technology by designing a Ring Oscillator]
[Measurements of Total Ionizing Dose Effects and Influence of NMOS Bulk Bias on a CMOS Image Sensor process]
[Development of a Stitched Monolithic Pixel Sensor prototype (MOSS chip) towards the ITS3 upgrade of the ALICE Inner Tracking System] MOSAIX
[Design of an analog monolithic pixel sensor prototype in TPSCo 65 nm ISC CMOS imaging technology]
[Bandgap Reference, Temperature Sensor and Low Drop-out Regulator Circuits for Monolithic Sensors in TPSCo 65nm ISC Technology]
[A 65nm Dual Mode 1.25/7 GHz PLL with CML Line Driver for ALICE ITS3 and EIC Applications]

TWEPP 2023

[Prototype measurement results in a 65nm technology and TCAD simulations towards more radiation tolerant monolithic pixel sensors]
[SAQRADC: An on-demand, low-power, minimal footprint, 10-bit resolution charge-redistribution ADC with internal clock generation]
[The Monolithic Stitched Sensor (MOSS) Prototype for the ALICE ITS3 and First Test Results] MOSAIX
[Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3]
[NAPA-P1: NANOSECOND TIMING PIXEL FOR LARGE AREA SENSORS]
[Development of the data transmission architecture of the stitched sensor prototype towards the ALICE ITS3 upgrade]

More references can be found in EP-RD reports below:
https://cds.cern.ch/record/2808204
https://cds.cern.ch/record/2852748
https://cds.cern.ch/record/2891650

…and many more, with more to come!

TJ 180nm

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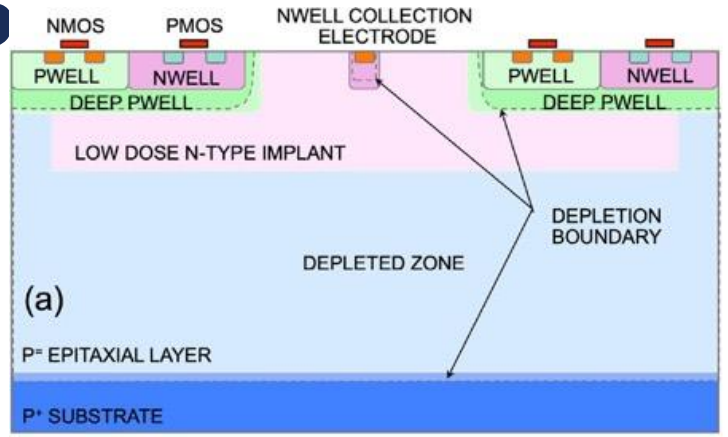
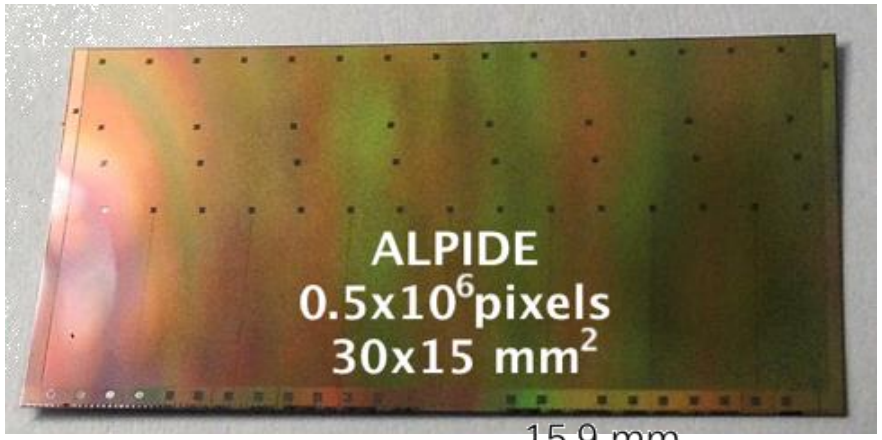
DRD7.6

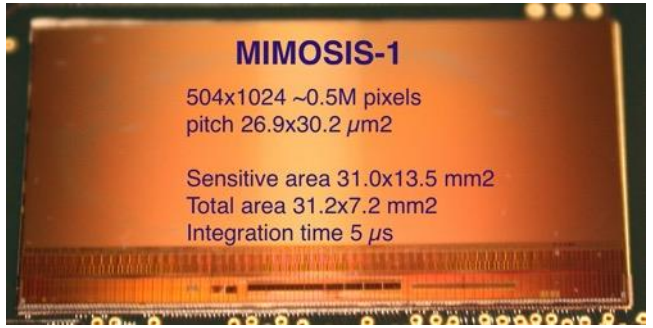


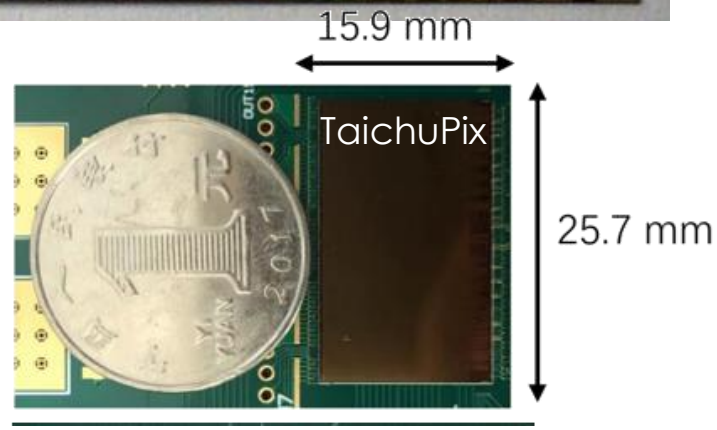
TJ 180nm Activities in DRD7.6a

- **Legacy of 10+ years of developments**
  - CMOS process: quadruple well, 7 metal layer stack
  - Sensitive layer: high-resistivity, variable thickness, process modifications
  - Small collection electrode implementation
  - Many contributors (review DOI:10.1016/j.nima.2023.168678)
    - Historic drivers: STFC, CERN, IPHC
    - Driven by tracking, calorimetry, X-ray imaging
  - Equip current largest MAPS-based tracker:
    ALICE-ITS2 with ALPIDE (DOI:10.1016/j.nima.2015.09.057)



- **Current experiment-based projects**
  - MIMOSIS for CBM micro-vertex det. (MVD)
  - OBELIX for Belle II upgrade
  - JadePix, TaichuPix for CEPC project



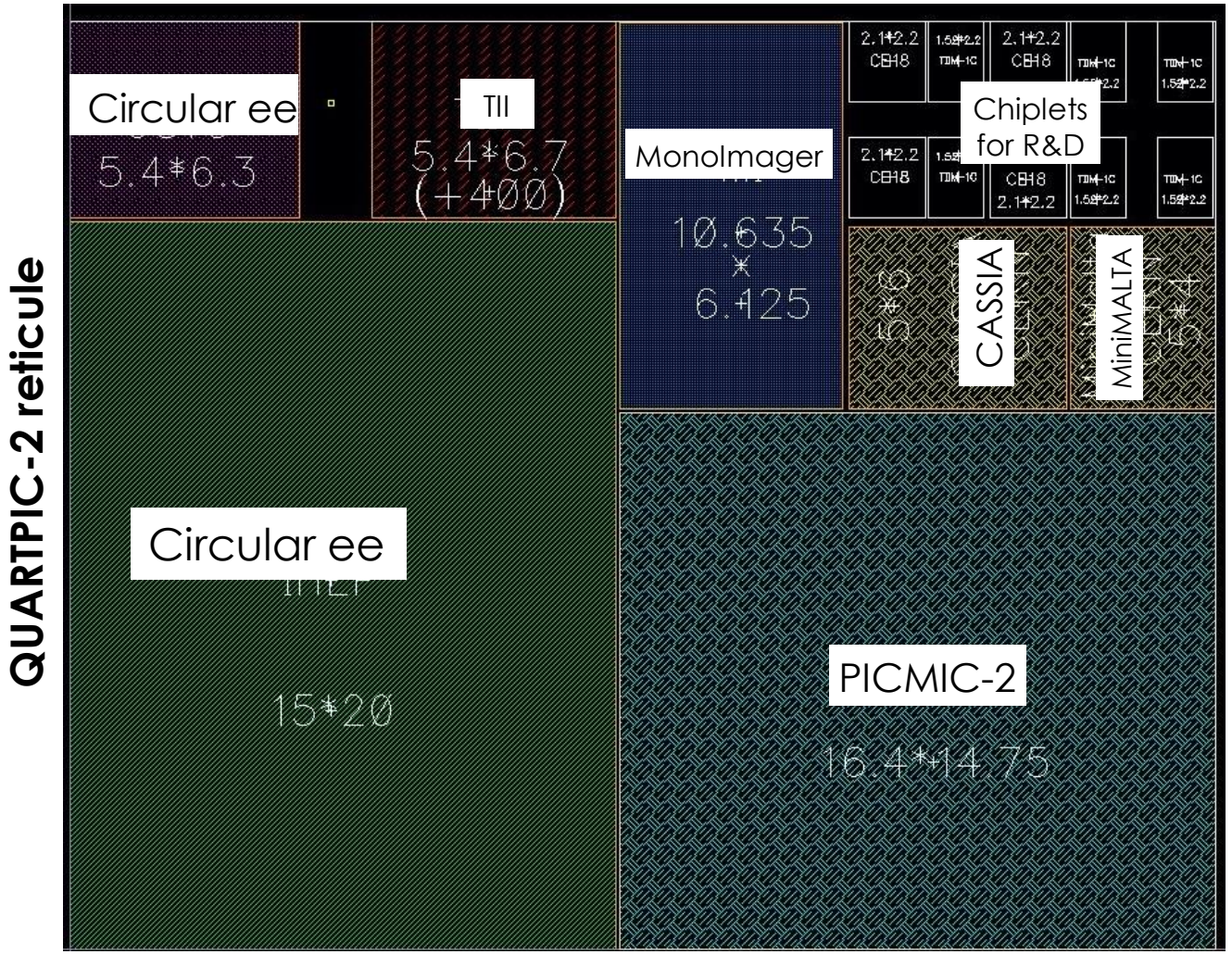


TJ 180nm Activities in DRD7.6a

- **Foundry submissions**
  - Planned ER with reticule assembled @ IN2P3-IPHC from various sensors & IPs and from multi-contributors (DRD3, …)
    - Fall 2024: surface booked-out, financed, date to be fixed
    - Fall 2025: still surface available, partially-finance
  - Planner ER for experiments
    - OBELIX-1 (2024), MIMOSIS-3 (2025)
  - Wafer dicing to retrieve individual sensors: MicroPacks platform in France
  - Export license with Tower: discussion on individual basis
- **Design support**
  - Digital on top flow available (used with IN2P3-IP2I for TIIX project)
  - Many IPs already existing from past projects (STFC, IPHC/CPPM, CERN,) => documentation to be discussed
  - IP under development: fast ADC-12bits (new DRD7 member, IN2P3-APC)
- **Through CERN**
  - Specific TCAD simulations
  - Availability of specific process modifications

DRD7.6

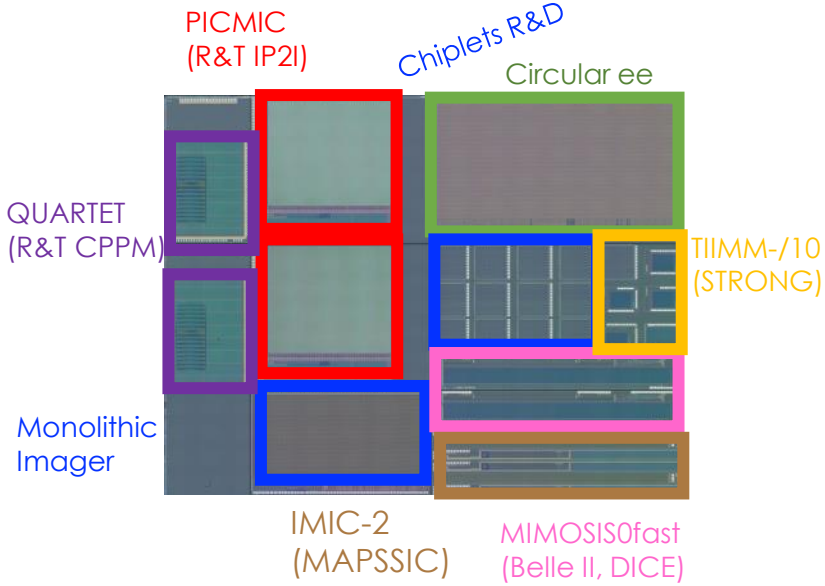
ER Fall 2024 Submission Content



Project categories:

- Tracking: circular ee, TIIX, MiniMALTA
- Imaging: MonoImager, PICMIC-2
- R&D: CASSIA, Chiplets

Previous ER 2022
QUARTPIC-1 reticule



LF 110nm CIS

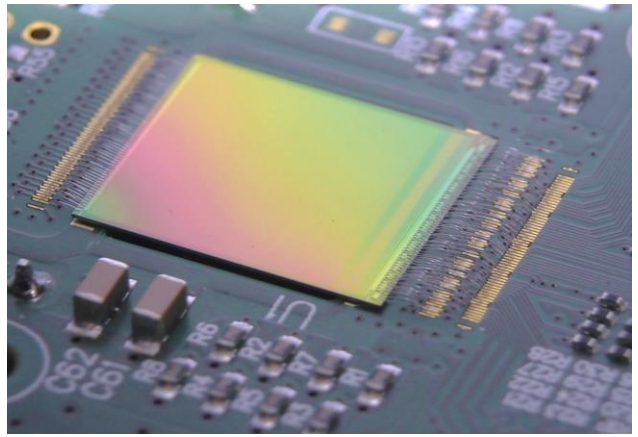
Marlon Barbero, Jerome Baudot, Manuel Rolo, Iain Sedgwick, Walter Snoeys

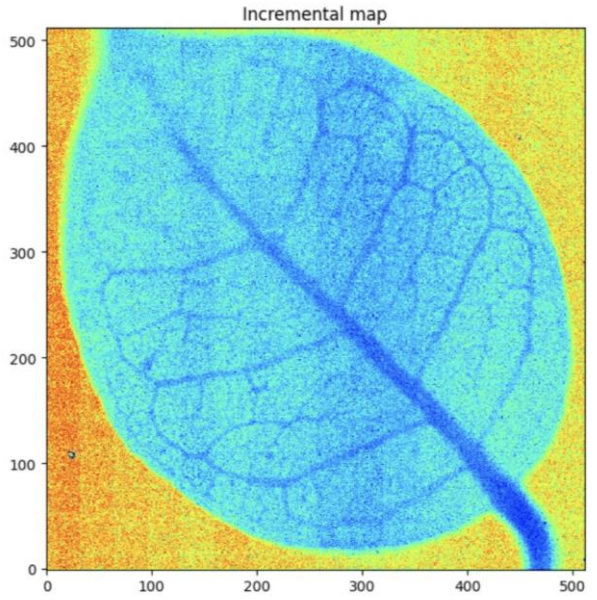
DRD7.6

ARCADIA LFoundry 110nm CIS

CMOS sensor design and fabrication platform on LF11is technology

- Scalable FDMAPS architectures with very low-power: 10 mW/cm^2
- MD3: demonstrator full-chip FDMAPS for Medical (pCT), Future Leptonic Colliders
  - Analysis of July/24 test beam data (120 GeV protons at FNAL) ongoing.
- Custom BSI process allow for fully-depleted thick sensors (> 400µm) for X-ray imaging
- Fully-depleted monolithic active micro strips with fully-functional embedded readout electronics
- Ongoing R&D for the implementation of monolithic CMOS sensors with gain layer for fast timing, candidate technology for the ALICE3 Time-of-Flight detector.
  - Wafers from ER5 just received, tests on devices with intrinsic gain layer ongoing.



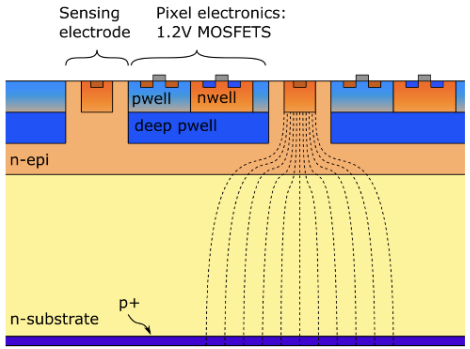


The ARCADIA **MD3** sensor (top) and a leaf imaged using 6keV X-rays from a ^{55}Fe source (bottom)

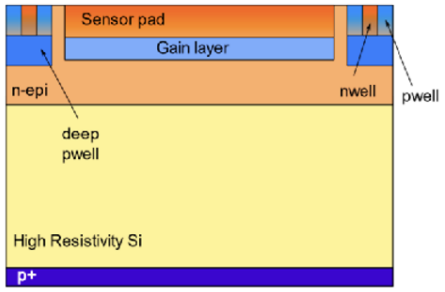
Recent presentation of the ARCADIA technology here: https://indico.cern.ch/event/1417976/contributions/5962699/

DRD7.6

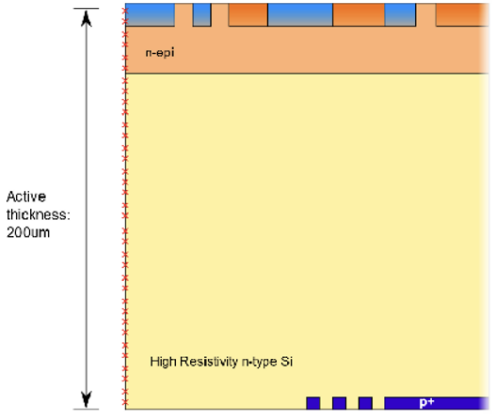
ARCADIA LFoundry 110nm CIS: sensor concepts



- n-type high resistivity active region + n-epi layer (reduces punch-through current between p+ and deep pwells)
- sensing electrodes can be biased at low voltage (< 1V)
- BSI Reverse-biased junction: depletion grows from back to top
- Ongoing R&D: Fully Depleted PAD sensors with gain layer



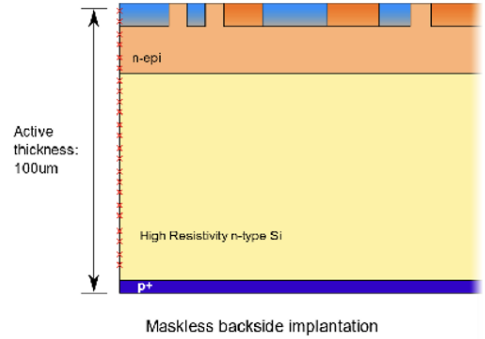
HR wafers - backside litho



Masked backside implantation

thinning, lithography, backside p+ implantation and laser annealing, insulator and metal deposition to create backside guardring structures

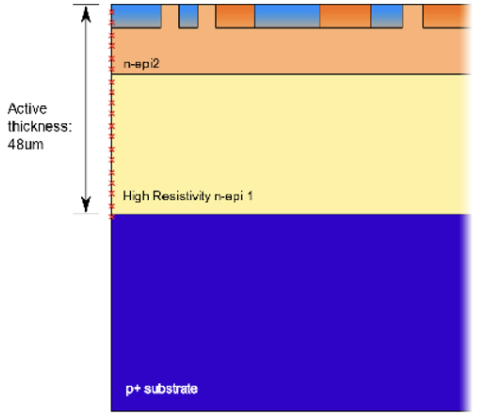
HR wafers - no backside lithio



Maskless backside implantation

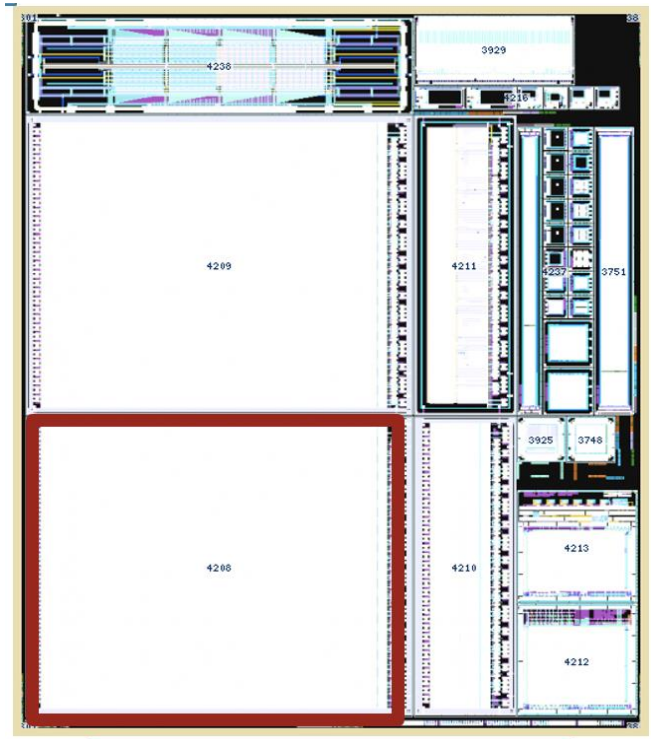
thinning, backside p+ implantation and laser annealing, no patterning on backside

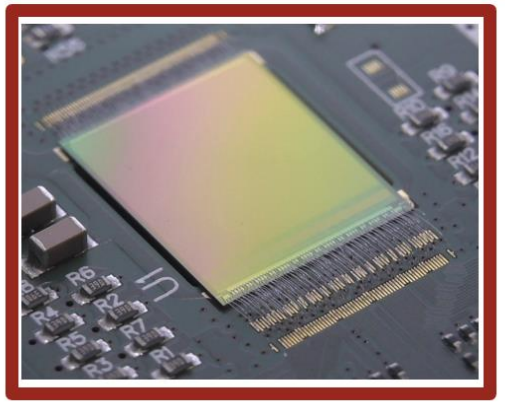
p+ wafers - double epi



Total thickness: 300um

thinning down to 100µm total thickness on a p+ starting substrate, active thickness below 50µm

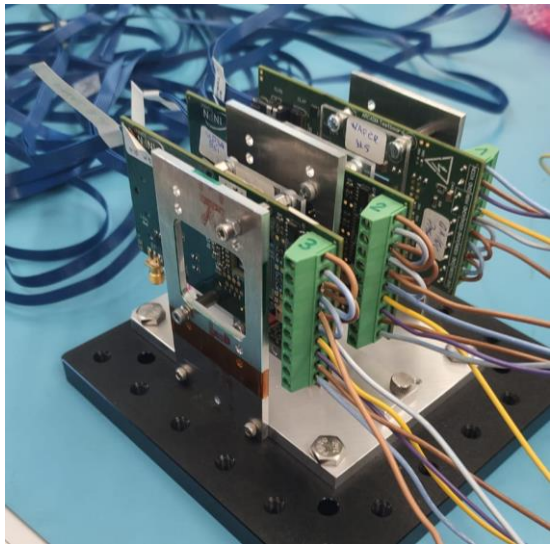


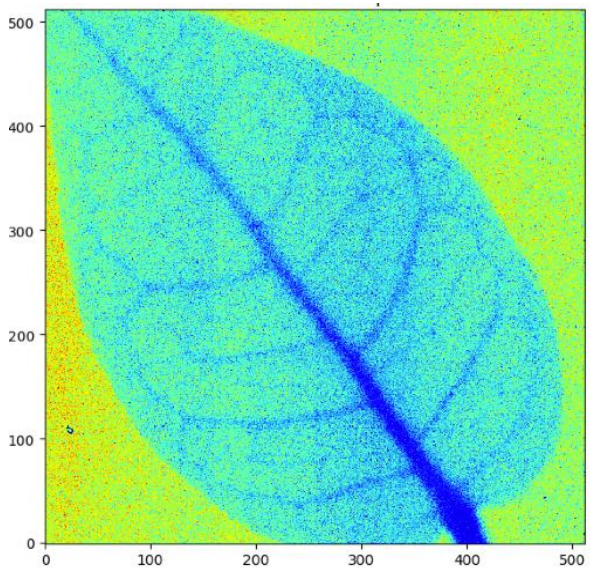


The ARCADIA reticle floorplan for ER3

ARCADIA LFoundry 110nm CIS
Common Access and Support for joint LF11is production runs

- Possibility to explore multiple wafer splits: n-epi thickness, n-type or p-type starting substrate, substrate resistivity, FSI or BSI process on different wafer thicknesses, use of a gain layer for the implementation of monolithic CMOS LGADs.
- INFN and LFoundry agreed on the terms to allow for the participation of third-party design groups to joint LF11is production runs, enabling straightforward and low-risk ramp-up of the R&D on FDMAPS using LF11is technology for new design teams.
- Silicon-proven IP available (Serialisers, c-LVDS Transceivers, bandgap/LDO, SPI, DAC/ADCs).
- Digital-on-top integration flow and scripts available.
- Multiple engineering runs (full-reticle sets and multi-layer mask set) already funded at INFN through 2025-2028, possible to host new IP and test-chips in the framework of DRD7.6





The ARCADIA **MD3** telescope (top) and - again - a leaf imaged with a 6keV X-rays using a ^{55}Fe source (bottom)

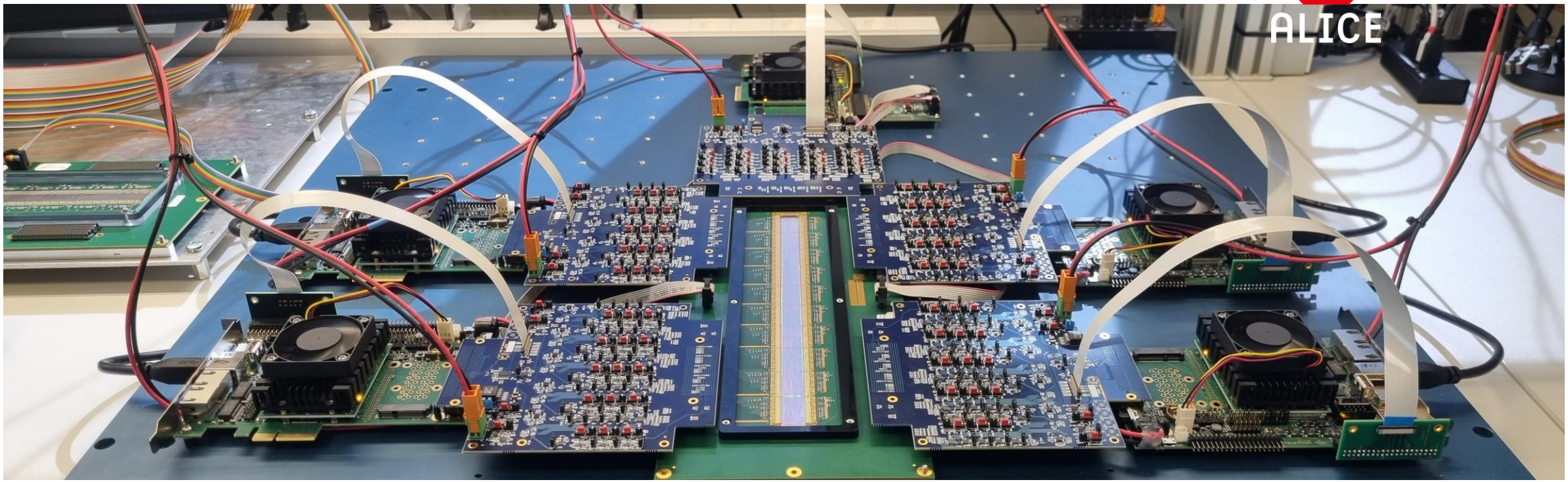
Resource Table

Resources cannot easily be finalised, and the picture is complex.

- Some funds are already in place (e.g. EP R&D funding, and INFN funding for LF)
- However, most institutes will have to request these funds from their funding agencies based on the support of DRD7. These requests will have different deadlines, timescales and commitment horizons.

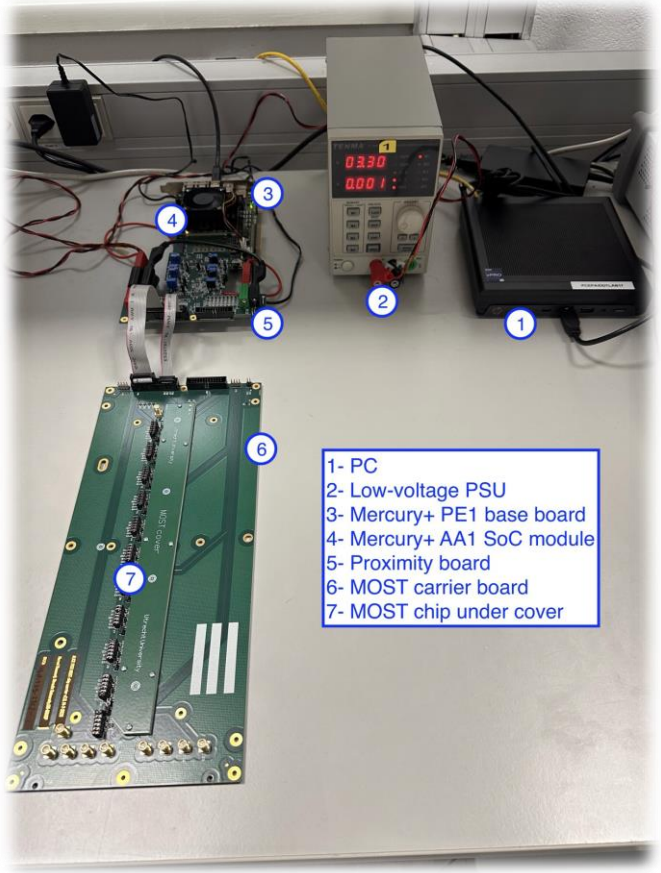
Questions?

Backup



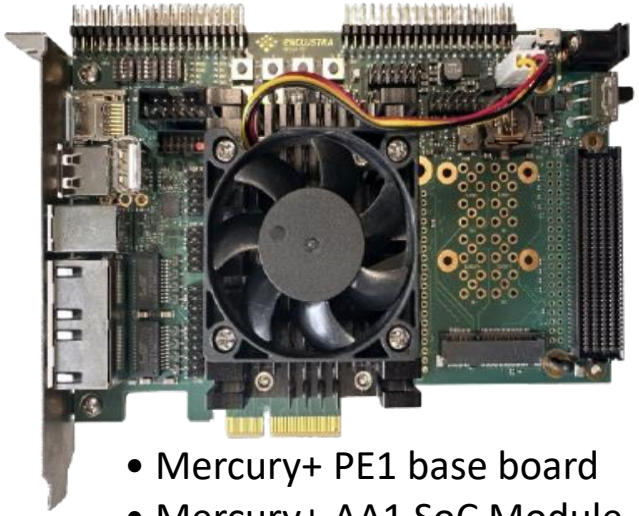
MOSS Stitched Sensor Functional Tests

- MOSS design fully functional
  - Design concepts and methodology validated
  - Block level yield and local defect rate under study
    - Faults probability seems negligible with respect to power shorts
  - No evidence of yield difference between the two layout densities
- Learnings and improvements to be employed in the ER2 engineering prototype (MOSAIX)



MOST Stitched Sensor test setup

Base board



- Mercury+ PE1 base board
- Mercury+ AA1 SoC Module
- USB connection to PC
- FMC connection to Proximity board
- Needs FX3 + MOST firmwares

Proximity board

- 1 x DAC63004 for VDD supplies
- 2 x AD5668 for bias supplies
- 1 x AD7091R for current monitoring
- VDD regulators + Digital buffers
- FMC connection to base board

- Significant test effort at Nikhef and CERN Documentation: • MOST Test-System and Hardware Wiki
- Firmware/software development Younes Otarid (several elements from ALICE)
- Carrier and proximity board design (Marcel Rossewij Nikhef)