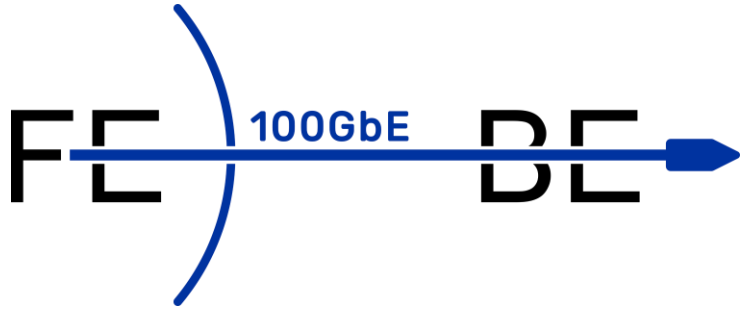
From Front-End to Back-End with 100GbE

(Project 7.5b)



sophie.baron@cern.ch

On behalf of the 7.5b contributors

Imperial College London | UKRI Science and Technology Facilities Council | University of Bristol | CPPM Centre de Physique des Particules de Marseille | Nikhef | Brookhaven National Laboratory | CERN

Project Target

- The perspective of future HEP experiments with lower radiation levels opens the door to increasing complexity in Front-End
- FE Datalink bandwidth follows (at a distance) the Ethernet trend (10G, 4x10G, 4x25G)
- New SiPho developments enabling 100Gb at FE

⇒ All the ingredients are there for high throughput 100GbE-based FE data readout link

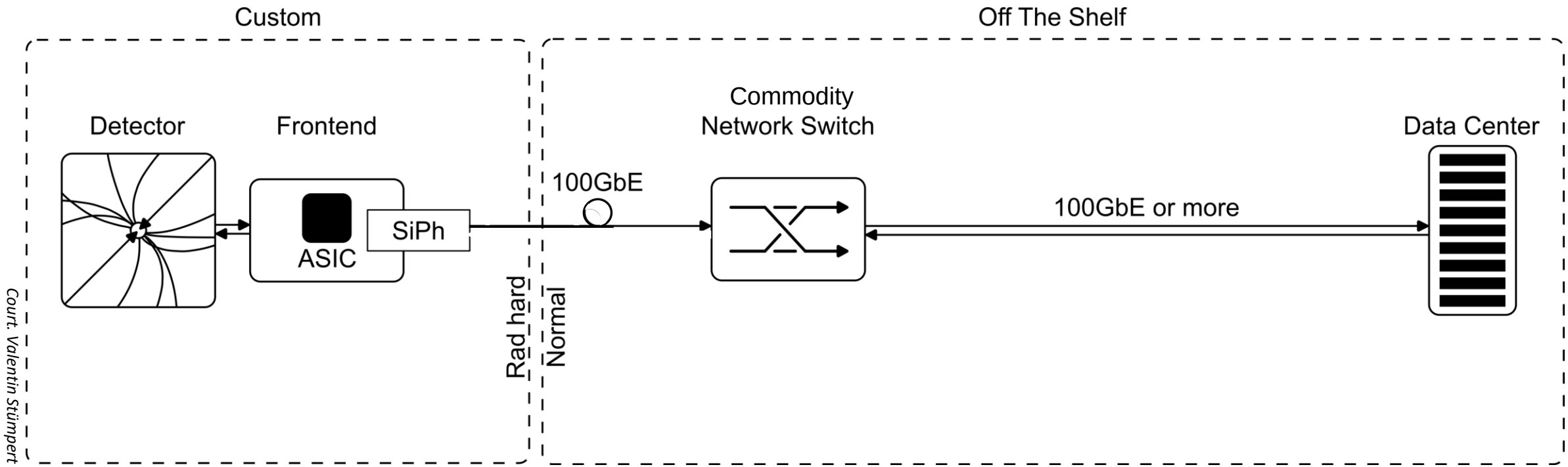
⇒ Right time to envisage a long-time avoided concept of implementing 100GbE in FE

⇒ All aspects shall be tackled (FE, BE, Network, Switches, Protocol..)

NEW PARADIGM to be investigated in DRD7.5b

Investigation Themes

- Approach 1: The radical One … NO BACKEND



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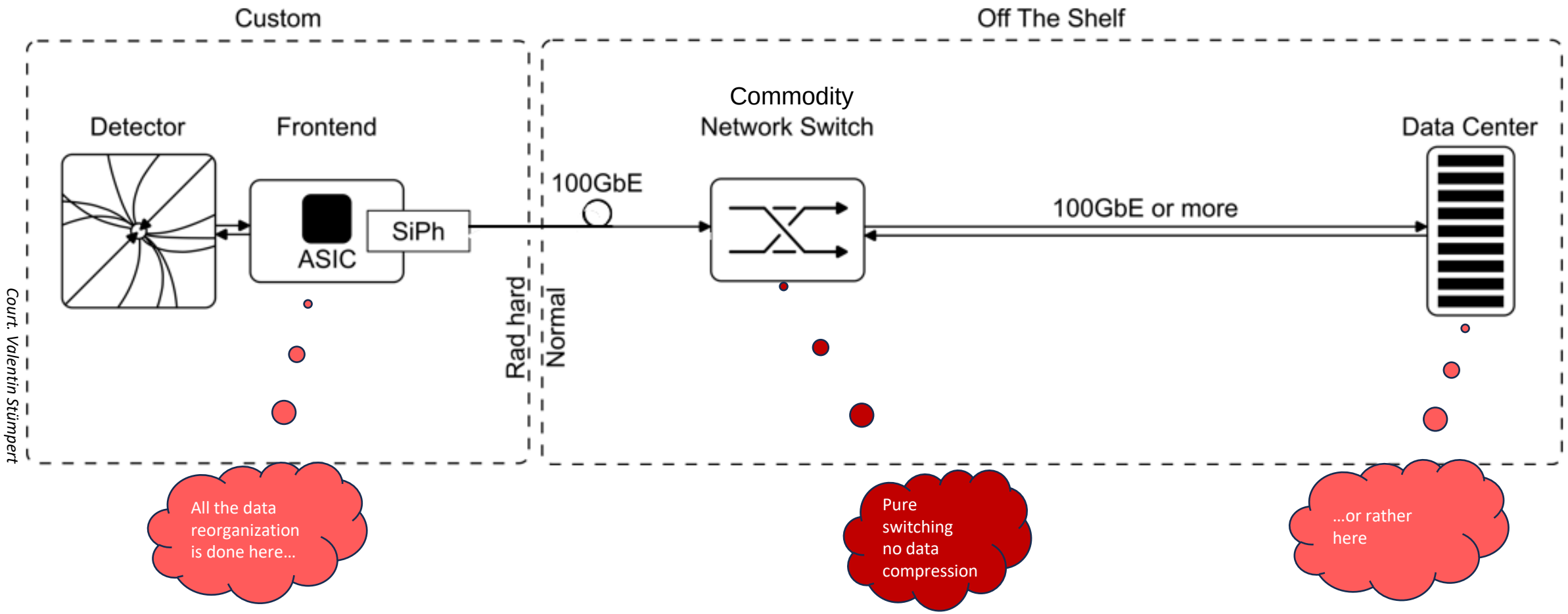
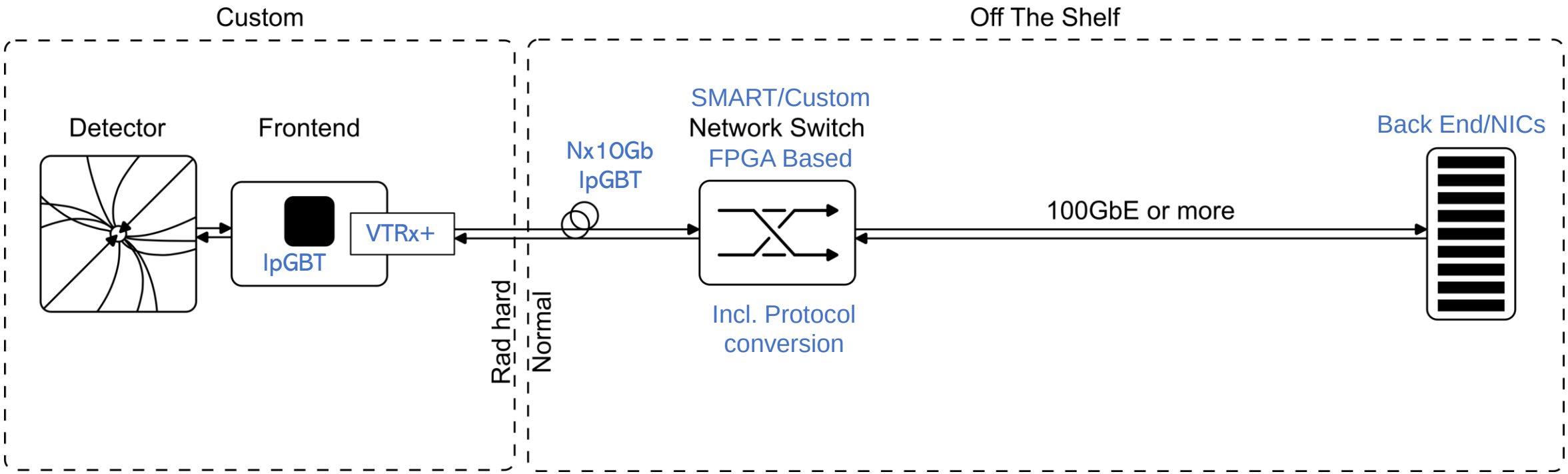


Investigation Themes

- Approach 2: A staged One … SMART SWITCH



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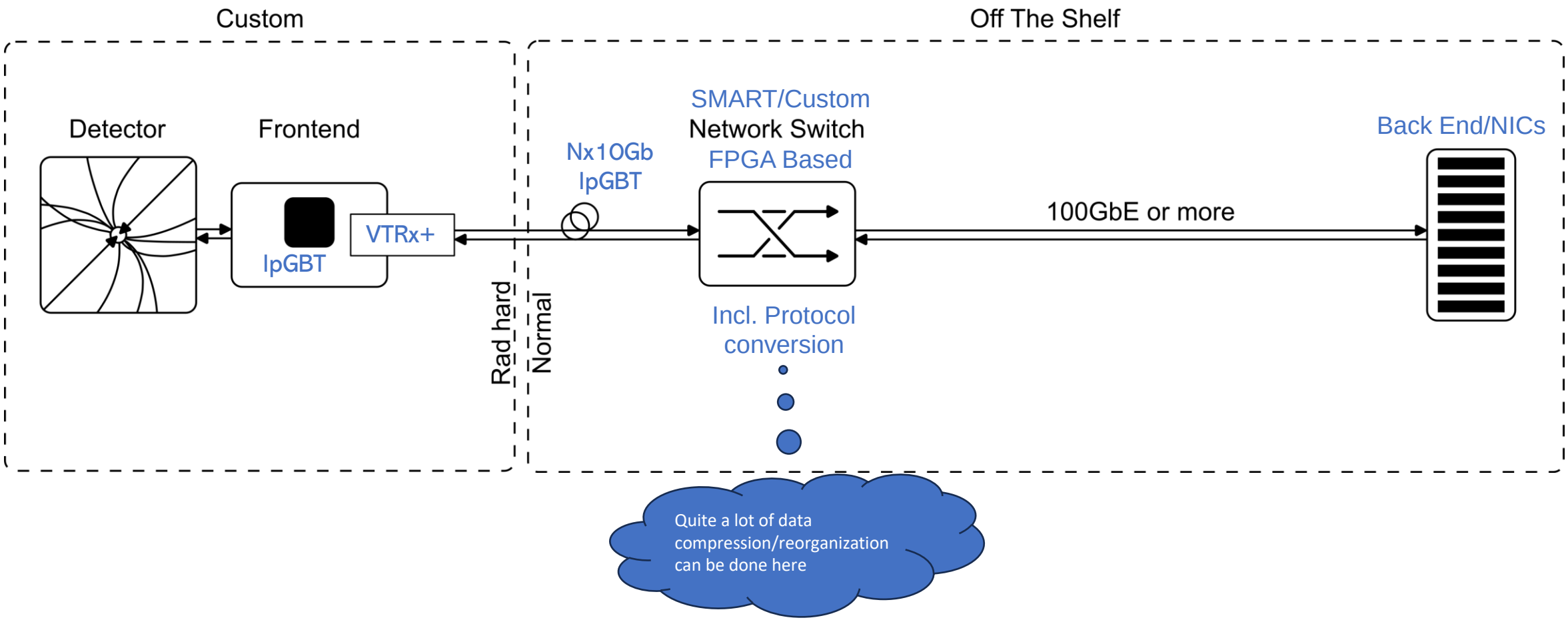

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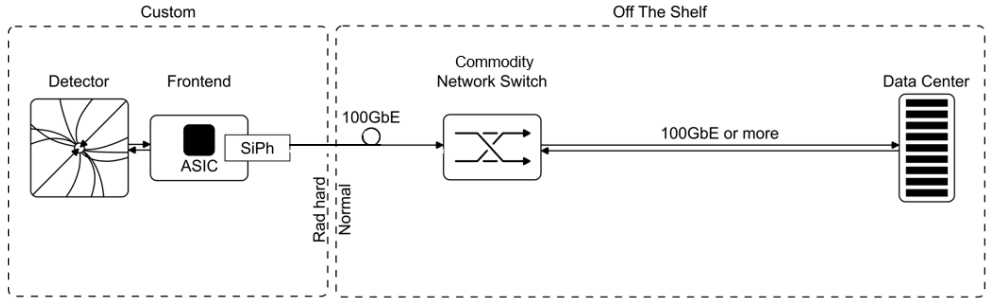
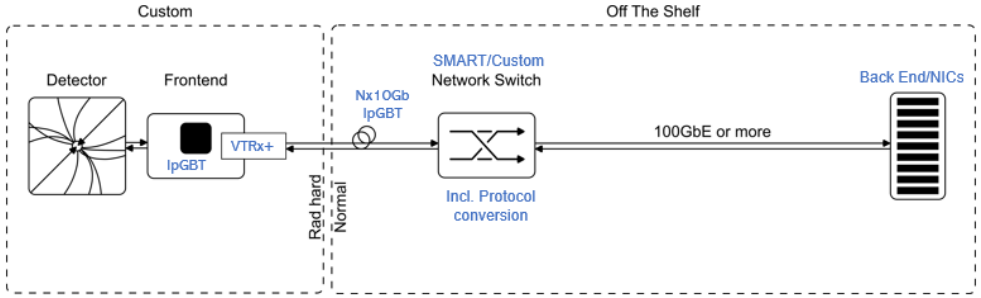
Investigation Themes

NO BACKEND



SMART SWITCH



Investigation Themes

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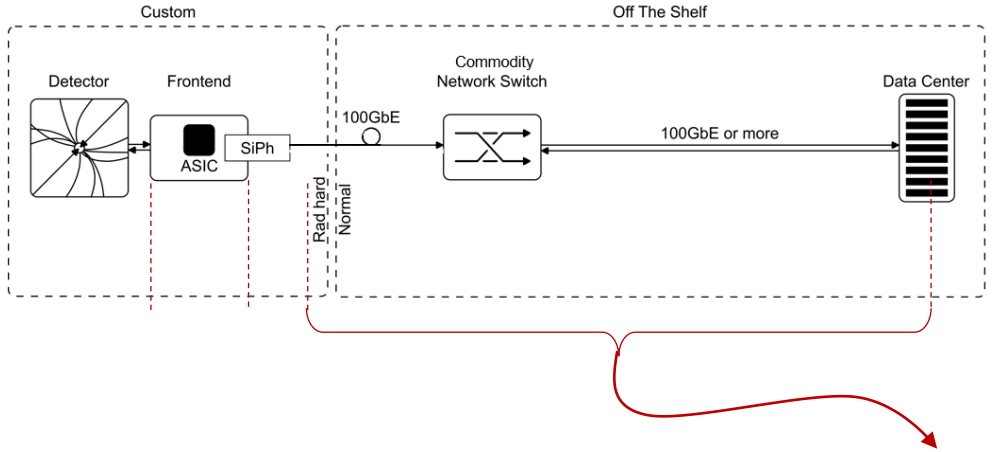

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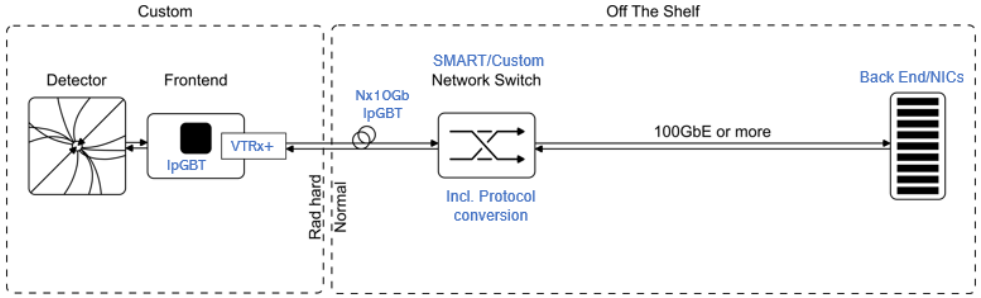
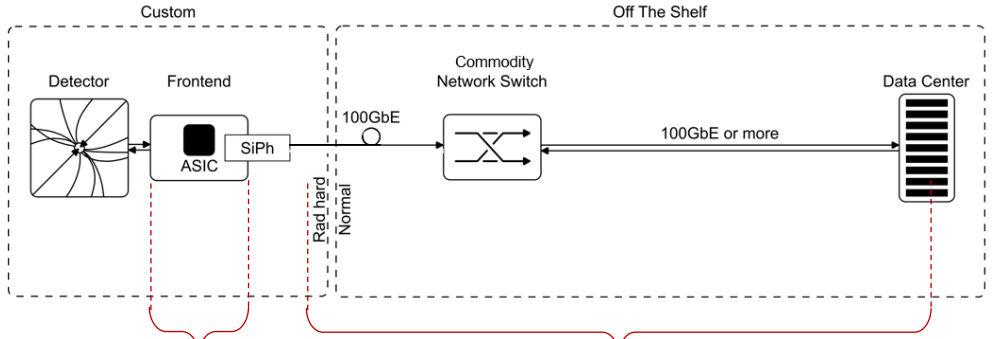


Theme 1 : using 100GbE COTS switches to handle data-streams from the Front-End to Network Interface Cards (NICs) or even DAQ processors (CERN LBC and ESE groups).

Investigation Themes

NO BACKEND



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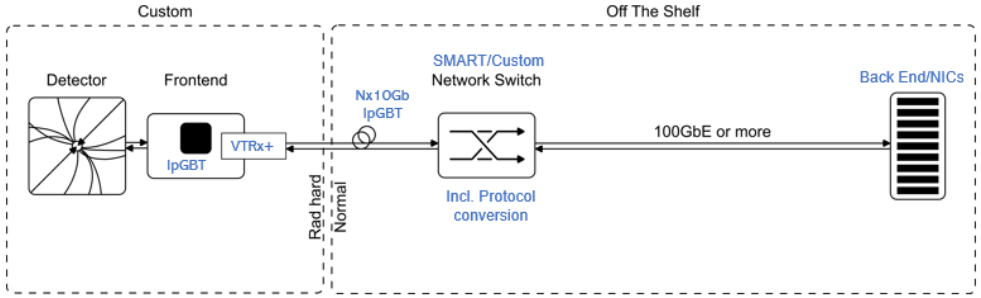

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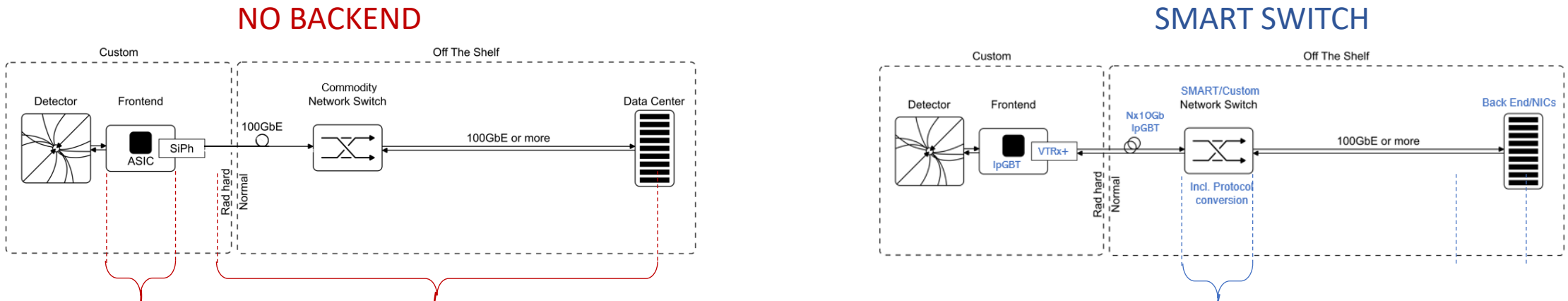
Theme 4 : study and design of the building blocks IPs necessary for 100Gb Ethernet cores implementation in future FE ASICs. (Rutherford Lab)

Investigation Themes



Theme 1 : using 100GbE COTS switches to handle data-streams from the Front-End to Network Interface Cards (NICs) or even DAQ processors (CERN LBC and ESE groups).

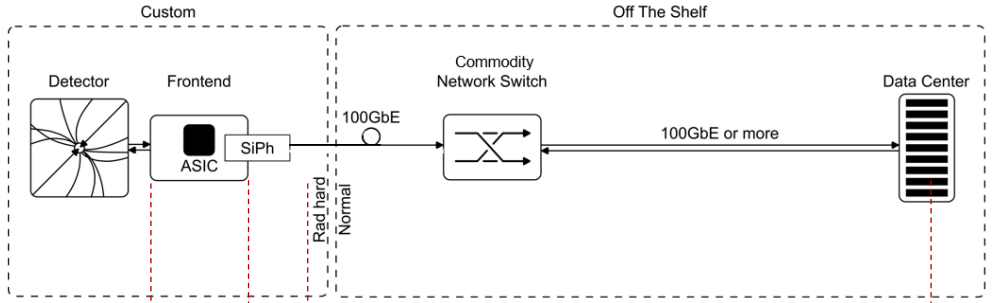
Theme 2: design of a COTS-based high-density switch bridging the detector environment to the COTS/DAQ world (Imperial College).

Theme 4 : study and design of the building blocks IPs necessary for 100Gb Ethernet cores implementation in future FE ASICs. (Rutherford Lab)

Investigation Themes

FE 100GbE BE

NO BACKEND



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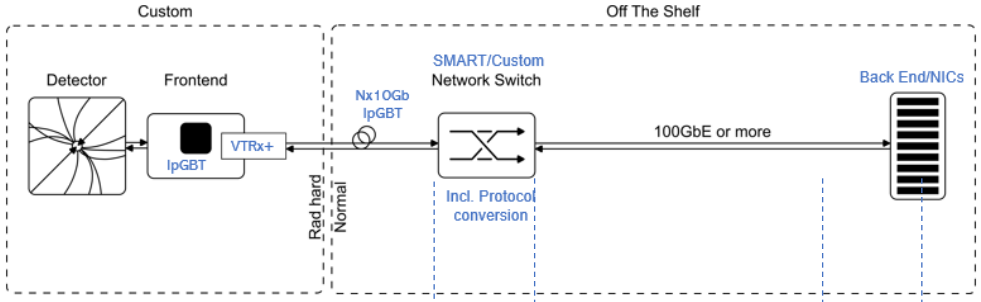

Theme 1 : using 100GbE COTS switches to handle data-streams from the Front-End to Network Interface Cards (NICs) or even DAQ processors (CERN LBC and ESE groups).

Theme 2: design of a COTS-based high-density switch bridging the detector environment to the COTS/DAQ world (Imperial College).

Theme 3 : to explore DAQ topologies (based on custom boards for DAQ, concentration and processing) (CPPM CNRS/IN2P3, Nikhef, Brookhaven National Lab

Theme 4 : study and design of the building blocks IPs necessary for 100Gb Ethernet cores implementation in future FE ASICs. (Rutherford Lab)

Organization

- Members
  - ~20 active members* from ...
  - 7 Institutes
  - 5 countries

ecfa-drd7-project7_5_b-contributors@cern.ch
ecfa-drd7-project7_5_b-observers@cern.ch

*FTE count is much less though ☺

Organization

- Members
  - ~20 active members* from ...
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- Meetings
  - https://indico.cern.ch/category/18021/
  - Kick-off meeting @ CERN in March 2024
  - 2 remote Catch-up meetings in June and September
  - Next one Nov dedicated to Data Format

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- Project Lead
  - Project Lead: Sophie Baron, CERN
    - Sophie.baron@cern.ch
  - Deputy: Antonio Pellegrino, Nikhef
    - antonio@nikhef.nl
  - Rotating every year

ecfa-drd7-project7_5_b-contributors@cern.ch
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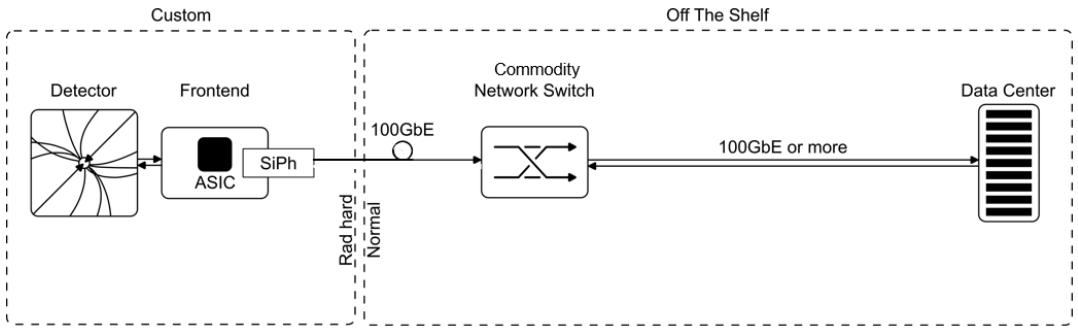
Progress Report - NO BACKEND APPROACH



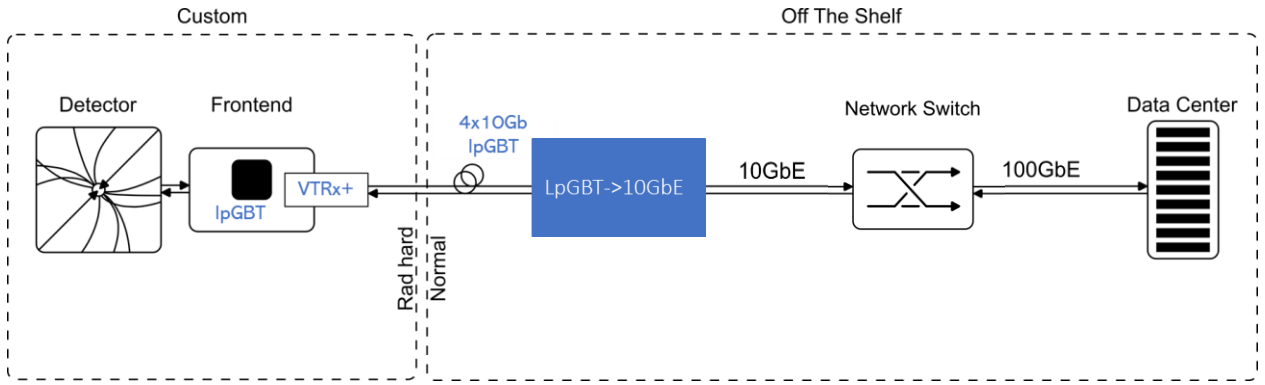
EP- ESE & LBC

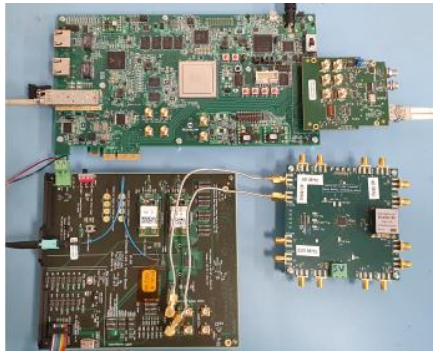
Checks

- ☑ Compatibility with COTS
- ☑ Unidirectionality
- ☑ Data Format compatibility with radiation induced SEUs
- ☒ Triggered systems
- ☒ Timing Distribution

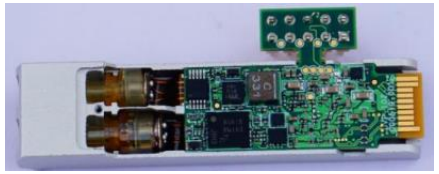
Funded

Demonstrators / Stepping Stones towards full 100GbE: on-going work

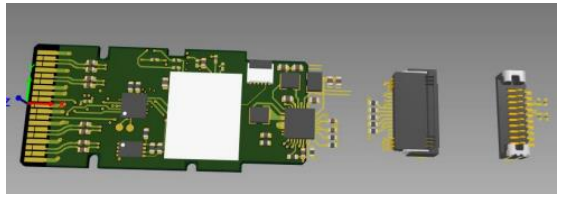




Eval kits based



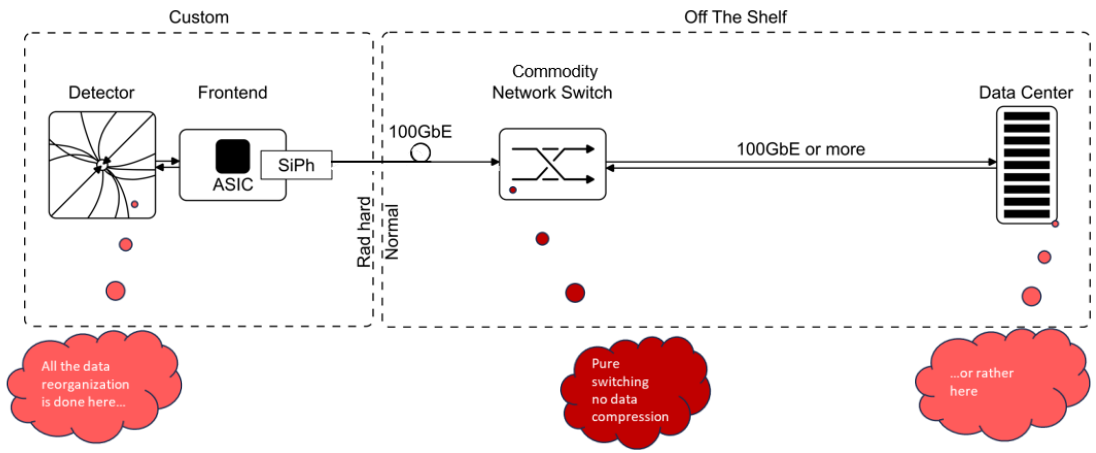
SFP based (Commercial)



QSFP based (in-house design)

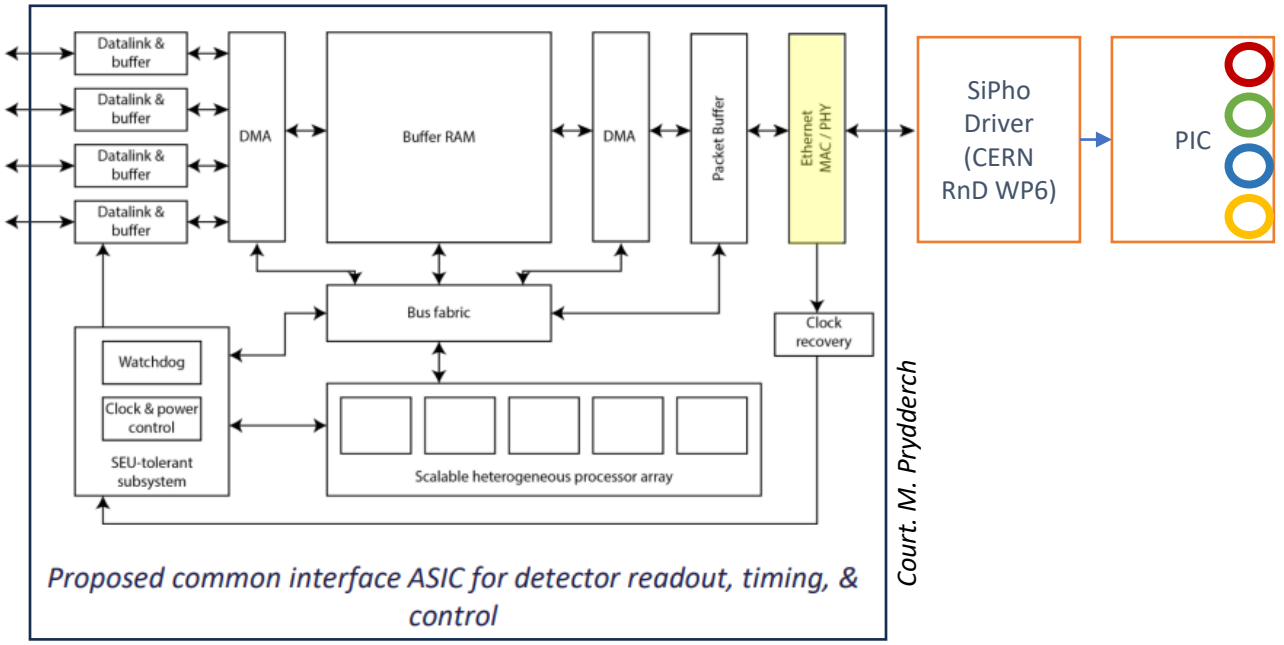
See poster @ CERN EP RnD Days or TWEPP 2024

Progress Report - NO BACKEND APPROACH



Early stage of funding request passed
Now waiting for the second stage

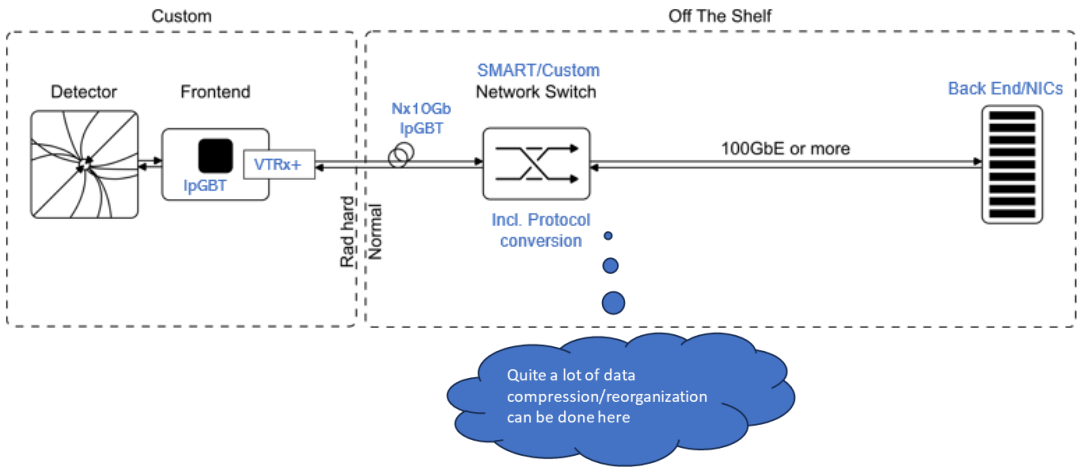
Science and Technology Facilities Council



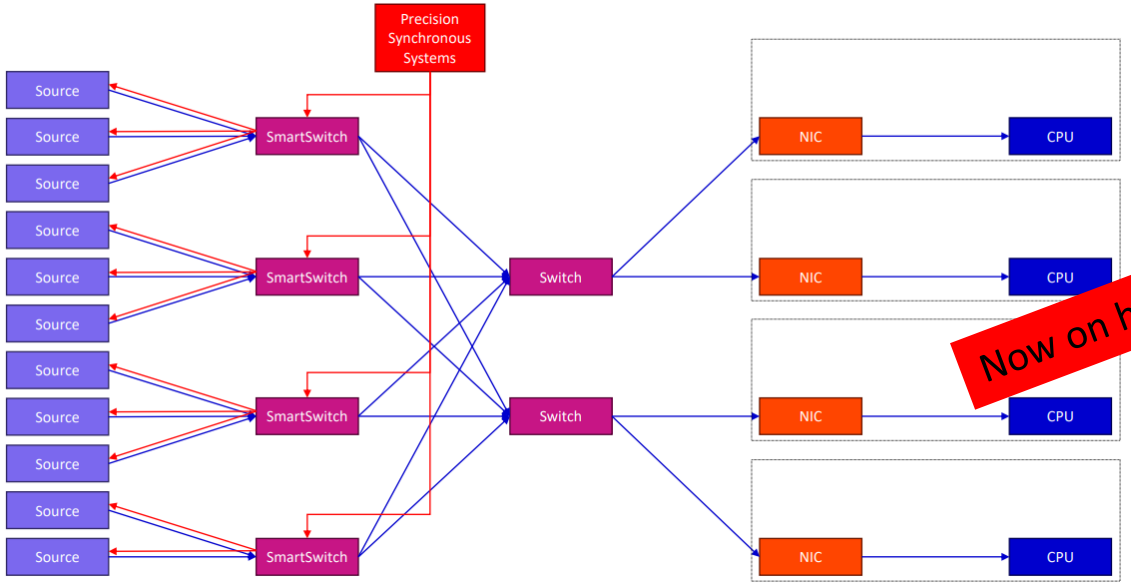
Project to start April 25 (together with 7.2.b SoC) if funding granted

Science and Technology Facilities Council
MANCHESTER 1824 The University of Manchester
WARWICK
UNIVERSITY OF BIRMINGHAM
University of BRISTOL
OXFORD

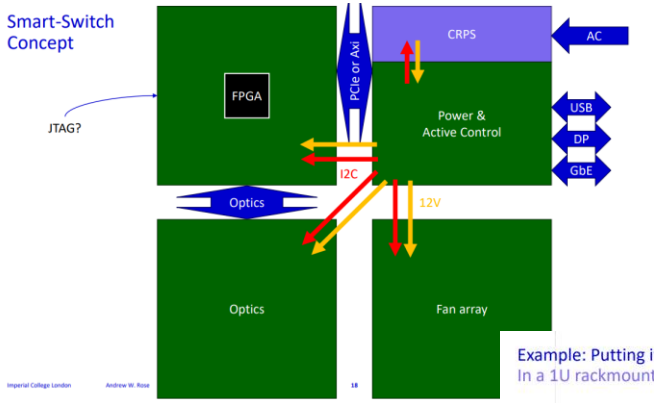
Progress Report - SMART SWITCH APPROACH



Smart Switch concept:



Court. A. Rose



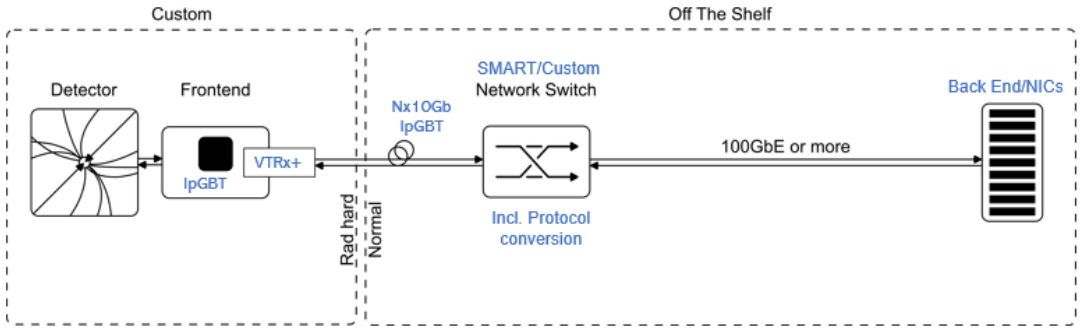
Court. A. Rose

Now on hold as not funded for 2025

Court. A. Rose

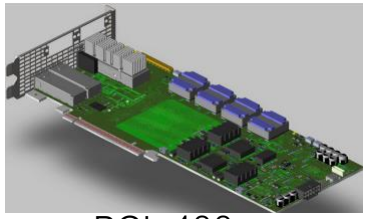
Status:
Preliminary design work completed

Progress Report – BACK-END BOARDS



CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE
CPPM

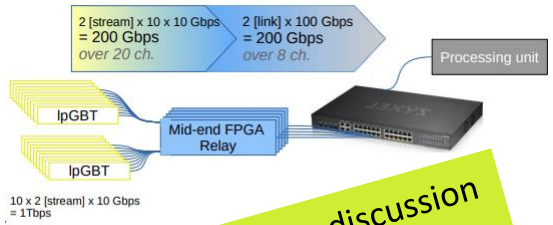
Various DAQ topologies based on PCIe 400



PCIe400…

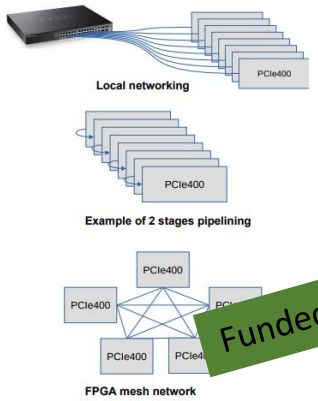
WORK NOT YET STARTED

…as Mid-End Relay



Funding under discussion
But should be ok

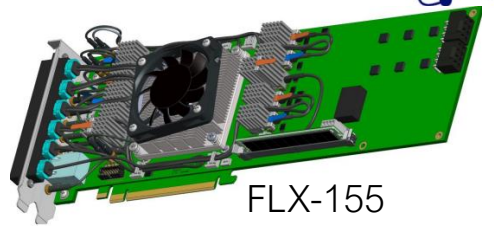
…as Back-End



Funded

Nikhef
Brookhaven National Laboratory
IFIN-HH
NEW

FLX-182



FLX-155

1. All to/from data transfers of 1 kByte blocks via 100 GbE link interfaced directly to the on-board FPGA – e.g. using RDMA (with IFIN-HH): on-going activity
2. Slow control of FPGA custom card via the 100 GbE link with standard TCP
3. Fast control (low-jitter bunch-crossing clock, fixed-latency trigger and resets, BUSY) via the 100 GbE link

Partially funded
Awaiting for 10-year funding round

Plans & Updates

- NO BACKEND : No show-stoppers on the hardware side
  - Although some challenging caveats
    - Unidirectionality and timing inducing system constraints
    - Software/CPUs would have to deal with large and scrambled data frames
      - As data reduction will probably not be portable into the FE
  - Intermediate stage with translator modules
    - Could potentially be used for LS4 updates
    - Data format under discussion:
      - converting lpGBT frames into GbE / intermediate reduction stage in translator modules ?… getting closer to the Smart Switch approach
      - This will be the topic of next project meeting in November
  - FE awaiting for funding
- SMART SWITCH on hold for now
  - Will be re-envisaged in next funding round
- Work on Back-End starting
  - 2/3 platforms with 2 FPGA vendors
- New candidates joining the « Back-End studies »
  - FPGA-based RDMA communication on Virtex (IFIN-HH, Bucharest)