DRD 7.6b
Shared Access to 3D Integration
Progress Report

MPG HLL
Fachhochschule Dortmund
University of Applied Sciences and Arts
UNIVERSITY OF OSLO
NORWEGIAN MICRO- AND NANOFABRICATION FACILITY NorFab
UNIVERSITÉ DE SHERBROOKE
UNIVERSITAS BERGENSIS
USN University of South-Eastern Norway
KIT Karlsruher Institut für Technologie

Contact persons: L. Andricek, M. Caselle, S. Charlebois

DRD7.6 *ID card*

Project Name	Shared Access to 3D Integration (WP7.6b)
Project Description	Develop advanced chiplet and 3D integration technologies, including the integration of SiPh chips on detector, by in-house infrastructures and third-party vendors
Initial duration	3 years with potential for further prolongation beyond
Innovative/strategic vision	Potential of silicon interposer and chiplet technologies. In-house infrastructure for quick production of prototypes/demonstrators and test vehicles, by employing bump-bonding and detector packaging technologies already available. To establish a concrete connection with the industrial partners
Performance Target	*Shared competences/experiences* and infrastructures/processes. *Build up and maintain the capability* for a quickly transposed to 3D integration. *Keeping a cost-effective access to selected technologies*
Multi-disciplinary, cross-WP content	Strong connection with 7.1 for the integration of SiPh chip and optical fiber on detector module. Strong connection with 7.6a (e.g. 3D integration/chiplets)
Available resources	5.5 FTE/yr , 390k/yr

Proposed Milestones and Deliverables

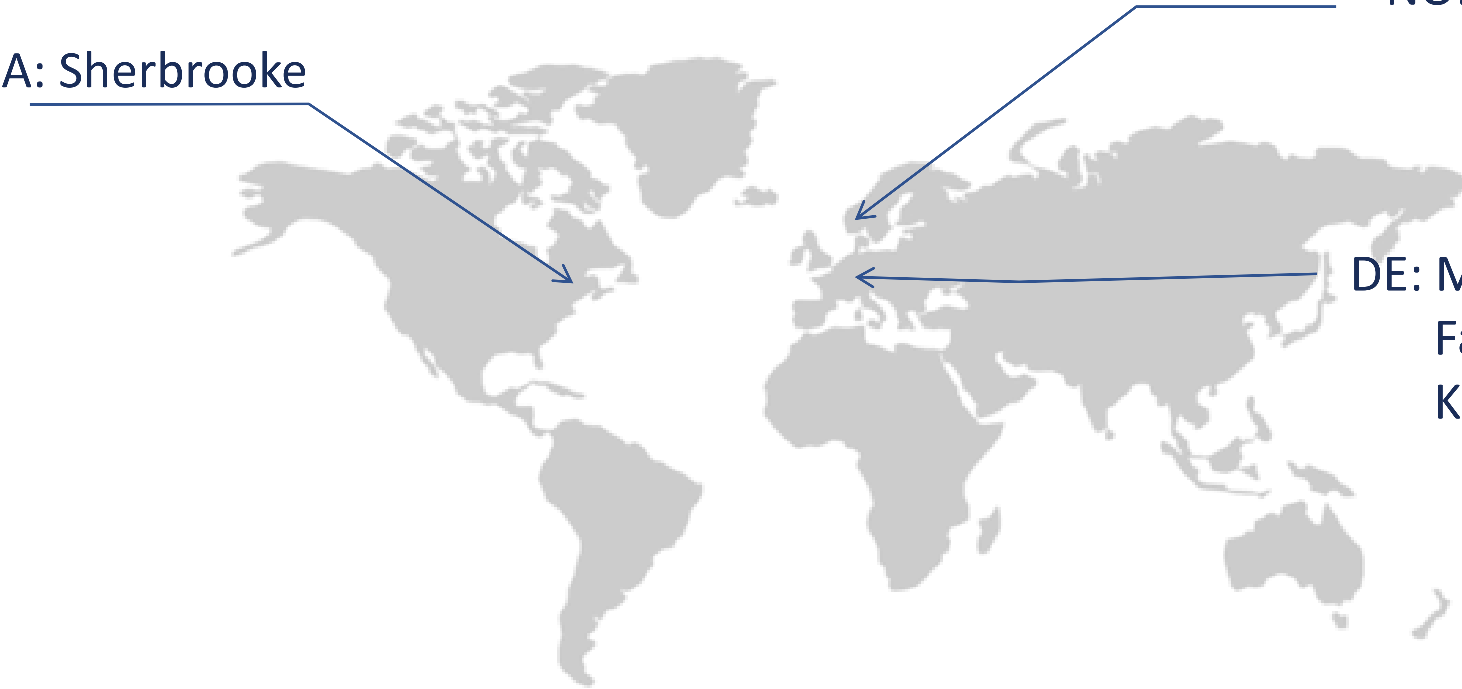
- M7.6b.1 (M18) Establish TSVs process on active/passive interposer, wafer/single die
- M7.6b.2 (M24) Establish RDL process and back-side metallization on real CMOS sensors and custom-designed silicon interposer

- D7.6b.1 (M30) Delivery of report summarising the integration of SiPh on detector by 2.5D interposer/chiplet technologies (→ with DRD 7.1)
- D7.6b.2 (M30) Delivery of a report on W2W bonding by industrial partners
- D7.6b.3 (M36) Deliver documentation of the process for the common use

Work Topics and Areas of Contribution

- Provide access to TSV technology
  - MPG HLL , KIT
- Provide access to RDL technology
  - MPG HLL, KIT
- Provide access to small-pitch 2D-bonding process including maskless (ACF/ACP)
  - Norway, MPG HLL, KIT
- Provide access to chiplet/2.5D integration
  - FH Dortmund, MPG-HLL, KIT, Norway, Sherbrooke
- Provide access to W2W, C2W by industrial partners
  - Sherbrooke, Norway
- Integration of Photonic IC on the detector (→ with DRD 7.1)
  - Sherbroke, KIT

Contributors



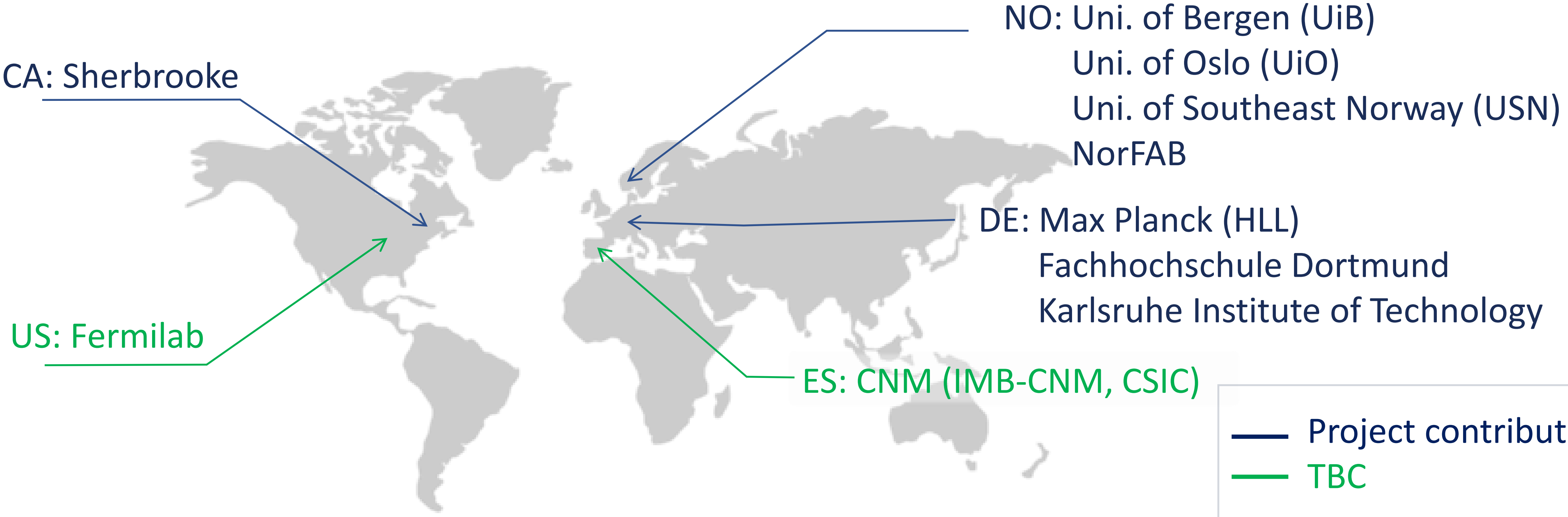
CA: Sherbrooke

NO: Uni. of Bergen (UiB)
Uni. of Oslo (UiO)
Uni. of Southeast Norway (USN)
NorFAB

DE: Max Planck (HLL)
Fachhochschule Dortmund
Karlsruhe Institute of Technology

— Project contributors

Evolution of the collaboration within 7.6b project



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Fachhochschule Dortmund
Karlsruhe Institute of Technology

US: Fermilab

ES: CNM (IMB-CNM, CSIC)

— Project contributors
— TBC

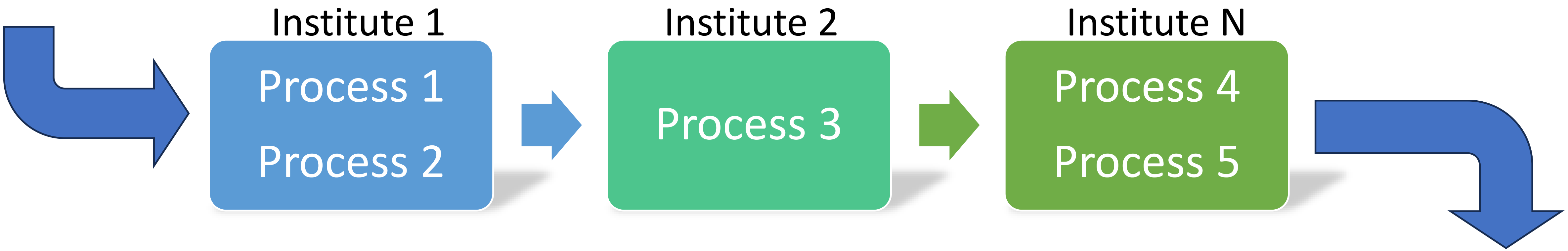
- CNM and Fermilab have expressed interest in joining. 10 institutes, 5 large national labs with well-renowned experience in interconnection technology and detector production
- Kick-off meeting - September 3rd (2024)

International Distributed Detector Laboratory

- Establish a distributed laboratory that operates as a hub-service for the community
- Each institute highly specialized in one or more technological processes

From community:

- Request of process/service
- Rapid prototyping of new detector
- Detector production (large scale)



Maintaining a strong connection with application/experiment requirements

To community
(institute/experiment)

International Distributed Detector Laboratory

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From community:
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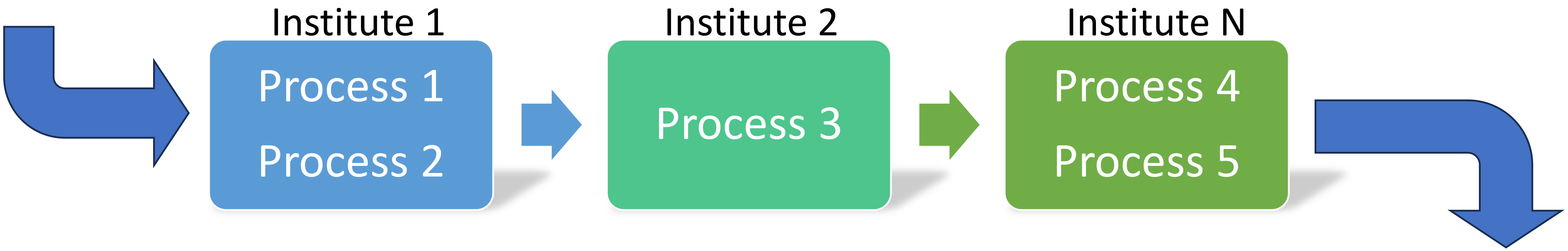
Key parameters, are:
- Interface between institutes/processes
- Redundancy
- Complementary
- Development of new processes that are not currently in place



Institute 1

Process 1

Process 2

Institute 2

Process 3

Institute N

Process 4

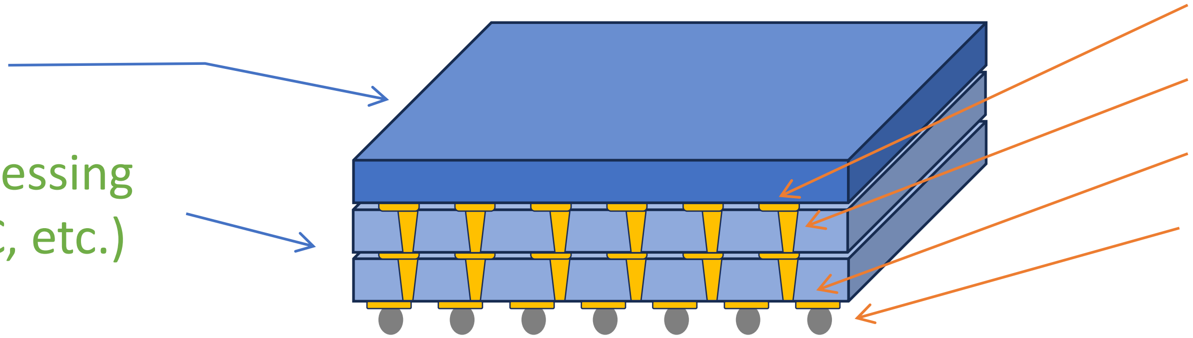
Process 5

Maintaining a strong connection with application/experiment requirements

To community
(institute/experiment)

Heterogenous 3D-ASIC integration

- The combination of TSV, RDL technologies, along with already existing in-house packaging technologies, will allow for a rapid transition towards the implementation of **3D-ASIC integration at the level of a single assembly (**e.g. Multi-Project Wafer)



Monolithic sensor
(TJ, TPSco, LFoundry)

Digital memory + processing
(65/28nm TSMC, UMC, etc.)

High-density intercon.

TVS

RDL

UBM/bumping deposition

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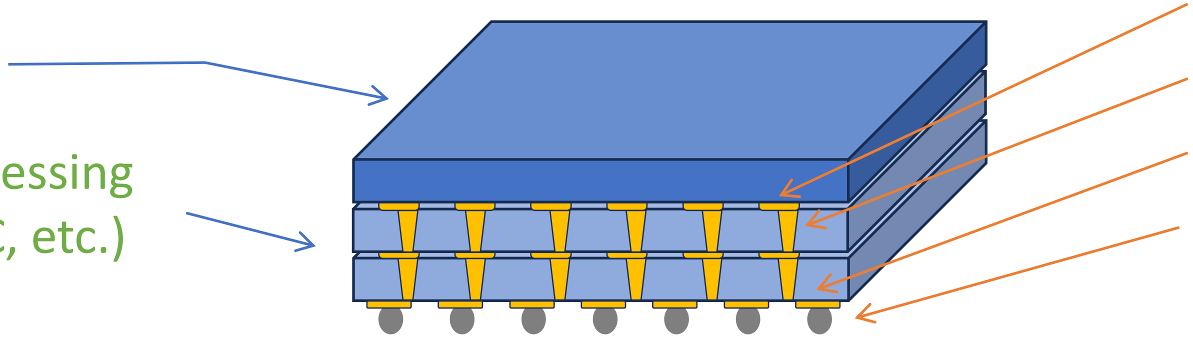

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Digital memory + processing
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UBM/bumping deposition

- Roadmap
  - Production of dummy structures (Si) with one/two metals for connection testing
  - *Establish* the process steps and procedures for 3D-ASIC integration
  - Perform comprehensive *mechanical & electrical characterization* of TSV/RDL processes
  - *Extraction of equivalent circuit*, layout design rules /PDK (optionally)

Integration of SiPh chip and optical fibers on detector module

- Establish the necessary process steps to ensure the long-term availability of the integration of silicon photonics (SiPh) chip with state-of-the-art monolithic/hybrid detector module

One/multi RDL layers for signals routing

Bump-bonding /interconnections

Optical fiber packaging (edge or grating couples) by automated/semi-automated procedure

Synergy with DRD7.1a (Jan’s slides)

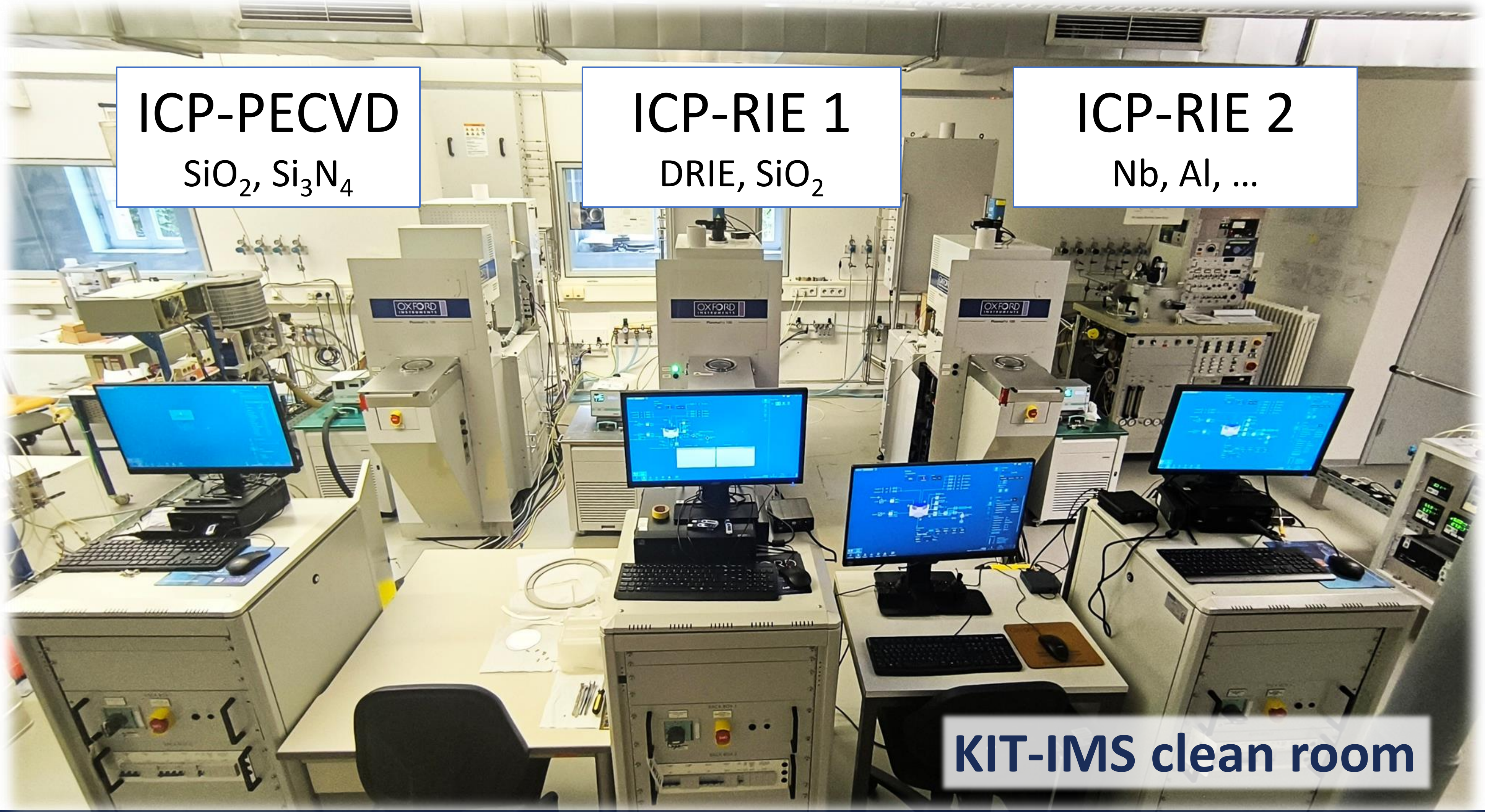
Progress report

- Infrastructures / machineries
- Technical

Three new machines from Oxford Instruments Plasma Technology

Installed and in operation

Courtesy: Mathias Wegner



ICP-PECVD
SiO_2, Si_3N_4

ICP-RIE 1
DRIE, SiO_2

ICP-RIE 2
Nb, Al, …

KIT-IMS clean room

Three new machines from Oxford Instruments Plasma Technology

Installed and in operation

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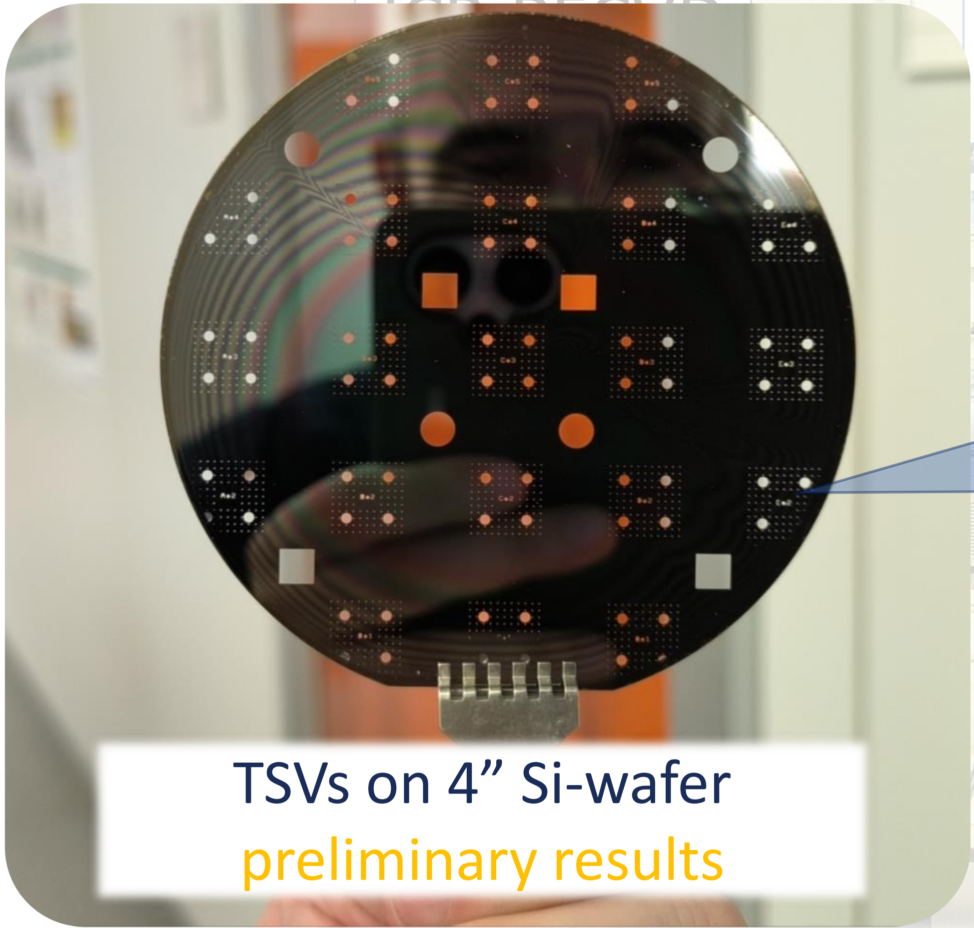
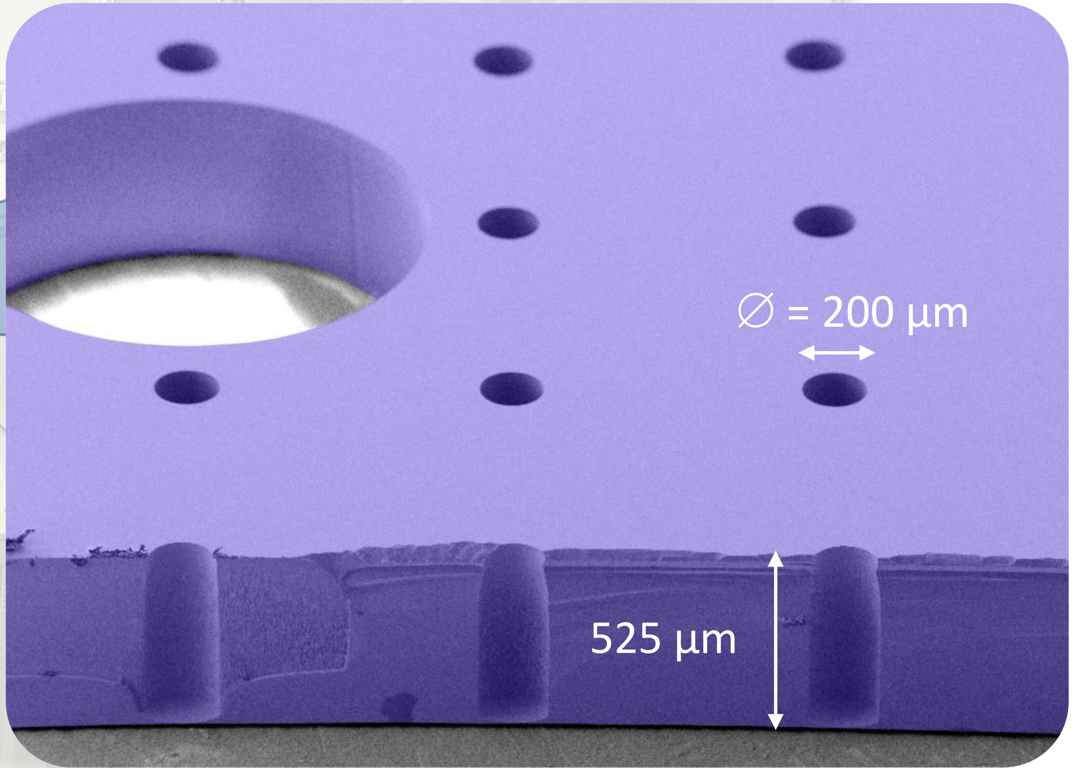
ICP-PECVD

ICP-RIE 1
DRIE, SiO2

ICP-RIE 2
Nb, Al, …



TSVs on 4” Si-wafer
preliminary results

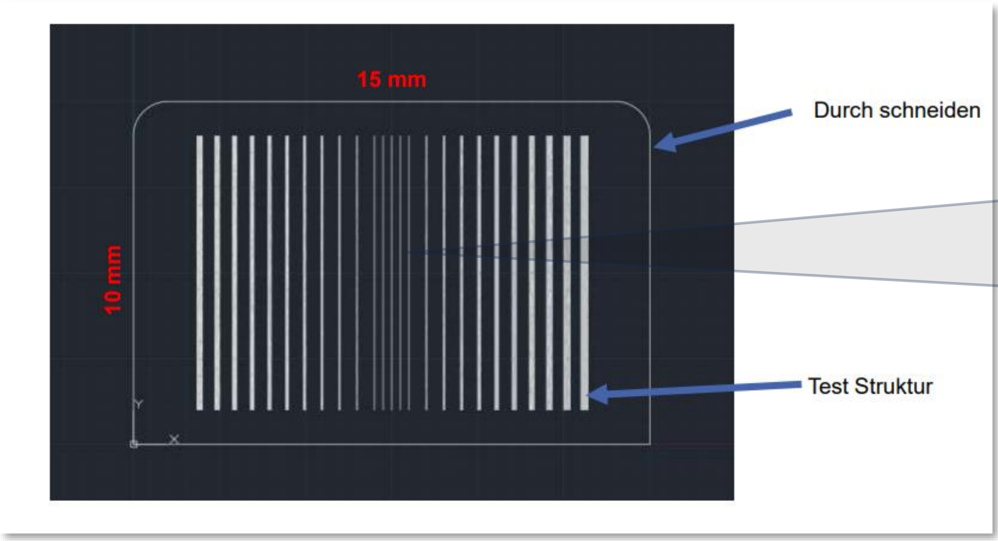


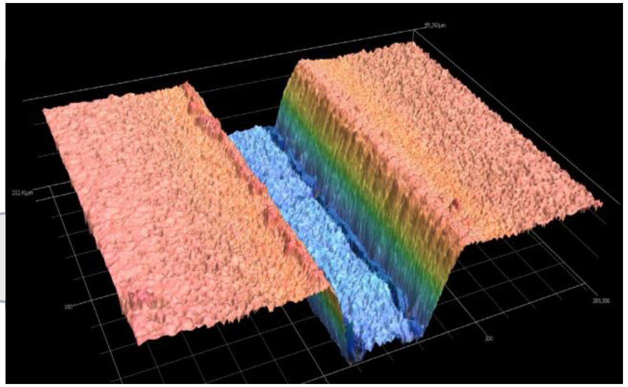
Laser drilled through silicon vias, maskless process for wafer and single die

Laser machine DR2000 from Photonic System

Courtesy: Felix Steiner and Thoms Blank

- Laser spot diameter: 20 µm
- Suitable for Si, glass, PCB
- Very large working area: 610 x 520 mm^2





To be installed at KIT

Strip structure 15 to 20 µm spacing

Laser drilled through silicon vias, maskless process for wafer and single die

Laser machine DR2000 from Photonic System

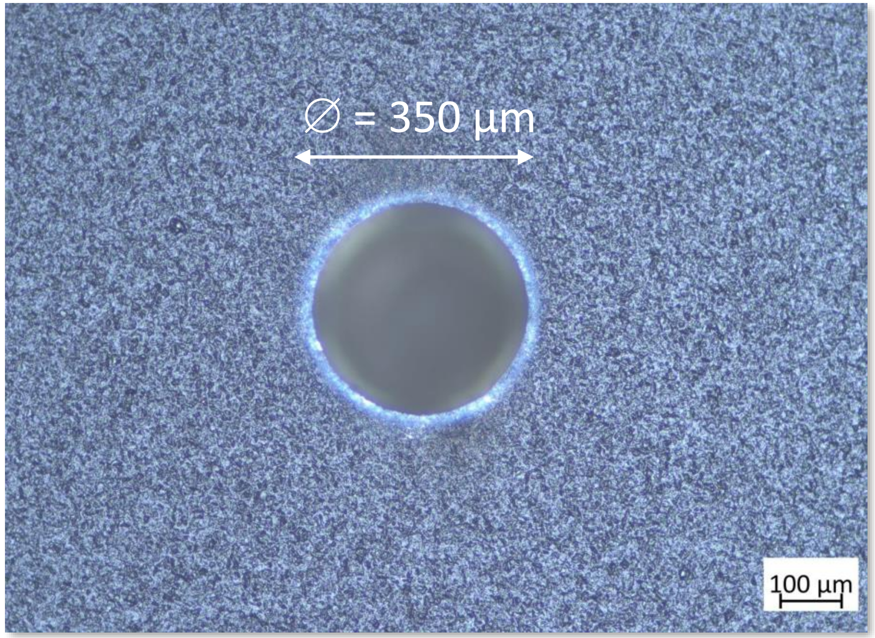
Courtesy: Felix Steiner and Thoms Blank

er: 20 µm

ss, PCB

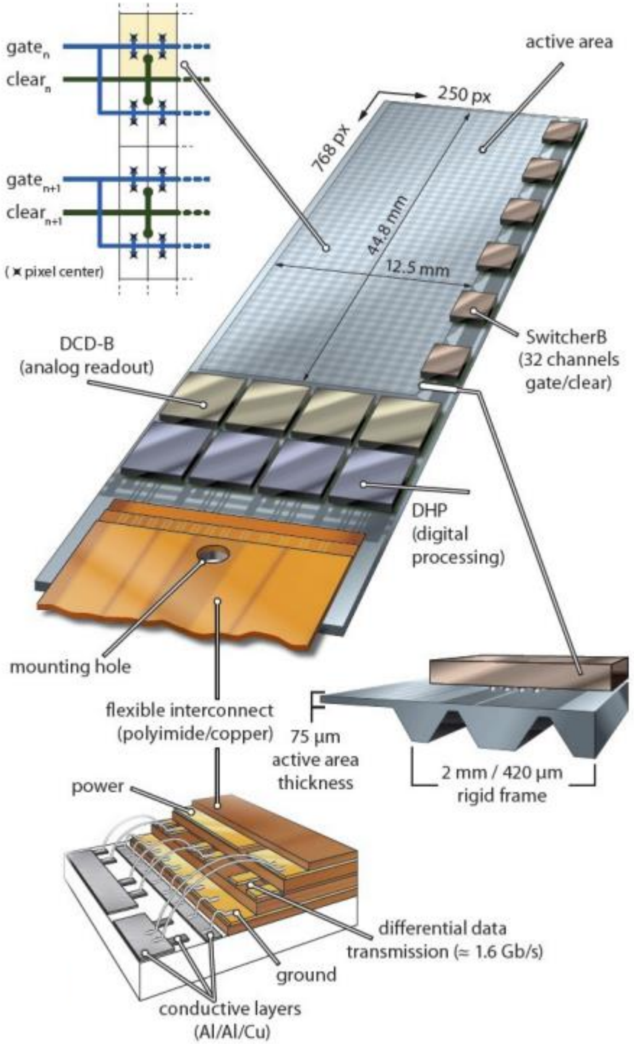
g area: 610 x 520 mm^2

Laser drilled TSVs (preliminary results)



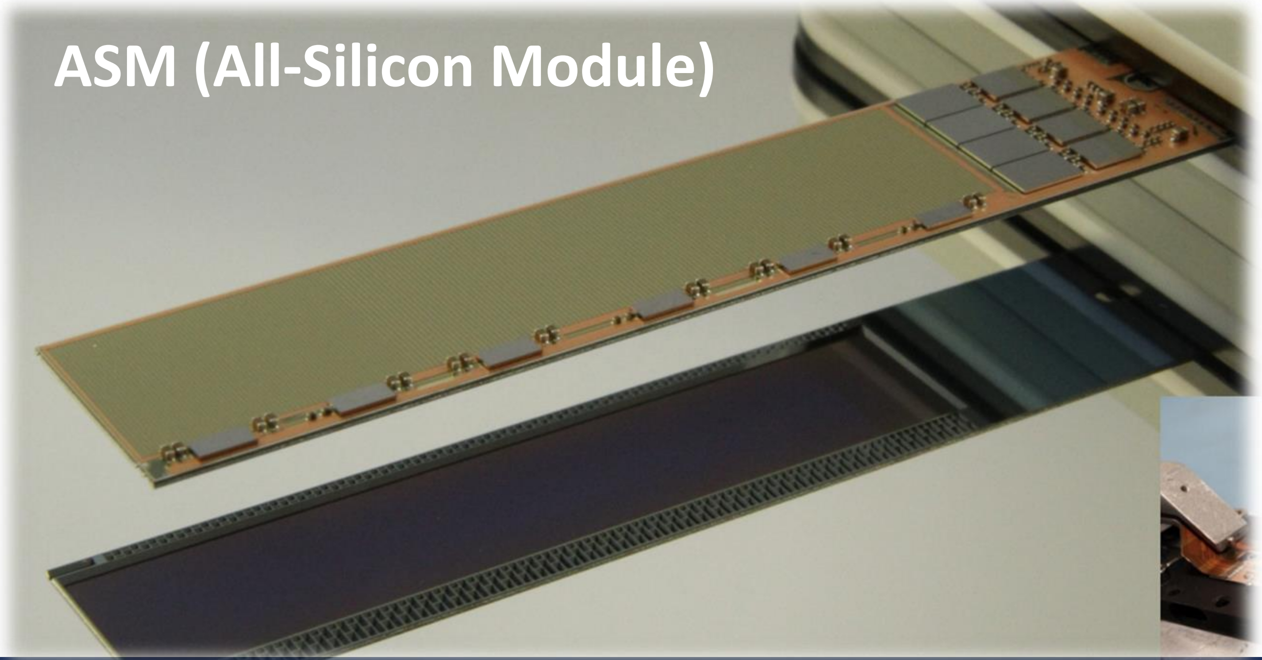
The DEPFET all-silicon module for Belle II PXD

Courtesy: Ladislav Andricek



Technology readiness level at MPG HLL

- Sensor employed as active interposer
- Routing based BCB/Cu RDL on sensor (up to 3 metal layers)
- ASICs bump-bonded on sensor (as a chiplet architecture)
- µ-channels cooling by DRIE and direct bonding (optionally)

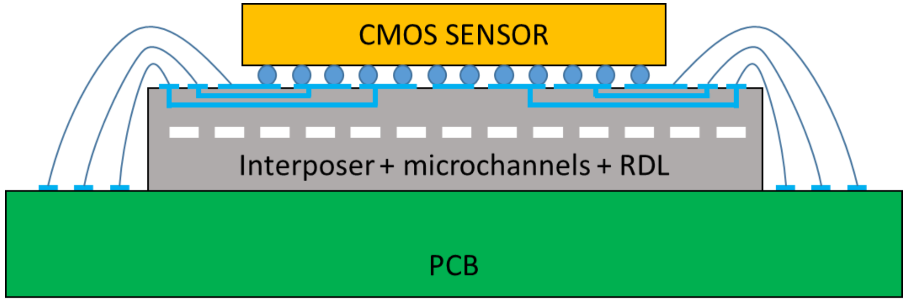

ASM (All-Silicon Module)

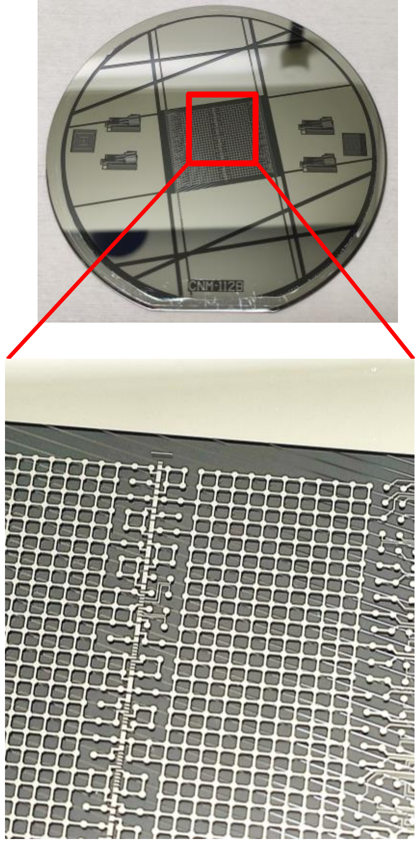
Centro Nacional de Microelectrónica CSIC

Active Interposers

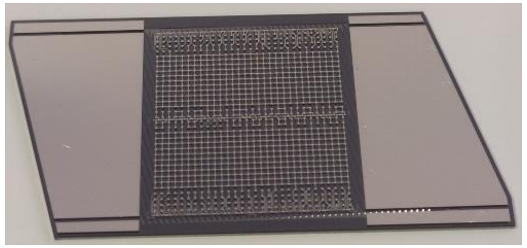
Courtesy: Miguel Ullan

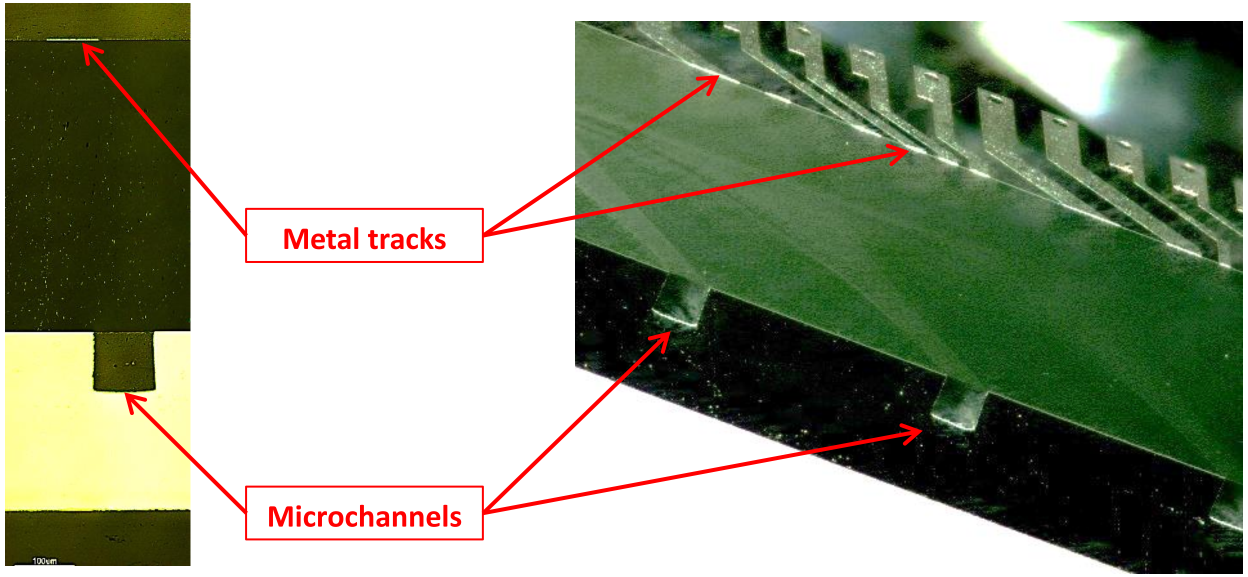
- Integration of µ-channels in silicon plates with redistribution layer (RDL)
  - Compatibilization of microchannel cooling fabrication with RDL metal routing
  - Signal and power distribution and cooling in the same silicon plate





Fabricated Silicon Plate

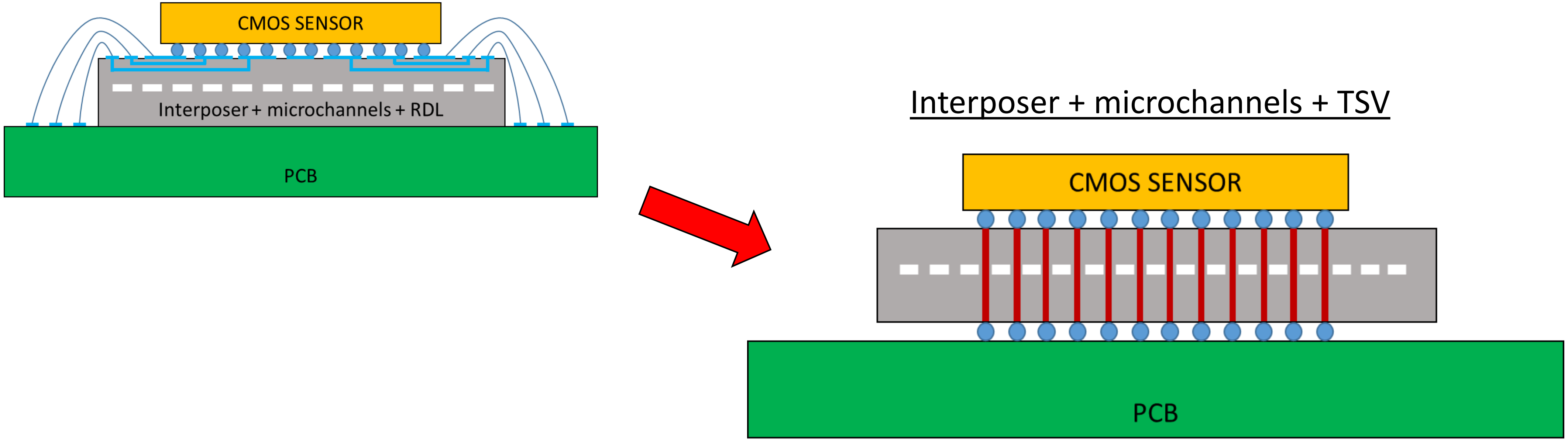




Future Developments

Courtesy: Miguel Ullan

- Redistribution layer improvements for better interconnection capabilities
  - ➢ Multilayer (2-3 layers)
  - ➢ Cu
- Interposers with TSV
  - ➢ Developing interposers with Through Silicon Vias (TSV) in order to improve the interconnection with the detectors
  - ➢ TSV development
  - ➢ Technological compatibility with microchannels in the same substrate



DRD7.6

Université de Sherbrooke TRIUMF

Contact person: Serge Charlebois Serge.Charlebois@usherbrooke.ca , *Fabrice Retiere* fretiere@triumf.ca

- Capabilities, technologies and their readiness level: Pratte et al., Sensors doi.org/10.3390/s21020598
  - Photon-to-Digital Converters (PDC, digital SiPM): SPAD, electronic readout, and 3D assembly
  - time-to-digital converters (TDC), embedded signal processing (framework nEXO experiment)
- Current R&D
  - Industrial fabrication by Teledyne DALSA (Bromont, Québec)
    - 150 mm diameter W2W bonding of SPAD onto CMOS readout, AlGe bonding TRL 3 / MRL 5
    - Frontside illuminated SPAD layer optimization TRL 4 / MRL 6
  - TSMC 180nm readout electronics, low power (techrxiv.171624070.00301513/v1) TRL 4 / commercial
  - To come: Design of a backside illuminated SPAD compatible with the PDC fabrication process
- Future R&D plans/activities
  - Migration of SPAD wafer diameter to 200 mm (led by Teledyne DALSA foundry)
  - Design of a 5×5 mm^2 readout in TSMC 65nm with TDC
- Contribution to DRD 7.6
  - Low power PDCs available to explore capabilities of the device
  - Codesign of a CMOS 65nm readout for the wafer production in 2029

TRL: technology readiness
MRL: Manufacturing readiness

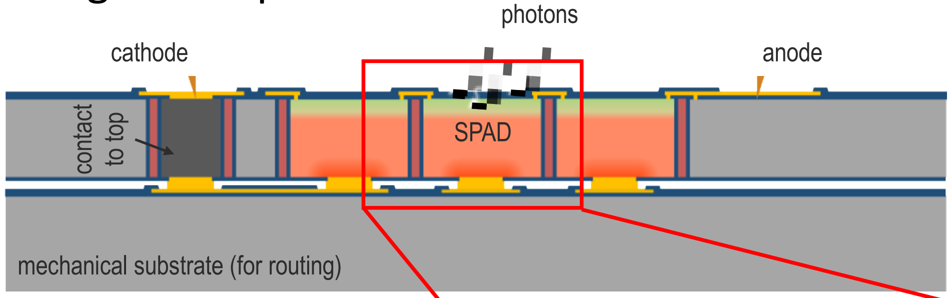
DRD7.6

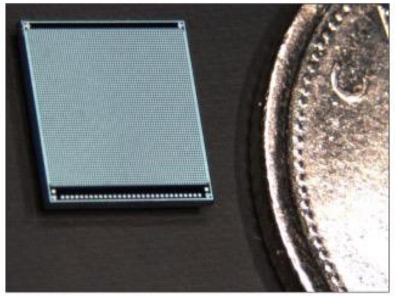
Université de Sherbrooke

TRIUMF

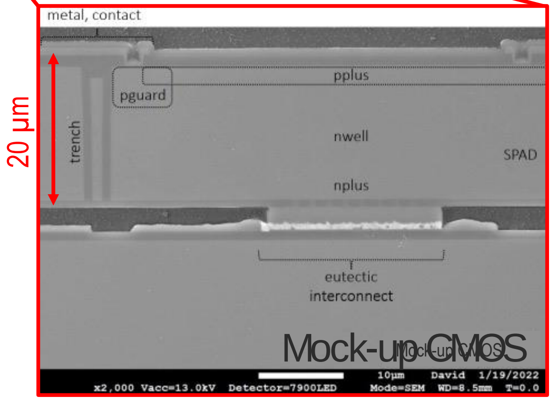
Contact person: Serge Charlebois Serge.Charlebois@usherbrooke.ca , *Fabrice Retiere* fretiere@triumf.ca

All 3D assembly critical gates passed:
proceeding to complete the first wafers of PDCs.





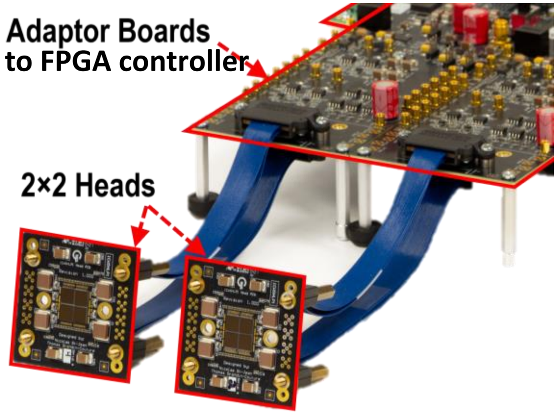
3D SPAD array
(canadian 10¢ for reference)

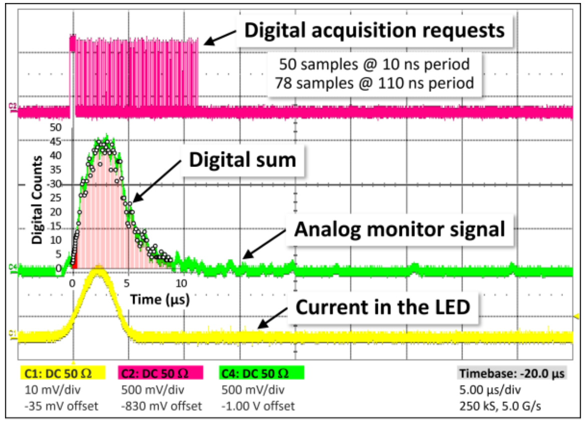


SEM cross section image

August 2024: 3 wafers successfully aligned and bonded

Small system prototypes functional. Waiting for full PDC

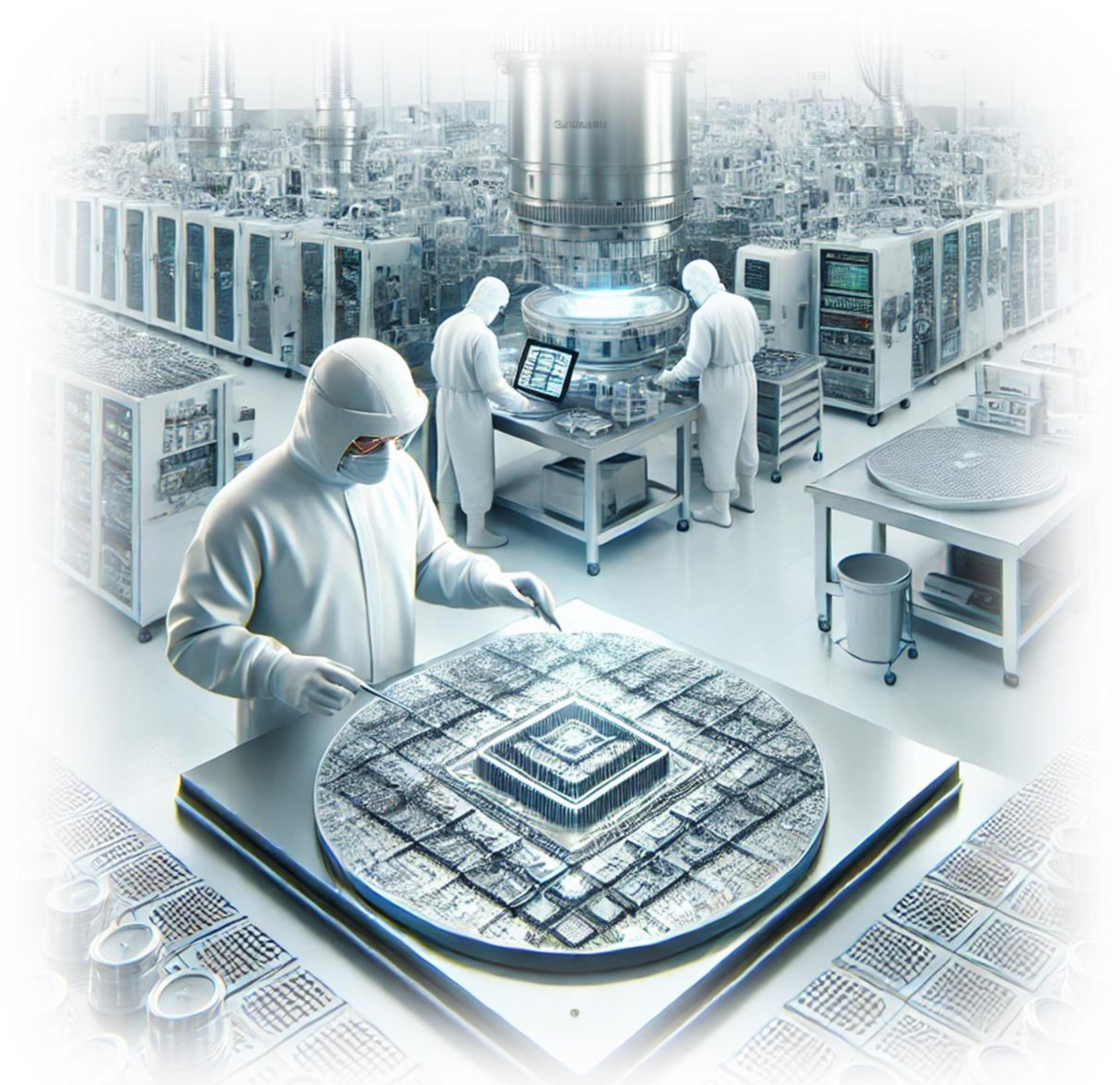




Large systems in development
for neutron imaging and spectral LIDAR

Conclusions

- Modern integration technologies and detector packaging rely on many processes: wafer dicing/singulation, metal deposition/UBM, bumping deposition, flip-chipping, wire- and tab-bonding, and many others. All these technologies are at a ***readiness level*** within the DRD 7.6b community
- A productive kick-off meeting on September 3rd, ***regular meeting*** is scheduled, the initial discussion will include the following points:
  - How to interface and collaborate effectively, identifying technologies at the readiness level
  - How to allocate tasks/processes, and how institutes could potentially benefit from the technologies available within the DRD 7.6b community
  - Identification of potential technologies/capabilities to be developed with a relevant impact factor in the detector community
- Maintaining a constant and productive connection with the DRD3 community is essential. Discussed with Giovanni Calderini, the opportunity to initiate a *new series of* ***seminars*** *focused on 3D advanced interconnection and photonic integration*



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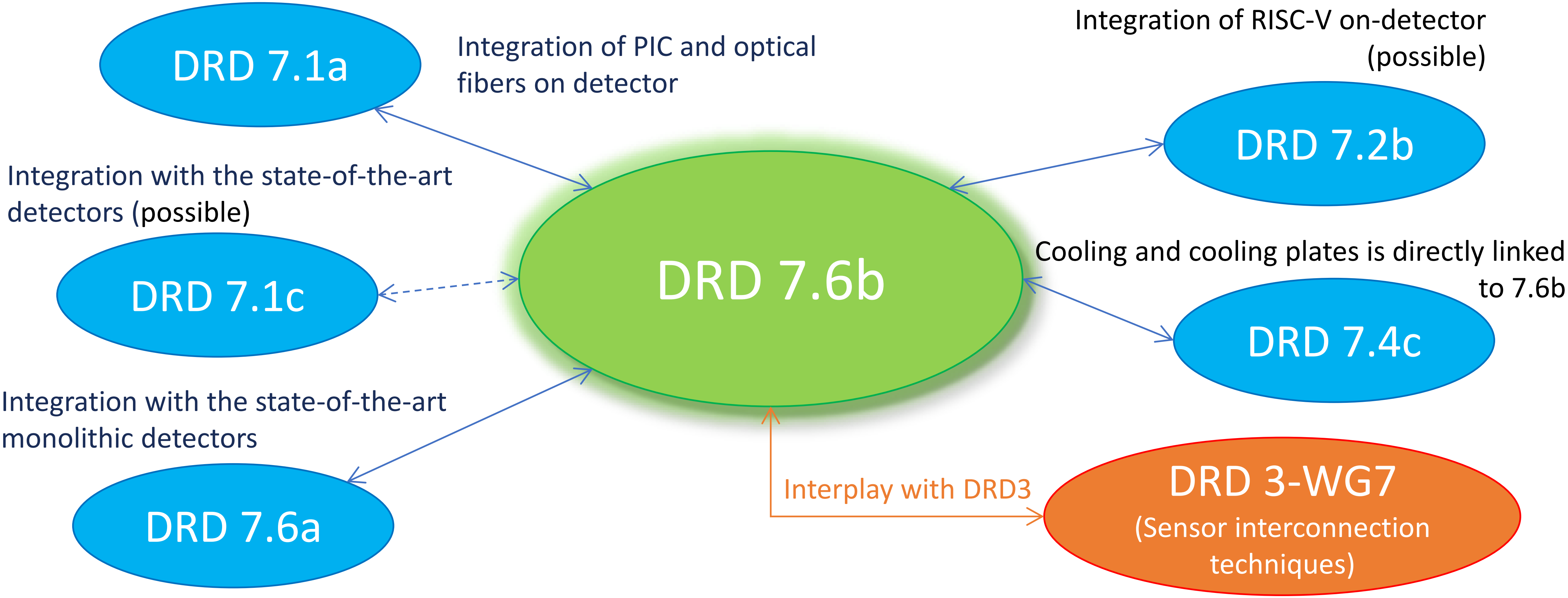
Thank you very much for your attention

Backup slides

Multi-disciplinary, cross-WP content

- Integration technologies plays a central role within DRD 7 and beyond



Interplay between DRD7.6b and DRD3-WG7

In agreement with Giovani Calderini

DRD 7.6b Development of fundamental integration technologies (i.e. 2D, 2.5D and 3D), includes:

- Maskless connection (in-house ACF/ACP)
- Bump-bonding by solder (in-house/industrial)
- TSVs and RDL for 2.5D and chiplet
- 3D integration (die- and wafer- levels)

DRD 7 (only)

Provides access to industrial wafer-level 3D integration

Provides the integration of SiPh chip and optical fibers on detector module

Provides integration of RISC-V and FPGA on detector module

DRD3 – WG7 More experiment oriented

- Requirements
- Request of new technologies

Examples of ongoing projects and collaborative work:

- TimeSpot hybridisation with conductive adhesives (Cagliari, Geneva U, CERN EP R&D)
- Timepix3 hybridisation with conductive adhesives (Geneva U, CERN EP R&D, Medipix)
- 100µPET (Geneva U, EPFL, HUG Geneva)
- MALTA (CERN EP R&D, Geneva U)
- ALICE ITS3 wafer-scale bent modules (Bari, Trieste, with other ALICE institutes)
- Timepix4 TSV bonding with ACF/ACP (Geneva U, CERN Medipix) and many others

DRD7.6

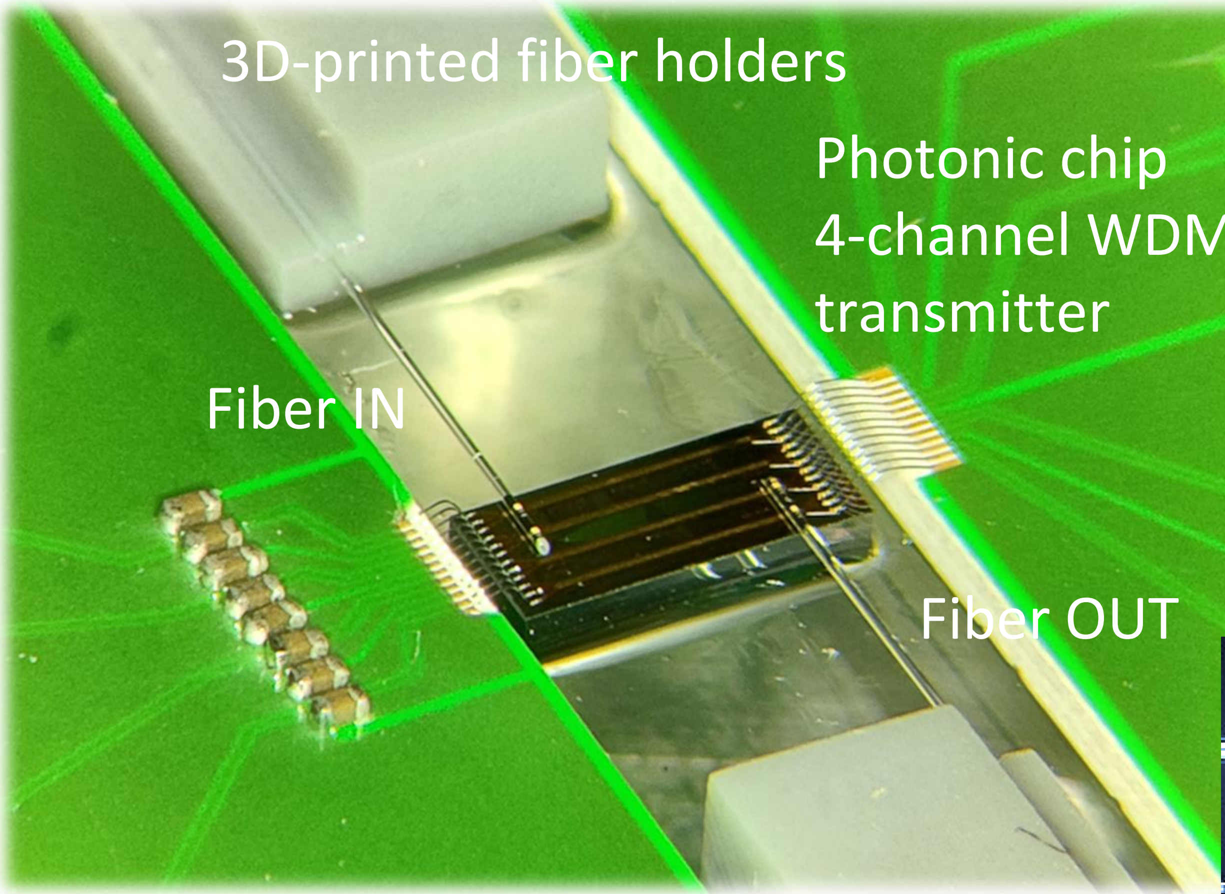
Contact person: Miguel Ullan miguel.ullan@imb-cnm.csic.es

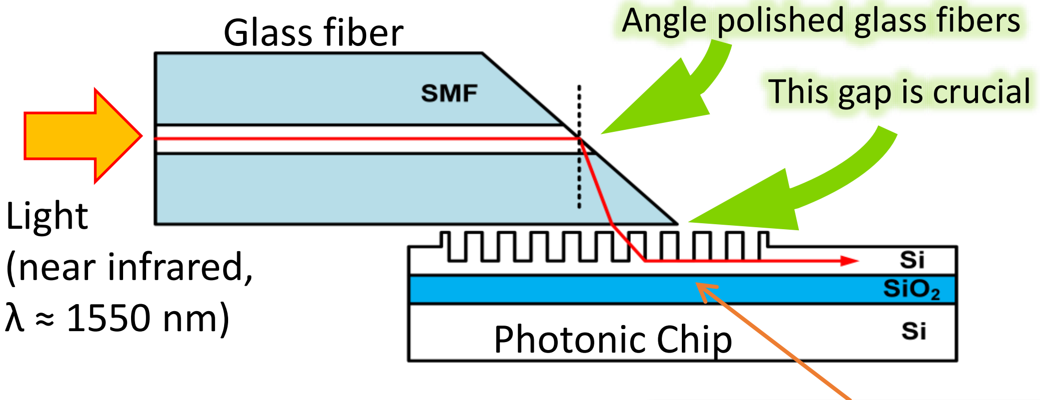
- Capabilities, technologies and their readiness level:
  - Micro-fabrication Facility with full sensor fabrication capabilities (Strip, pixel, 3D, LGAD, etc.)
  - Past work in the group on Embedded Pitch Adapters
  - Interposers with aluminium RDL on Si
  - Experience in wafer bonding technologies
- Current R&D
  - Active Interposers with microchannel cooling and RDL (framework AIDAinnova)
- Future R&D plans/activities
  - Development of TSV
  - Active interposers with TSV
- Contribution to DRD 7.6
  - Al & Cu RDL on silicon interposer
  - DRIE for deep silicon etching (micro-channel cooling and TSVs)
  - Laboratory for characterization (thermal probe station, X-ray tube, Alibava system)
  - Microelectronic Packaging Lab (Wafer dicing, wire-bonding, bump-bonding, ...)

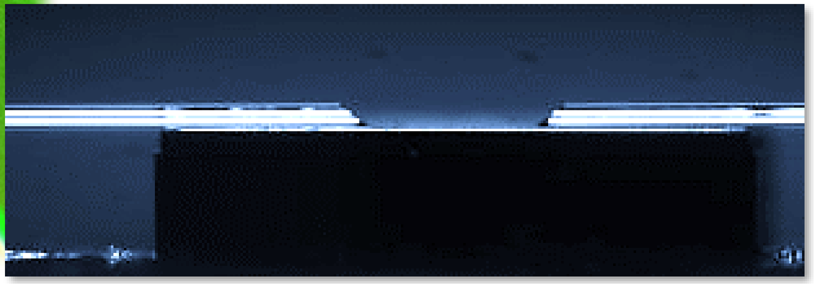
DRD7.6

Optical packaging

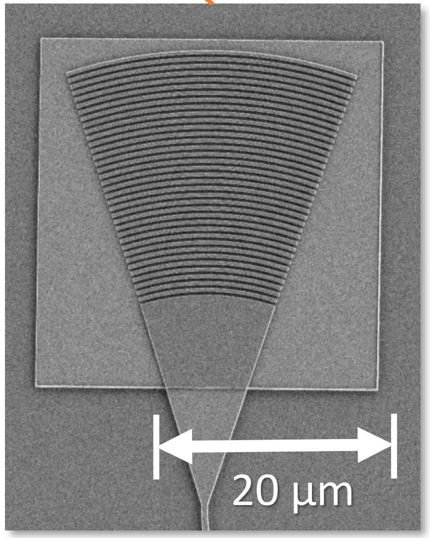
Courtesy: Marc Schneider







Grating coupler structure



For more details, Marc Schneider's talk at TWEPP 2024

Synergy with DRD7.1a (Jan's slides)