DRD 7.3a
High Performance ADC and TDC blocks at ultra-low power

Marek Idzik

On behalf of the DRD 7.3a project team

Project description

- Ultra-low power, area-efficient, fast Analog-to-Digital Converter (ADC) and precise Time-to-Digital Converter (TDC) are two indispensable blocks of a SoC-type readout ASIC
- The aim of DRD7.3a project is to develop a high performance ADCs and TDCs. In addition, other circuits directly interacting with them, such as analog front-ends, discriminators, fully differential amplifiers or serializers&data transmitters may be part of this project
- For HEP applications the technologies commonly adopted by the particle detector community, i.e. CMOS processes 130/65 nm and 28 nm are primarily used
- The performance of ADC/TDC block, mainly resolution and power, strongly depends on the technology used. One of the main goals for each block is a very good Figure of Merit, compared to state-of-art developments in the same technology

Organization - Members

AT: TU Graz

ES: ICCUB

Institut de Ciències del Cosmos
UNIVERSITAT DE BARCELONA

FR: CEA IRFU, CPPM, IP2I, OMEGA

KR: DGIST

PL: AGH

US: SLAC

Organization...

- By now two zoom meetings
  - 1st meeting January 2024
  - 2nd meeting last week (4/9/2024), https://indico.cern.ch/event/1449737/
- Project lead (temporarily)
  - Project lead – Marek Idzik
  - Deputy...

Proposed Milestones and Delvirables

M7.3a1 (M12) - Submission of ADCs and related blocks

M7.3a2 (M12) - Submission of TDCs and related blocks

M7.3a3 (M24) – Tests of ADCs and related blocks

M7.3a4 (M24) - Tests of TDCs and related blocks

D7.3a1 (M36) – Demonstrator ADC ASICs

D7.3a2 (M36) - Demonstrator TDC ASICs

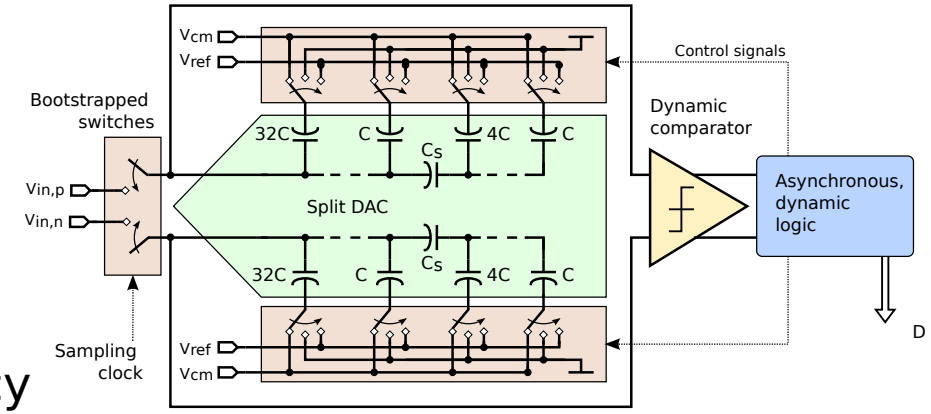
Progress Report

- Update on ongoing activities of different groups presented during last zoom meeting 4/9/2024
- Quick flash of recent results is given – not all activities of different groups are shown here
- R&D in different groups are done in frameworks of different projects – not only DRD7.3a
- Resources – more complicated – no statements yet...

Progress Report - AGH

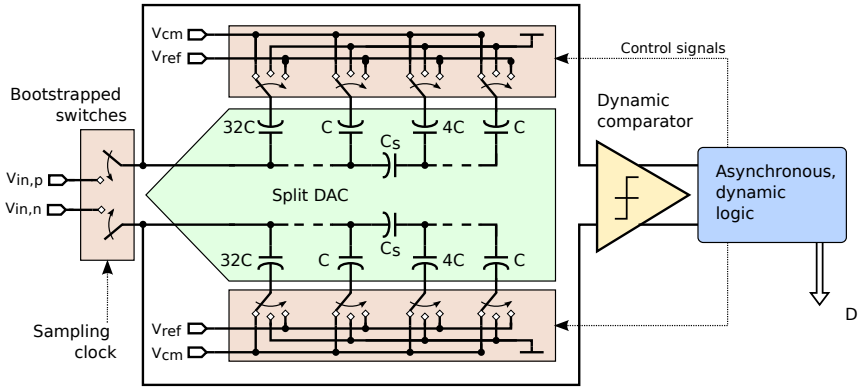
R&D on 10-bit ADC in 130nm with internal threshold

- Existing 10-bit SAR ADC consumes 680uW@40MSps & works <= 50MSps
- To decrease power consumption even further, additional internal threshold is added - to make a full conversion only for signal and not for noise
  - In worst case 2 additional comparisons are added
- The modified ADC is a bit slower, but
  - Estimated power for low occupancy ~ **one third of the current one**
- Schematic done, layout advanced, submission in close future...

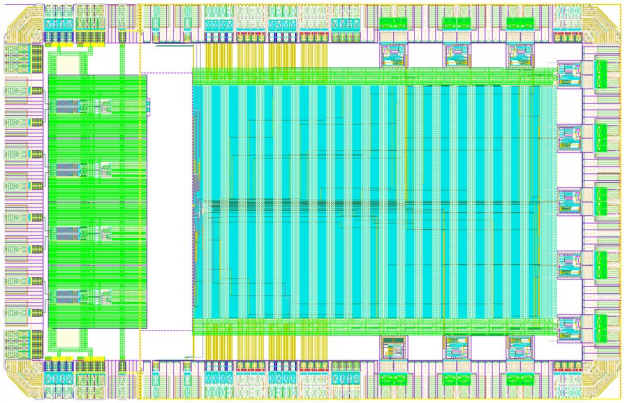


Progress Report - AGH

R&D on fast ultra-low power 10-bit ADC in 28nm



SAR architecture already verified in 130/65 nm



4-channel ASIC, one channel 279um x 110um

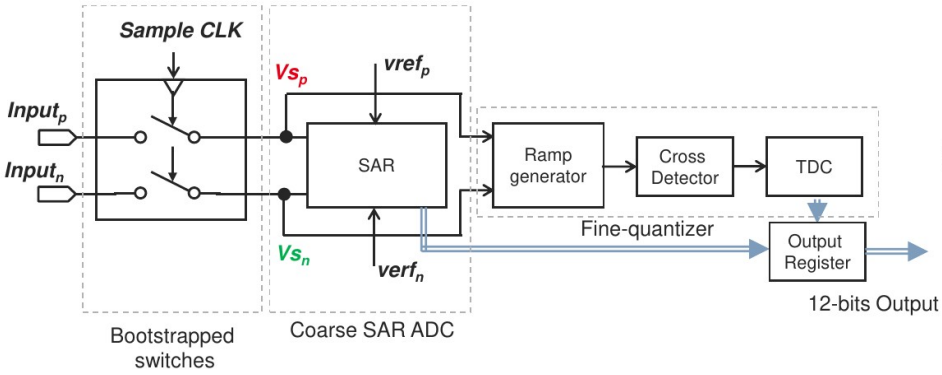
- The Goal – ultra-low power and the highest sampling rate
- MiniASIC submitted July 2024

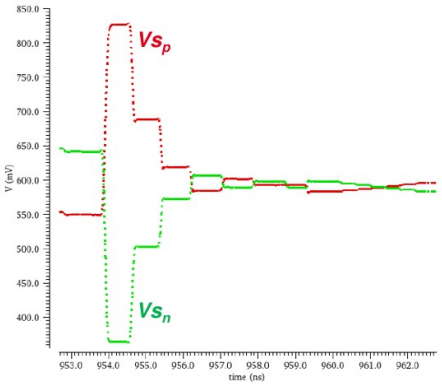
CMOS [nm]	Verification	Power@40MHz [uW]	Max Fsample [MHz]	
130	Prototype ASIC	680	50	M. Firlej et al. JINST 18 P11013 (2023)
65	Prototype ASIC	440	50-60	M. Firlej et al. JINST 19 P01029 (2024)
65	Prototype ASIC	~550	80-90	M. Firlej et al. JINST 19 P01029 (2024)
28	Post-layout simulation	<150 ?	~180 ?	

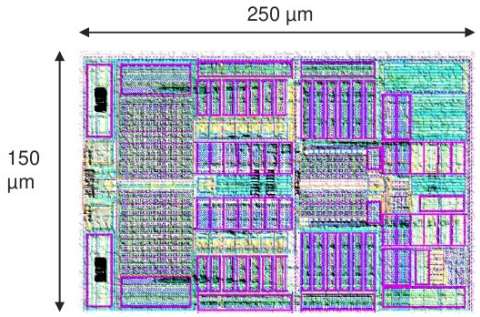
Progress Report – CEA IRFU

R&D on 12-bit ADC in 65nm

Motivation — Achieve high resolution, low power with a fairly fast sampling (> 40 MHz) rate for multichannel chip design.
We are exploring an architecture : TDC-assisted SAR ADCs







Design for multichannel ASIC with pitch 150 µm (ADC core + some decoupling) on DNW

Simulation performance summary

Parameters	This work
CMOS [nm]	65
Architecture	TDC-assisted SAR ADCs
Supply voltage [V]	1.2
Resolution [bit]	12
Input range [V]	0.98
Conversion rate [MS/s]	up to 60
DNL	0.47
Dynamic ENOB	10.34
Power [mW]	0.9 mW @ 50 MHz
Core area [mm²]	0.0375

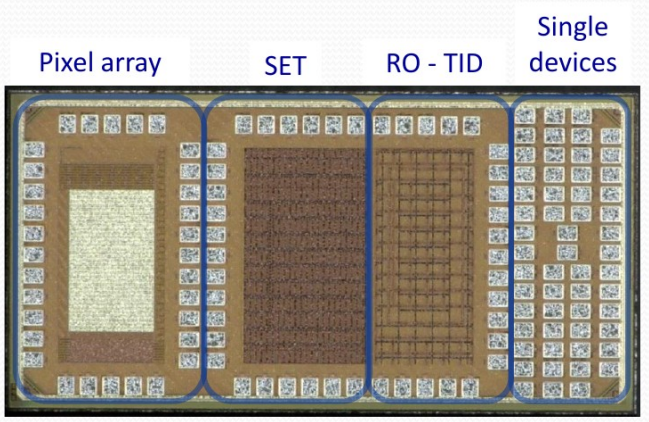
Calendar:

- The prototype was submitted on April 24 (die with other developments) and returns end of September 24
- First measures can be taken on October 24

Progress Report - CPPM

R&D on hybrid pixels with time measurement in 28nm

- The **radiation tolerance** of the 28nm process up to 1-2 Grad
- **Time measurement** with a resolution better than 50ps
- Small pixel size -> **25µm × 25µm**

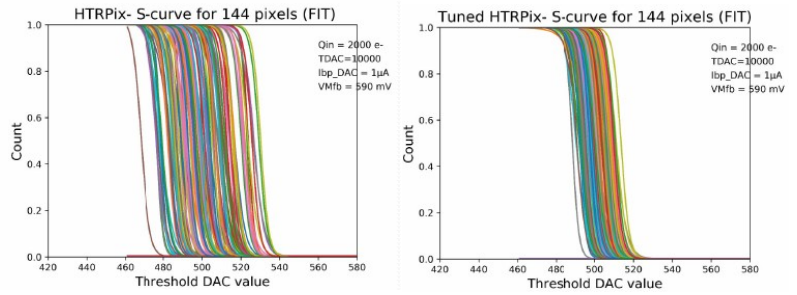


Mini@sics of 2×1 mm2 received June 2023, with 4 main blocks
Array of 12×36 pixels (432 pixels)
- Analog pixel array with Fast charge amplifiers for high time resolution
- Only the analog part is implemented (25×12 µm2)

SET test structures
- Measure the SET pulse width with a good resolution < 20 ps

Ring Oscillators for TID tests on digital standard cells
Test structures for TID tolerance studies

Threshold tuning

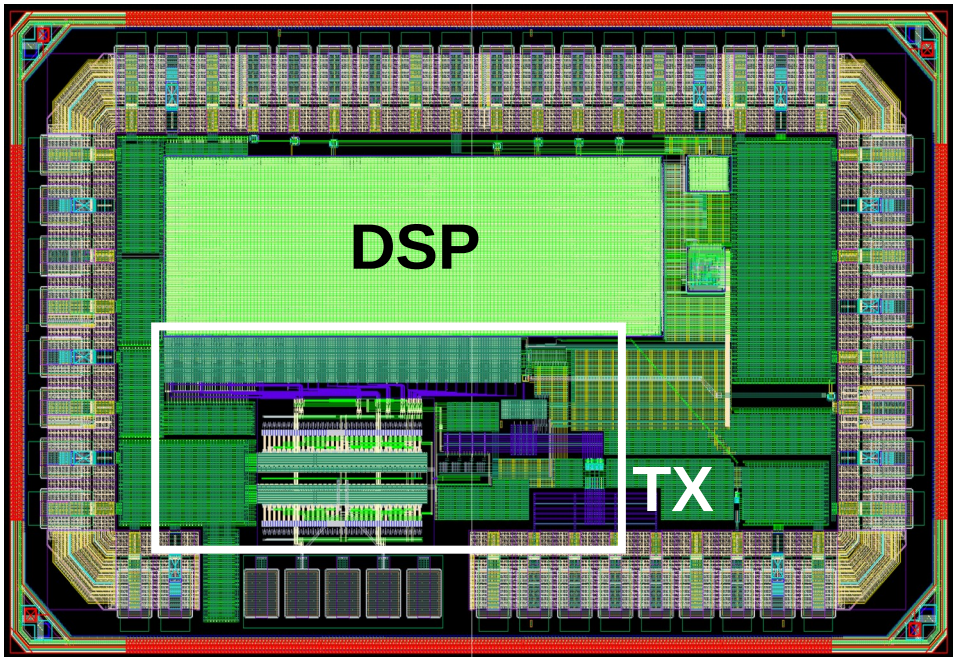


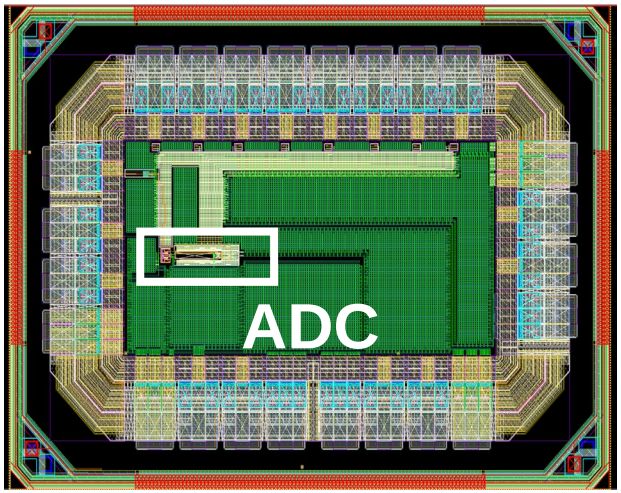
Continuation of the project
- Functional tests to be finalized October 2024
- Irradiation tests the end of 2024
- A new 28 nm design focused on pixel array :
  - TDCs for time measurements
  - Possibility to be bump bonded with sensor array
  - Use of CERN PDK makes the design more manageable
  - Prototype submission scheduled for Q1-2 2025

Progress Report - DGIST

R&D on high speed ADC and TX in 28nm

TSMC28nm CMOS Tapeout (2024.08)



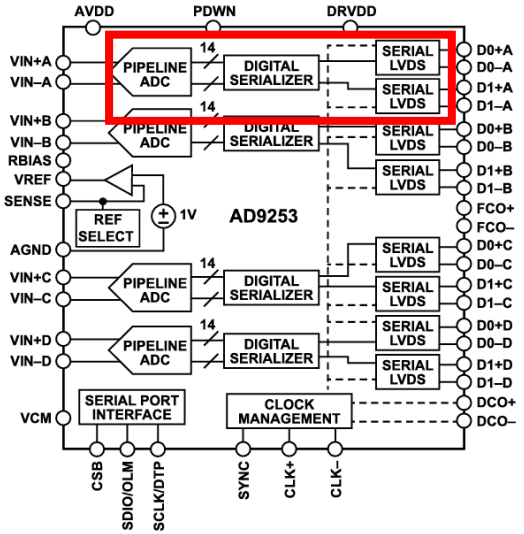


- Post-layout simulation shows >500MS/s (@ 8-bit) with >7 ENOB, 6-to-8 bit (variable) conventional SAR ADC
- 40Gb/s PAM-4 DAC-based transmitter (20GS/s 8-bit DAC) (post-layout sim)

Progress Report - DGIST

R&D on high speed ADC and TX in 28nm

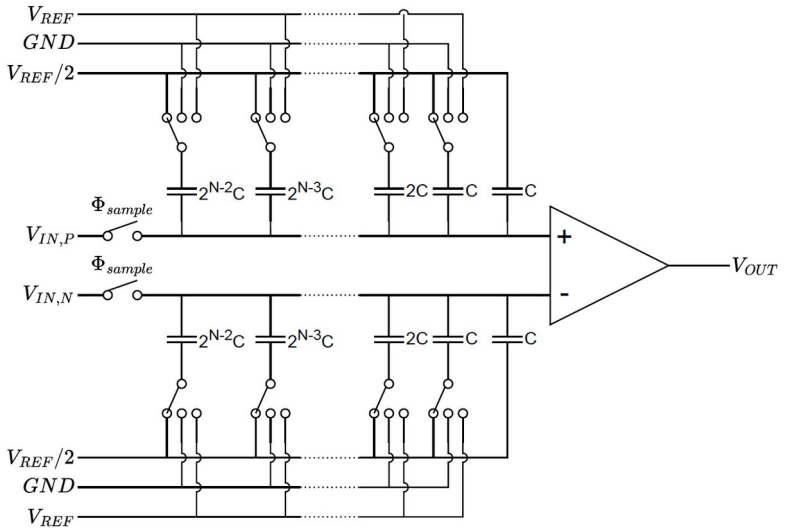
- Planned TSMC28 HPC+ RF shared block runs
  - 2024.12:
    - 8-way-interleaved 8GS/s 8-bit TI-SAR-ADC (asynchronous SAR)
    - Single slice loop-unrolled 8-bit SAR
    - 32Gb/s short-reach transmitter test chip
  - 2025.05:
    - 64-way-interleaved 64GS/s 8-bit TI-SAR-ADC (asynchronous SAR)
    - (Revision version of 2024.08 tapeout): 8-bit DAC-based 40Gb/s PAM-4 TX



Progress Report - ICCUB

R&D on 12-bit SAR ADC and 25ps time bin TDC

- 12-bit SAR ADC
  - Started 10 months ago
  - Verified physical design expected by the end of 2024



- 25ps time bin TDC
  - Started 1 month ago
  - Using a previous TDC design (based in a PLL) as starting point (25 ps time bin)
    - → Goal: understanding how to improve power, jitter and linearity using the same (or similar) architecture
  - Verified physical design: tbd

Progress Report - ICCUB

R&D on 12-bit SAR ADC in CMOS 65nm

- Digitized readout to measure the detected energy of
  - High energy physics experiments (LHCb [1])
  - Medical imaging applications (PET imaging [2])
- Expected ADC performance
  - Precise measurements resolution 12-bit
  - Very high speed > 40 MSps
  - High channel density channels > 16
    - → Very low power < 1mW/ch

Progress and Status

- ADC main blocks
  - SAR digital controller
    - → Schematic verified across corners
  - Latch voltage comparator
    - → Schematic verified across corners and with transient noise
  - Capacitive DAC
    - → Schematic verified across corners
    - → Layout floorplan defined, **currently** integrating the block and optimizing parasitic capacitances
- ADC performance
  - SAR digital controller
    - → Meets timing requirements, does not affect the resolution, and consumes < 0.1mW/ch
  - Latch voltage comparator
    - → Meets timing & resolution (ENOB > 11.5 bits) requirements, and consumes ≈ 0.1mW/ch
  - Capacitive DAC
    - → With initial post layout simulations, meets timing & resolution (ENOB > 11.5 bits) requirements

Progress Report - IP2I

R&D on TPSCo 65nm MCMOS sensors with high-prec. timing

Interest and proposed contributions in DRD7.3

- Investigate Novel Readout Architectures for Pixel Matrix Sensors:
  - Objective: Evaluate and optimize readout architectures to leverage the high precision features of the sensor and the on-chip Time-to-Digital Converter (TDC)
- TDC Architectures Investigated (TPSCo 65 nm):
  - Investigate two TDC architectures to be integrated within a pixel matrix: optimize both area and power consumption
    - Vernier Ring Oscillator TDC
    - Free-Running Delay Line TDC
  - Depending on power consumption and area constraints of the sensor, we may contribute to the design of key components such as FFE, discriminators, and SLVS transmitters…

Progress Report - OMEGA

Implementing ADCs and/or TDCs in multichannel chips

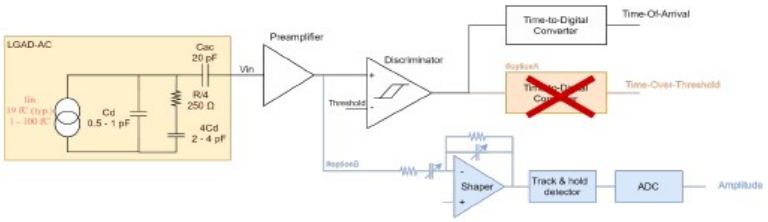
OMEGA has been collaborating with other groups developing complex chips containing ADCs/TDCs

- HGCROC 78 channels - collaboration with AGH, CEA, CERN, Imperial
- ALTIROC 15 x 15 pixels - collaboration with AGH, CERN, LPCF, SLAC
- HKROC 36 channels - collaboration with AGH, CEA, CERN, Imperial

EICROC0 : one pixel overview

Omega

- One pixel design
  - Preamp, discri taken from ATLAS ALTIROC
  - I2C slow control taken from CMS HGCROC
  - TOA TDC adapted by IRFU Saclay
  - ADC adapted to 8bits by AGH Krakow
  - Digital readout : FIFO depth 8 (200 ns)
- 5 slow control bytes/pixel
  - 6 bits local threshold
  - 6 bits ADC pedestal
  - 16 TDC calibration bits
  - Various on/off and probes

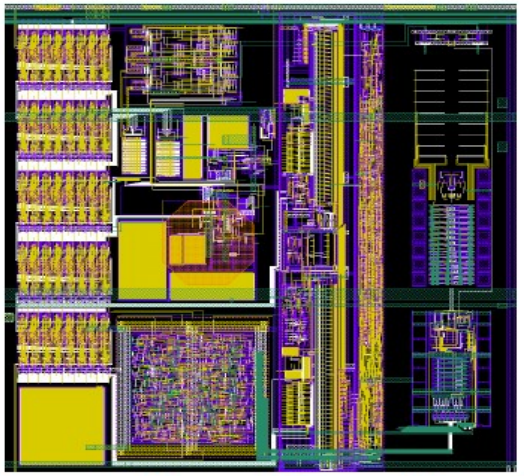


EICROC ePiC meeting 9 jan 2024

OMEGA Microelectronics

Irfu

AGH



Slow control | PA +discri | TOA TDC | 8b 40M ADC

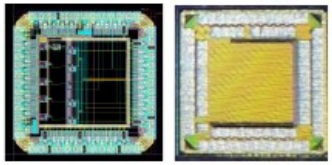
Progress Report - SLAC

R&D on high precision TDCs

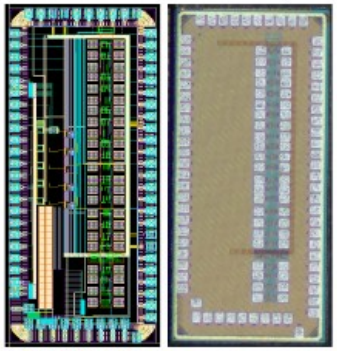
	TDC metrics
Technology	28nm
Timing resolution	6.25ps (TOA) / 50ps (TOT)
Time depth	1.6ns (8bit / 5bit) easily extendable by simple addition of bits to the counter
TDC core area	19µm x 44µm
Power consumption	(average, 25ns conversion cycle / bunch crossing)
10% occupancy	16µW
1% occupancy	2.5µW

28nm TDC Prototype ASIC – Test Setup

v1 (submitted Jan. 2023, issues with wire-bounding):



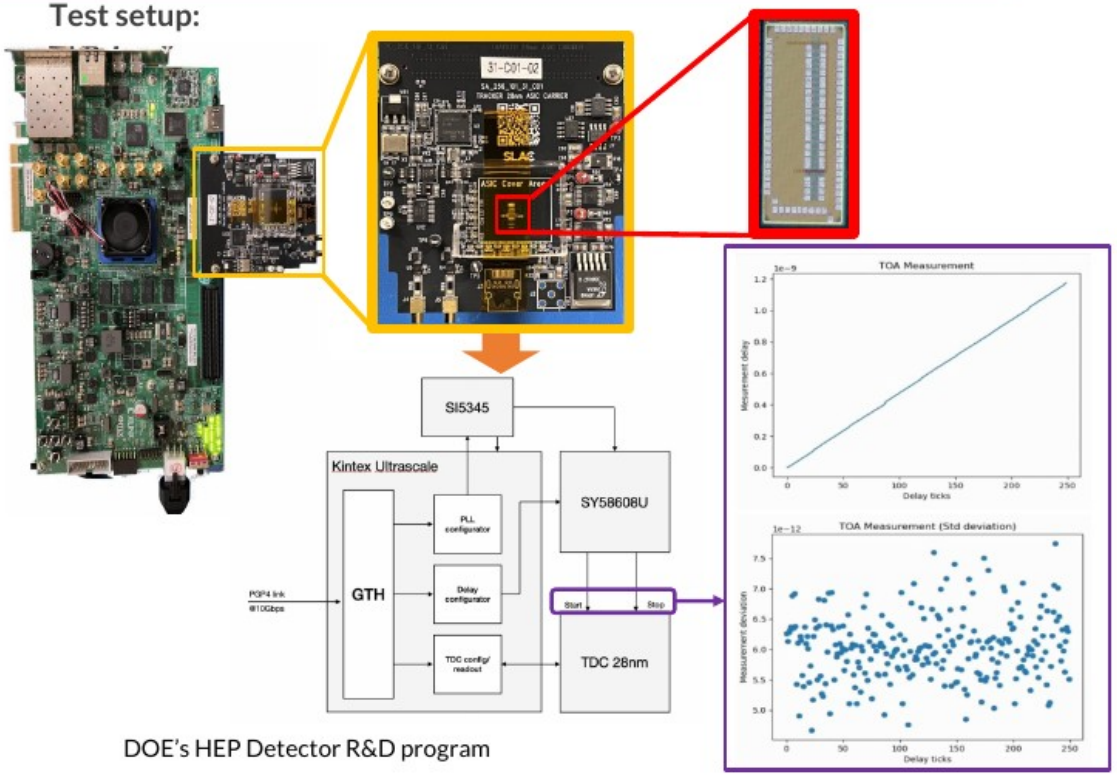
v2 (submitted Jan. 2024, received end of Jun. 2024):



*ASICs employ low-jitter RXs courtesy of Carl Grace (LBNL)

SLAC TECHNOLOGY INNOVATION DIRECTORATE | INTEGRATED CIRCUITS DEPARTMENT

Test setup:



DOE's HEP Detector R&D program

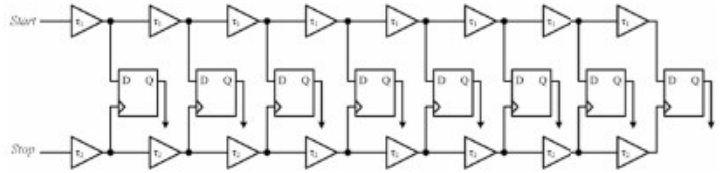
Progress Report - SLAC

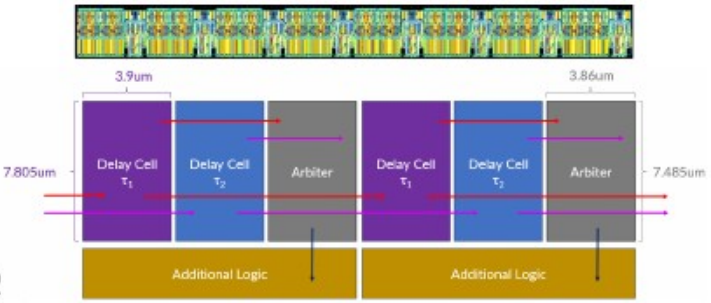
R&D on high precision TDCs

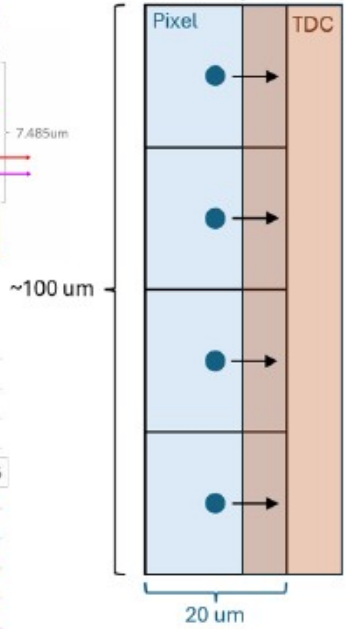
65nm TDC for MAPS

- HEPIC Summer Student (Megan Zeng, Sanford University)

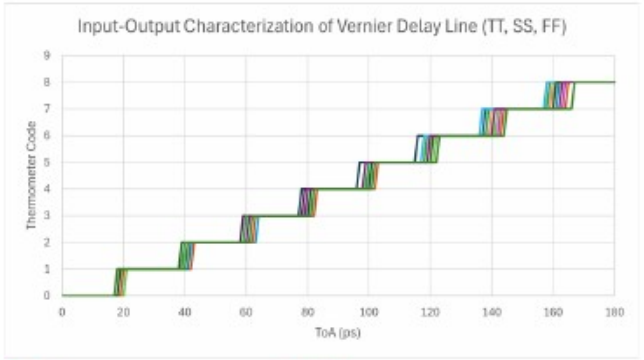
Vernier Delay Line

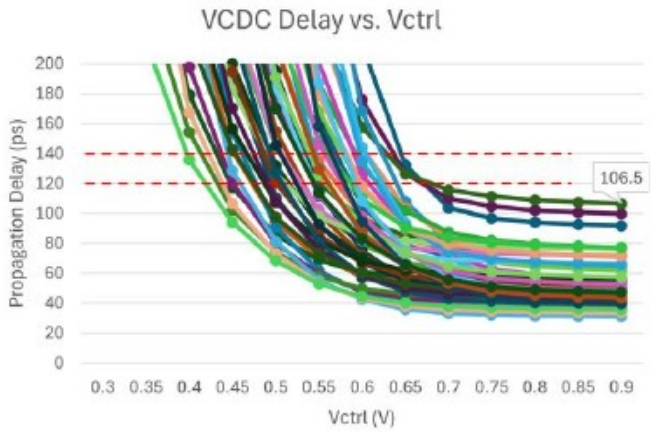






- 8 delay cells with respective delays of 140ps and 12 tuned by adjusting control voltage

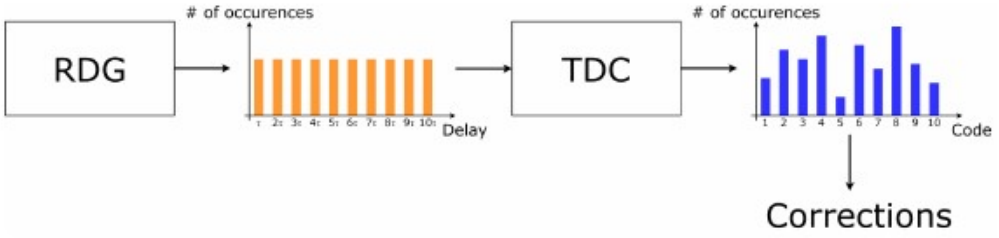




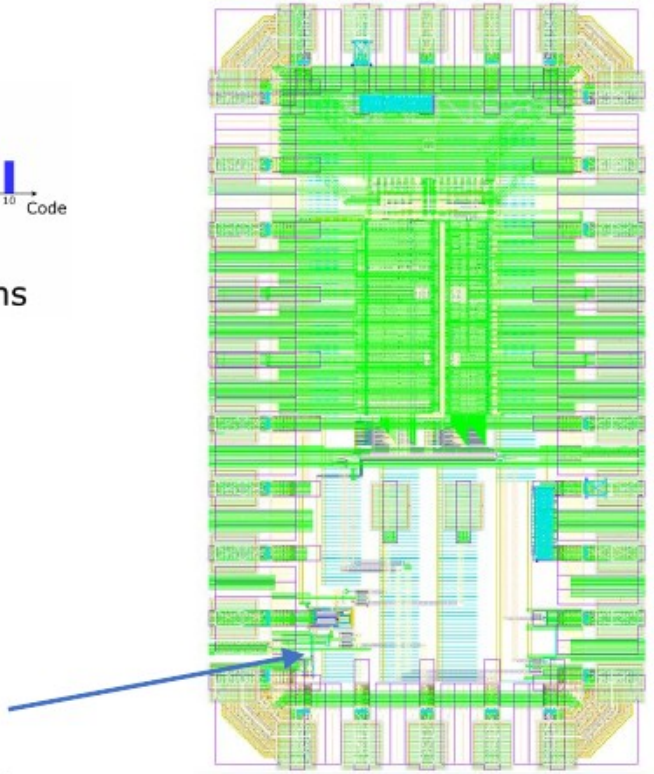
Progress Report – TU Graz

R&D on circuit reliability and RTN influence in 28nm

Random Delay Generator – for histogram calibration



Parameter	Specification	Design
Process	TSMC28nm	
Supply voltage	0.9 V	
Minimum delay	as small as possible	0.7 ns
Maximum delay	25 ns	40 ns
Delay resolution	< 20 ps	< 2.87 ps
Delay distribution	Uniform	Almost uniform (typ.)
Power consumption	as small as possible	300 μW
Area	as small as possible	1350 μm^2



Submitted in July 2024 run

Design: Marvin Lackner

Summary

- The work is ongoing in all contributing groups!
  - designs will be / have been submitted or prototype blocks are already under tests
- The mainly developed blocks are ultra-low power and/or fast 8-12 bit ADCs and sub10-50 ps resolution TDCs. All commonly adopted in HEP CMOS processes, namely 130nm, 65nm and 28nm are used

Thank you for attention