DRD7: Cooling plates

On behalf of the DRD7.4c collaborators

DRD7.4: EXTREME ENVIRONMENT AND LONGEVITY

IMPLEMENTING DRD7:
AN R&D COLLABORATION ON ELECTRONICS AND ON-DETECTOR PROCESSING

Oscar Augusto de Aguiar Francisco (The University of Manchester)
oscar.augusto@cern.ch

Cooling and cooling plates

B.4.3 Project 7.4c: Cooling and cooling plates

This project focuses on the development of the next generation of cooling plates for front-end electronics and sensors based on different materials/techniques. The main goal is to explore manufacturing techniques while improving electronics integration with a cost-effective solution. This project groups different topics covered by different collaborations which will be presented in the coming sections.

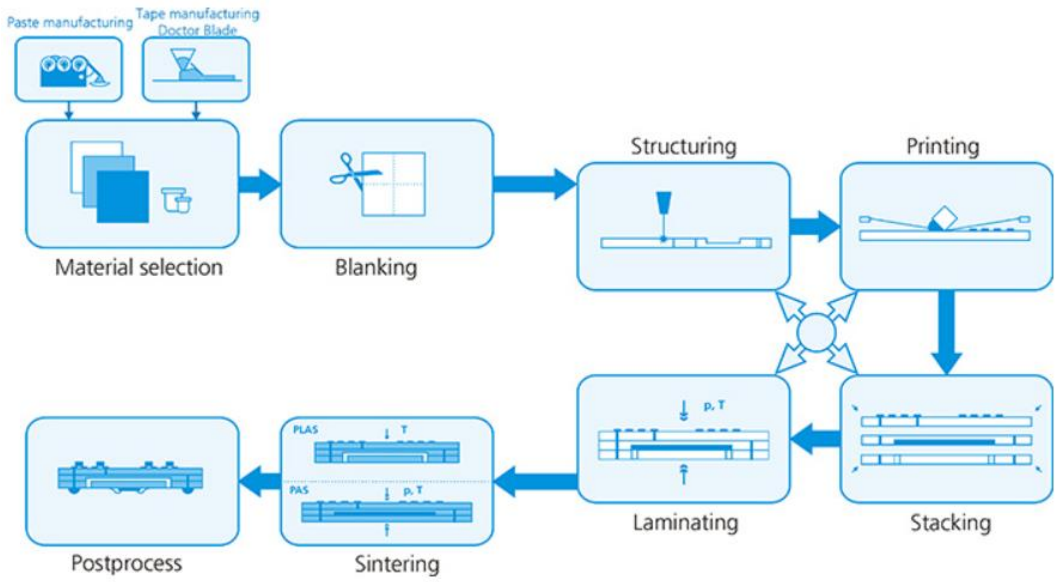
Note that depending on the evolution of the forming DRD8 Collaboration, some cooling-related projects may be best integrated in DRD8. This will be fine tuned in due-time to best match the needs of the projects.

Project Name	Cooling and cooling plates (WG7.4c)
Project Description	Development of the general purpose next generation of microchannels cooling structures to deliver excellent cooling performance, minimal material budget, and better electronics integration. Duration about 2+ years.
Innovative/strategic vision	Better integration of electronics features to the cooling plates especially in dense electronics applications. Better scalability considering alternative manufacturing techniques (more cost-effective). Thermal performance numerical simulation tools for new applications.
Performance Target	Different topics will explore different combinations of the following parameters: power dissipation (up to $2W/cm^2$), material budget ($\leq 0.5\%X_0$), integration and/or cost. Different experiments will be able to profit from the portfolio created and optimize those solutions for their final application. The progress will be tracked via public reports in the form of presentations, public notes and/or papers.
Multi-disciplinary, cross-WG content	Communication with DRD8 (Mechanics) and DRD3 (Semiconductor detectors) via liaisons and workshops (e. g.: Forum on tracking mechanics) and 7.6b project (common access 3D and advanced integration) within the DRD7.
Contributors	CERN DE: DESY ES: IMB-CNM, IFIC-Valencia UK: Manchester FR: French Collaboration

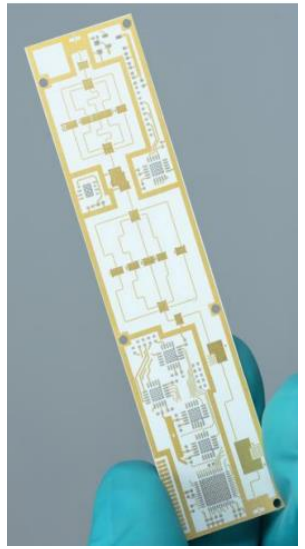
- No single solution for the cooling structure nor coolant
  - Different material budget constraints, power dissipation, space constraints, environment, …
- Key targets:
  - Electronics integration
  - Cost-effective and better scalability
- A portfolio of different approaches
  - Ceramics and 3D metal printing (UoM)
  - Microchannel cooling and active interconnection developments (CNM, DESY and IFIC)
  - Microchannel cooling manufacturing via thermocompression (CPPM)
- New projects and joining members are welcome

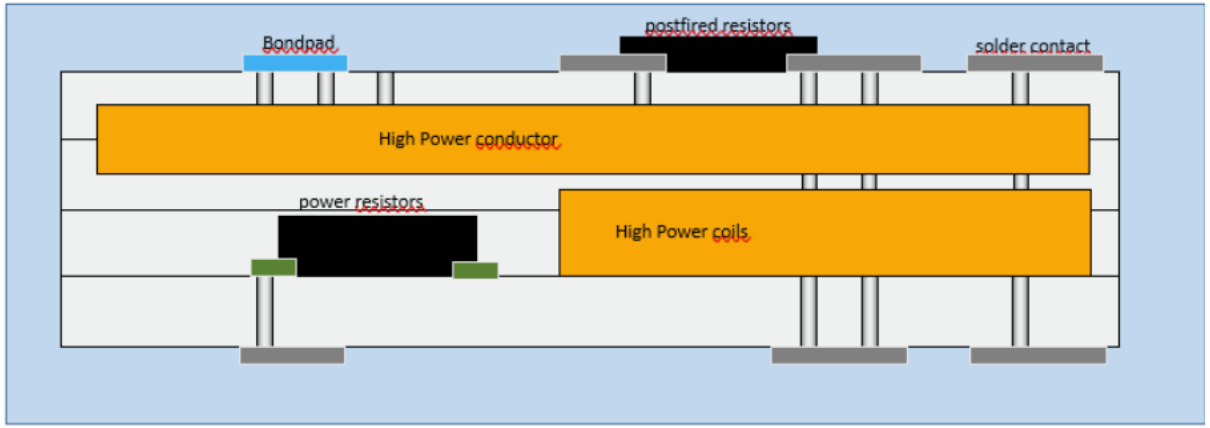
Ceramics

- Manufacturing at IKTS Fraunhofer (Germany)
- Different base materials: YSZ, Al_2O_3, … including **SiC** and **AlN**
- Manufacturing based on several layers
- <u>Why?</u>
  - Robustness, reliability, stability in ultra-high-vacuum
  - Possible to embed conductive layers in between ceramics layers and metalize the surface
    - Potential to integrate electronics or high conductivity elements
  - Mechanically robust and compatible with high ultra vacuum



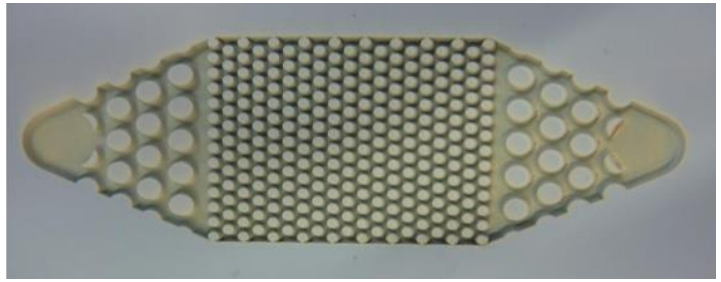
©Fraunhofer IKTS



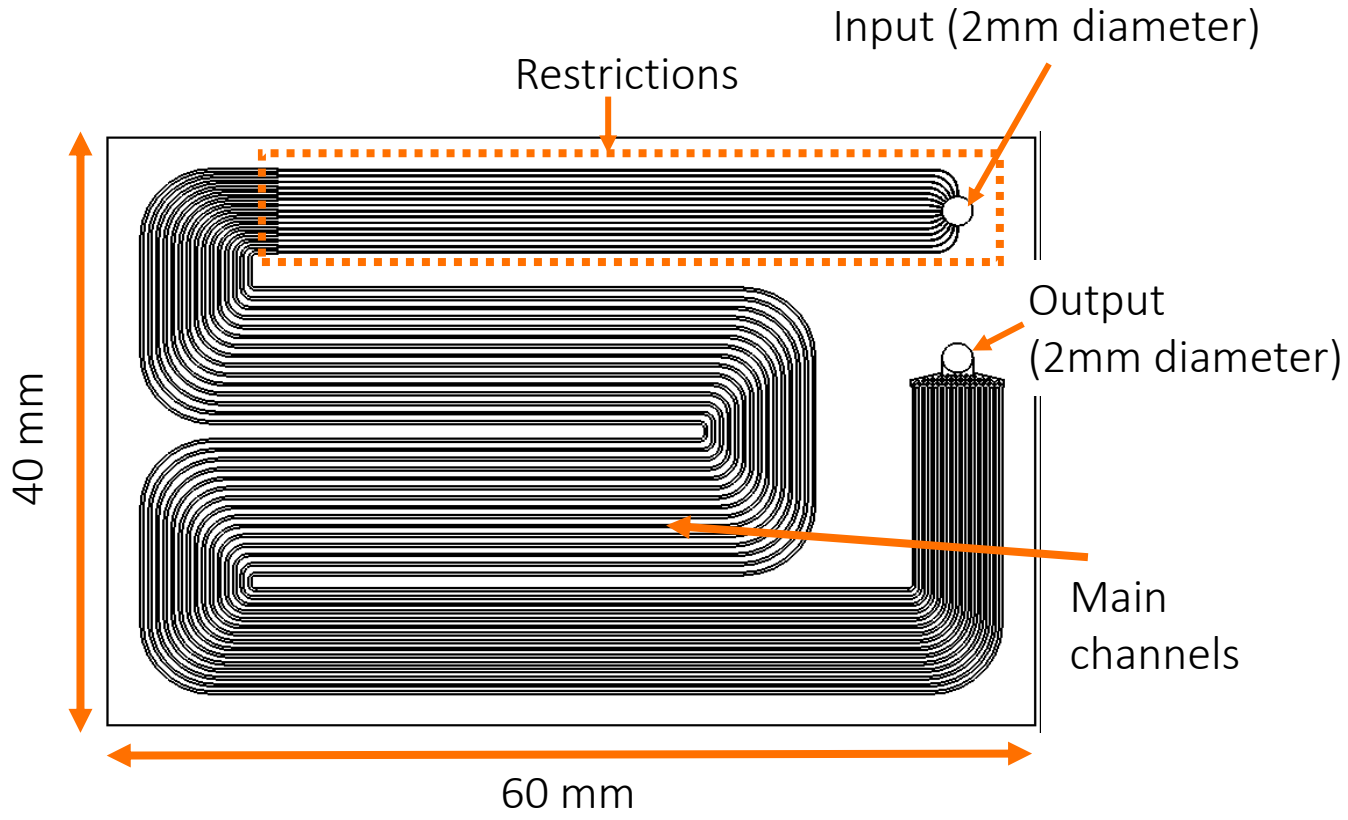


Ceramics

- Experience with fluidic applications
- First prototype based on the early VELO Upgrade I CERN design
  - Initial channel with $70\mu m$ width (restrictions)
  - Channels height $100\mu m$
  - Overall dimensions: $40 \times 60 mm^2$
  - Based on LTCC
    - $Al_2O_3/Glass \sim 1:1$
    - HTCC at a later stage (Al_2O_3 $\sim 96\%$)
  - Possible to move to SiC or AlN

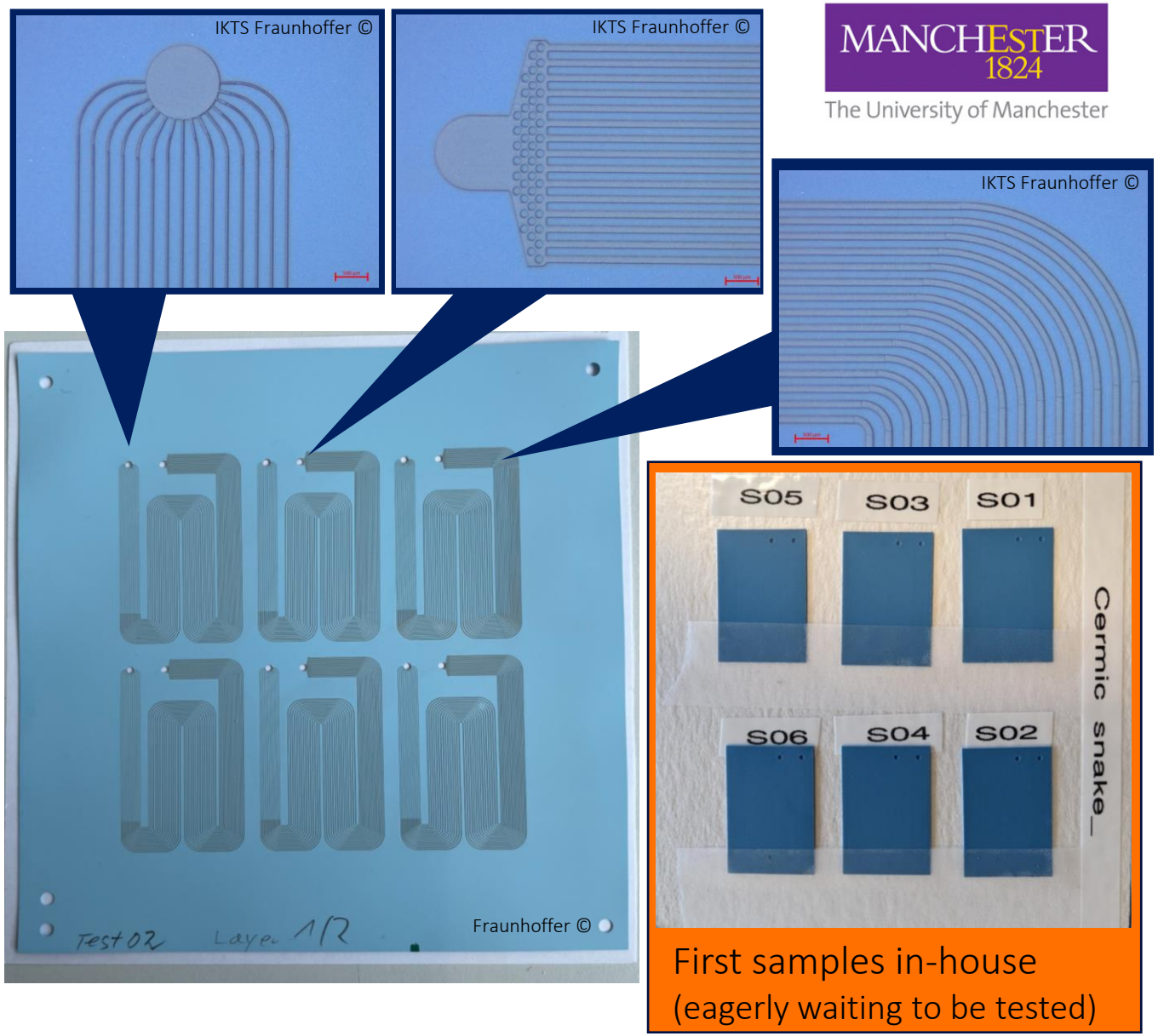


©Fraunhofer IKTS



Ceramics: Goal and status

- Goal:
  - ✓Manufacture first samples (IKTS)
    - ✓Miniaturized version (2x smaller in-plane)
    - ✓Expected 35um and 100um width restrictions and main channels respectively!
  - Second round being prepared
  - Validate initial prototypes to high pressure, leak tightness and cooling performance
  - Benchmark: LHCb VELO Upgrade 2 requirements (High pressure 186 bar, leak tight (vacuum operation) and excellent thermal performance
- Very encouraging first manufacturing results!!!

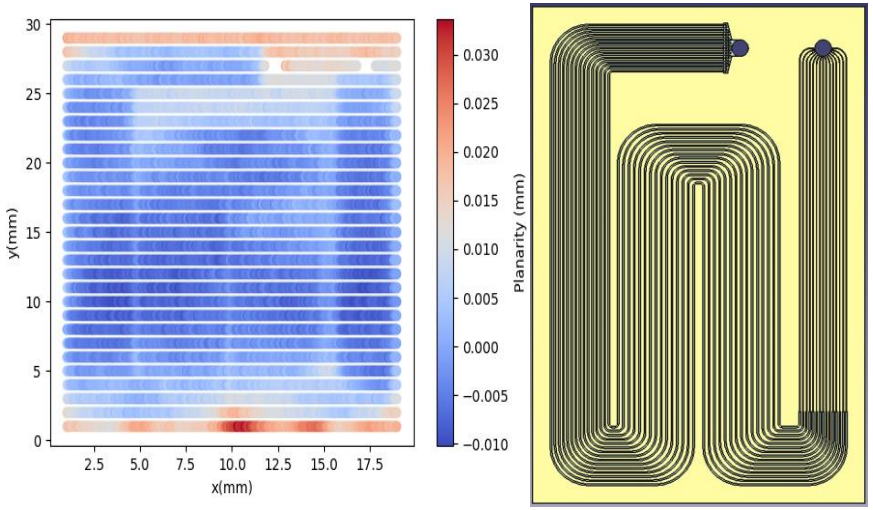


First samples in-house
(eagerly waiting to be tested)

Ceramics: Goal and status

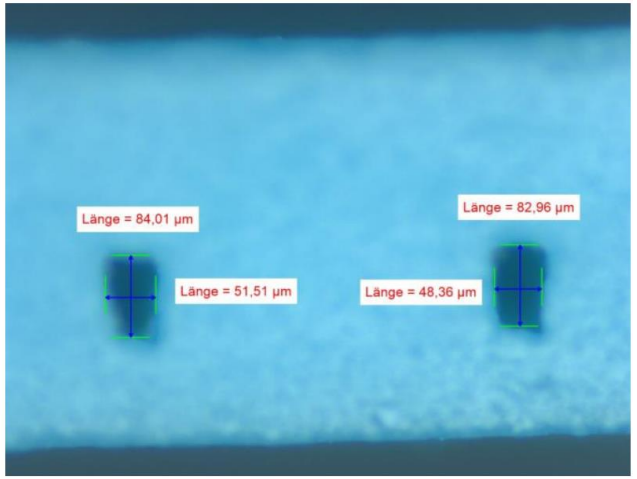
- Metrology of 20 x 30 mm2 samples of order of tenths of microns
  - Additional layer can be deposited and machine for better results
- High pressure testing
  - Target:186 bar (evaporative $\mathbf{CO_2}$)
  - 3 samples tested – broke up to a max. of 120 bar
  - Sample reinforcement and new design being prepared
- More samples arrived last week
  - $40 \times 60\mathbf{mm^2}$

Metrology

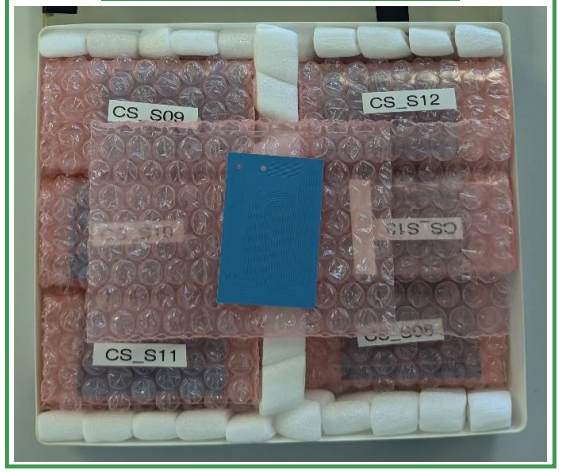


The University of Manchester

Destructive cross section measurement



Samples at UoM



3D metal

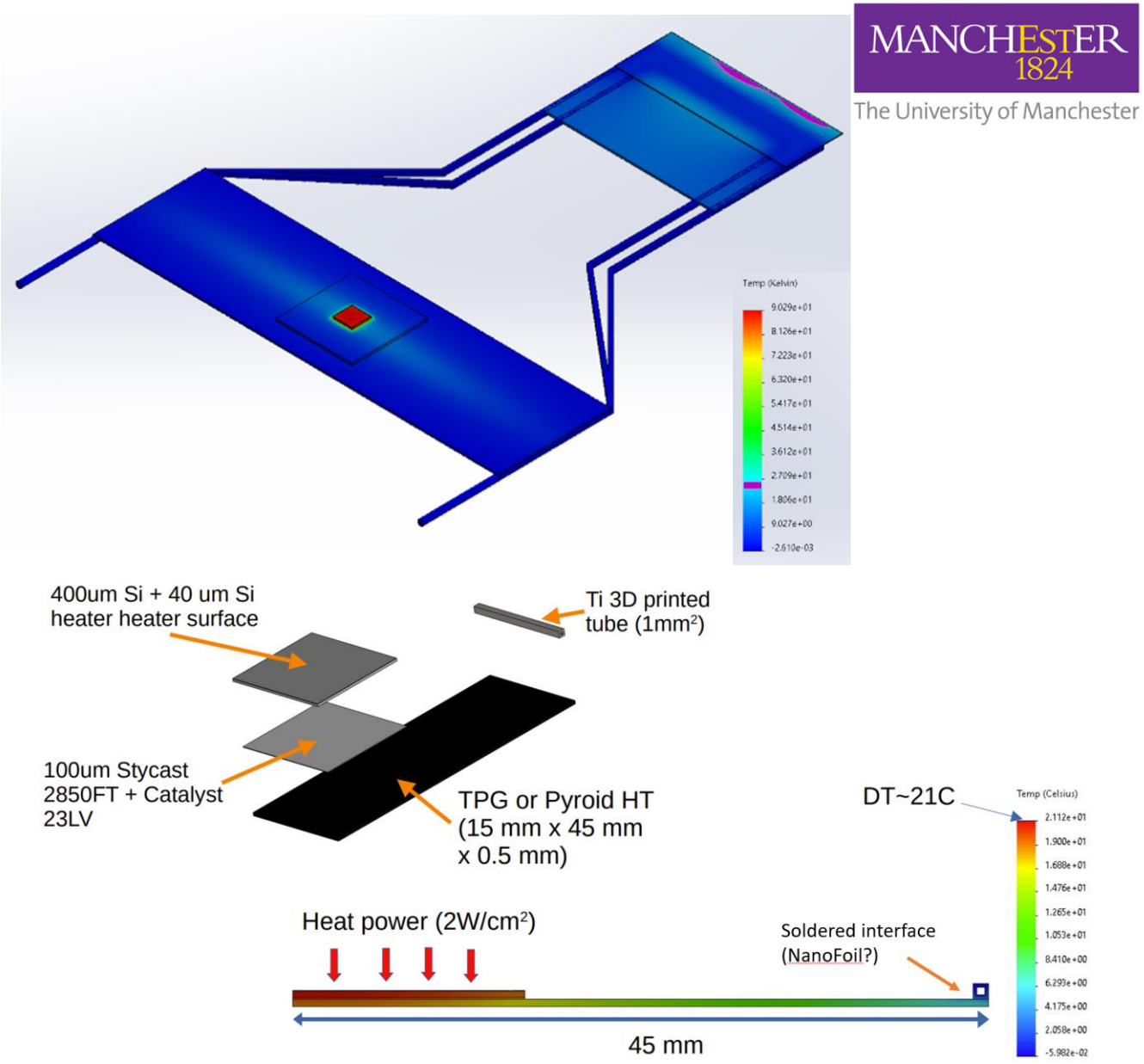
- Exploration phase
- Considering evaporative CO_2 as baseline solution
- Power dissipation of up to $2W/cm^2$

Aggressive U-track like design

- More aggressive design for reduced material budget due to the cooling substrate
- Largest variation of temperature on the sensor part around $25℃$ (with respect to the inner side wall)
  - Larger ΔT would have to be compensated by the coolant working temperature
- Alternative strategy to cooldown off-chip electronics would have to be improved (cooling routing lines)

Passive medium integration

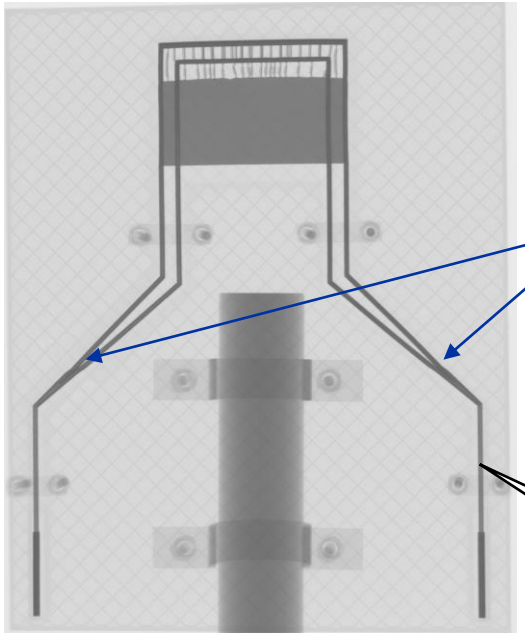
- Lower material budget contribution compared to same silicon thickness (factor x2)
- Cooling line integration via soldering (NanoFoil, 35–50W/mK)
- FEA indicates a $\Delta T \sim 21℃$ when pushing away the Ti2 cooling lines by $\sim 30mm$



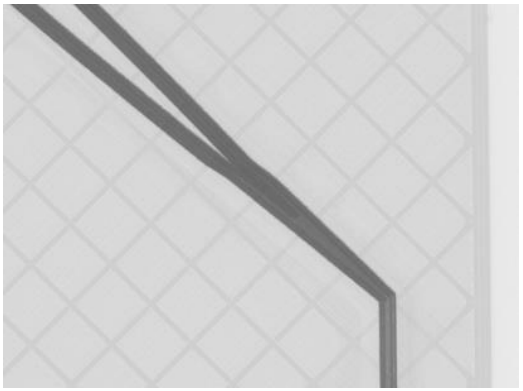
3D metal

- Royce Innovation Centre (Sheffield)
- Different designs
  - U-shaped design
  - Squared tube and connector prototypes
- X-ray tomography via NXCT

X-ray 2D tomography (one projection)

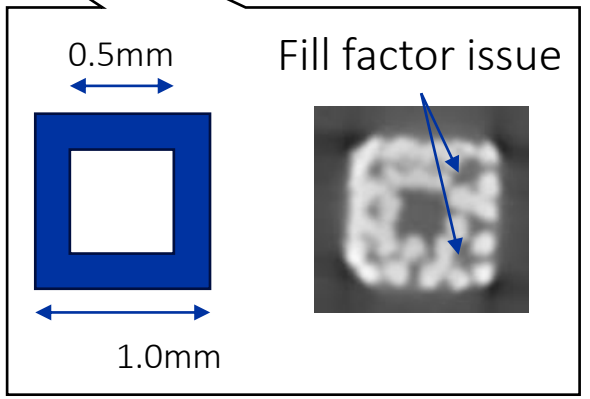


Printing distortion and blockage



New round of printing (August):

- Filling factor and distortions being improved
- Different printing parameters to improve distortions and fill factor
- Half of the samples will be electro-polished (easier integration?)
- Samples are being post-processed



Microchannel cooling and active interconnection developments

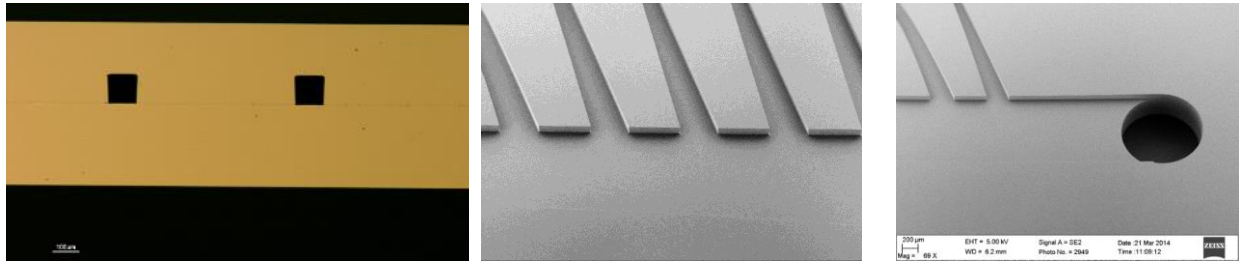
- **Miguel Ullán (IMB-CNM, CSIC)**, Carlos Mariñas (IFIC-UV, CSIC), Marcel Vos (IFIC, CSIC-UV), Ingrid Gregor (DESY), Sergio Díez (DESY) and Jonathan Correa (from DESY)
- In the past, we developed a technology of micro-channel cooling for High Energy Physics detectors
  - N. Flaschel, et al. “Thermal and hydrodynamic studies for micro-channel cooling for large area silicon sensors in high energy physics experiments”, NIMA, vol. 863, pp. 26-34, 2017. (link)
  - Ph.D Thesis: Micro-channel Cooling For Silicon Detectors. Nils Flaschel. Hamburg University. 2017 (link)

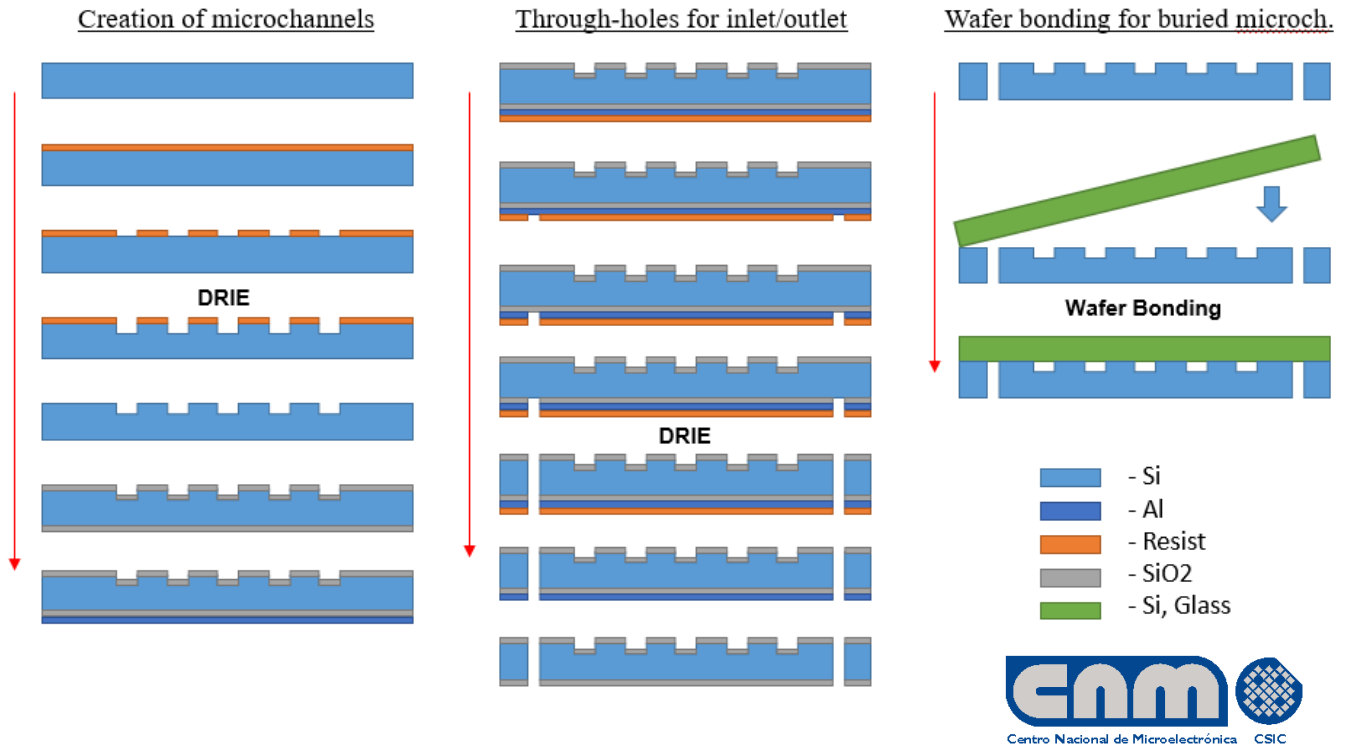
Microchannel cooling and active interconnection developments

- Technological process for micro-channels at IMB-CNM

- Creation of microchannels:
  - Deep Reactive ion etching (DRIE)

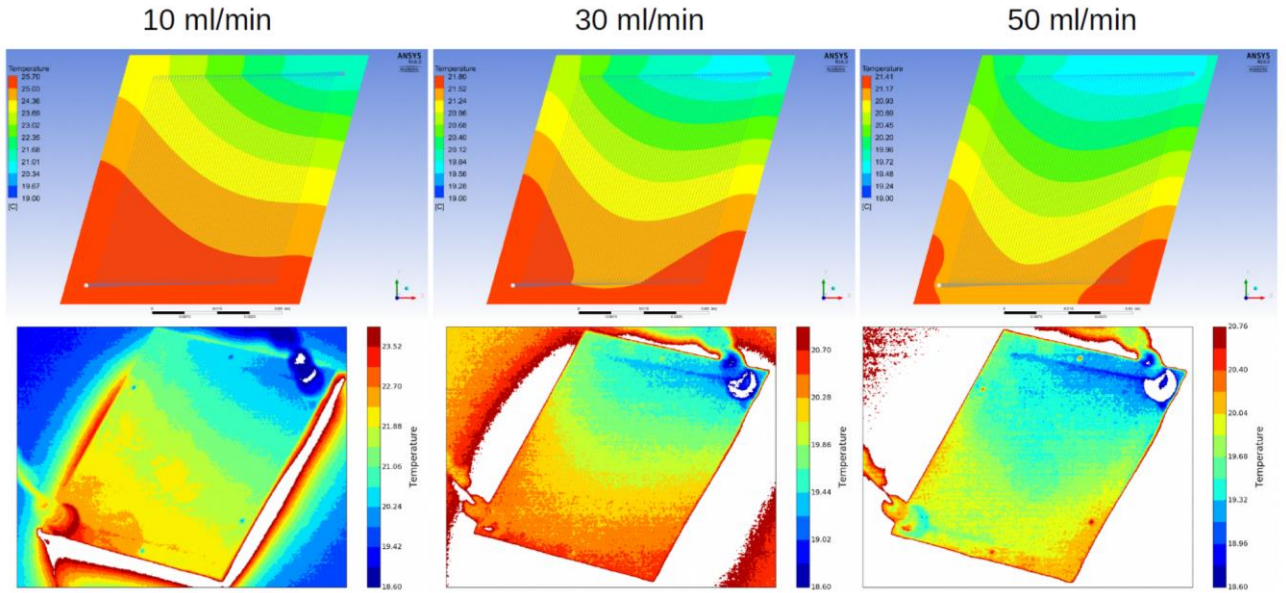
- Microchannels enclosure via:
  - Wafer bonding

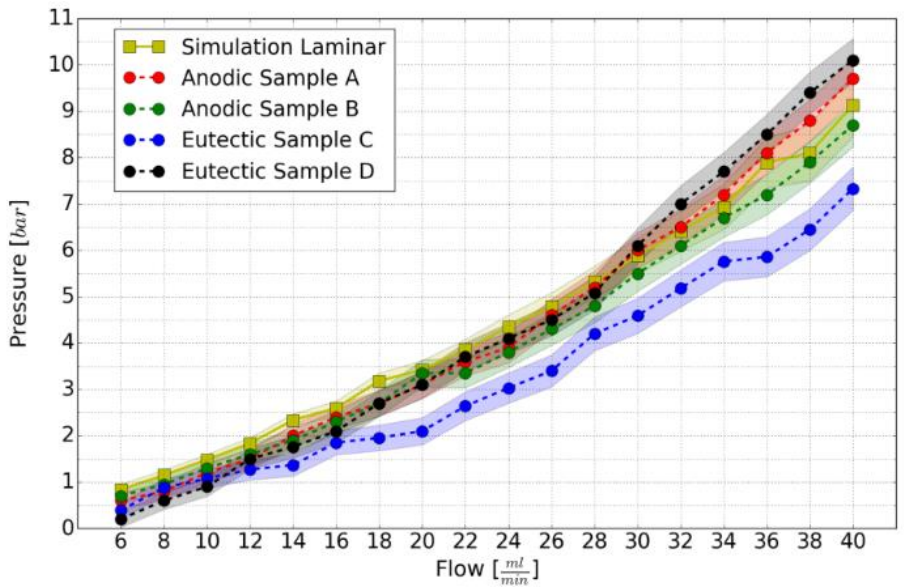




Microchannel cooling and active interconnection developments

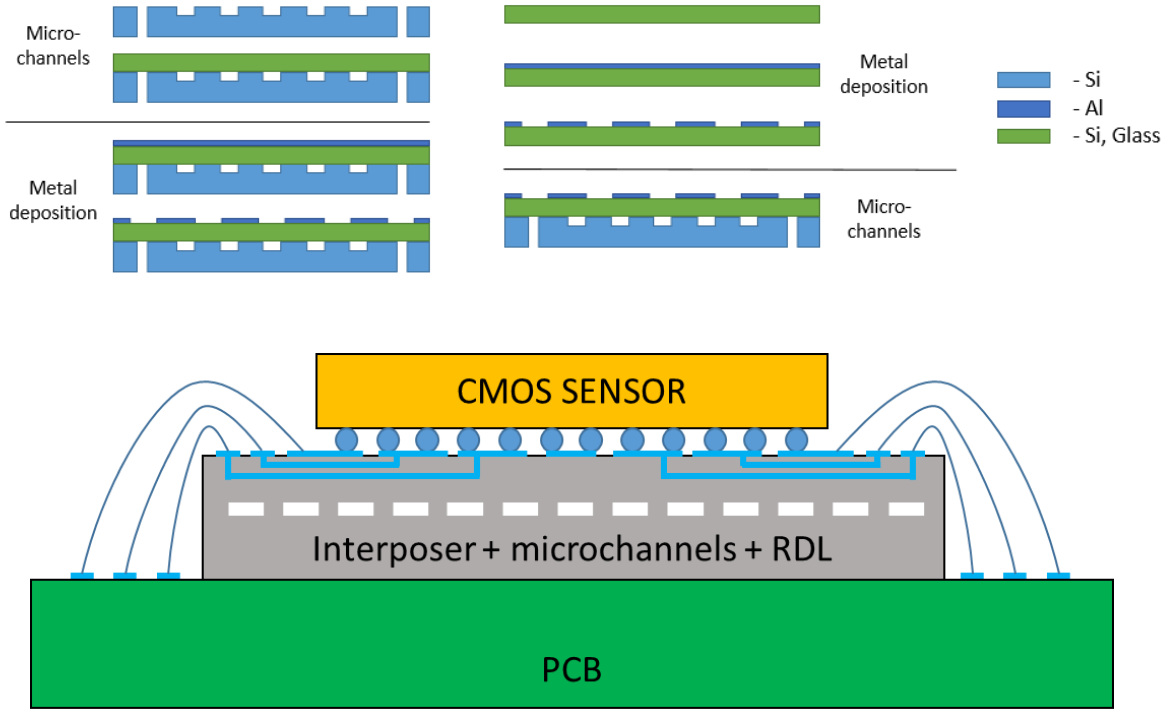
- Previous results on fluidic and thermal tests
- Laminar flow
- Coolant: 3M HFE7100
- Low power density: $30.8\mathrm{mW/cm^2}$
- Good agreement with simulation
- Thermal homogeneity across the sample($\sim 4 \times 4\ \mathrm{cm^2}$ large), $< \pm 1$ ºC (for lowest flow rate)





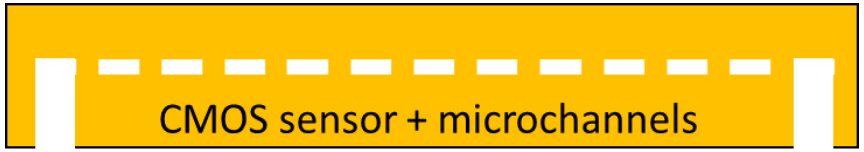
Microchannel cooling and active interconnection developments

- Main Objective I: Integration of micro-channels in silicon interposers with integrated signal and power routing (RDL)



Main Objective II: Full integration of the sensor (CMOS technology) with the microchannel cooling in a single silicon piece

- Full integration of DMAPS chip with the microchannels in a single monolithic piece
- Post-processing at wafer level with a CMOS compatible process
- Following the "post-processing" technique developed previously
- Additional technological developments
  - ✓ Low temperature ($350°C$) anodic bonding
  - ➢ Microchannels created on glass substrates (isotropic wet etching)
  - ➢ Eutectic and/or fusion bonding
  - ➢ Improve post-processing compatibility
  - ➢ Full demonstrator



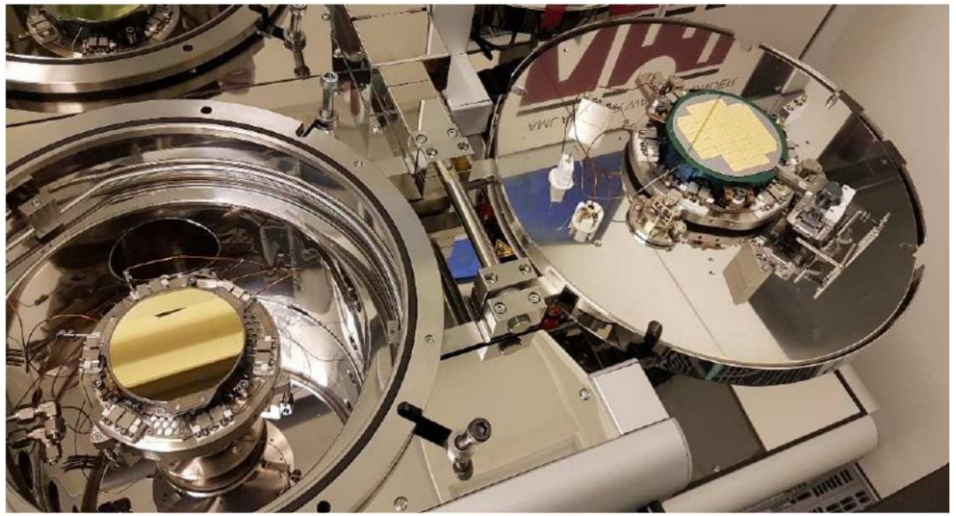
Microchannel cooling manufacturing via thermocompression

R&D to develop a low-cost micro-channel production process

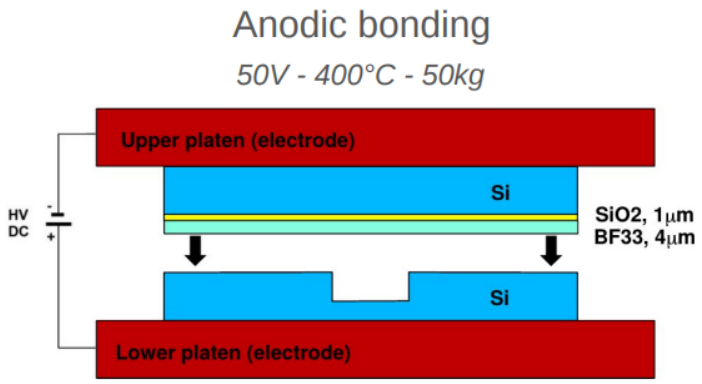
As an alternative to the complicated and costly direct Si/Si bonding, investigate bonding techniques with intermediate thin layers:

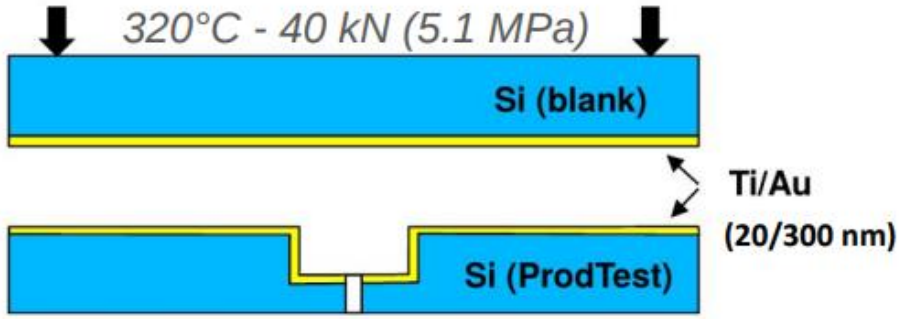
- Anodic bonding with glass (BF33)
- Thermocompression with gold

Bargiel et al., Micromachines 2023, 14, 1297



Thermocompression





Microchannel cooling manufacturing via thermocompression

Bargiel et al., Micromachines 2023, 14, 1297

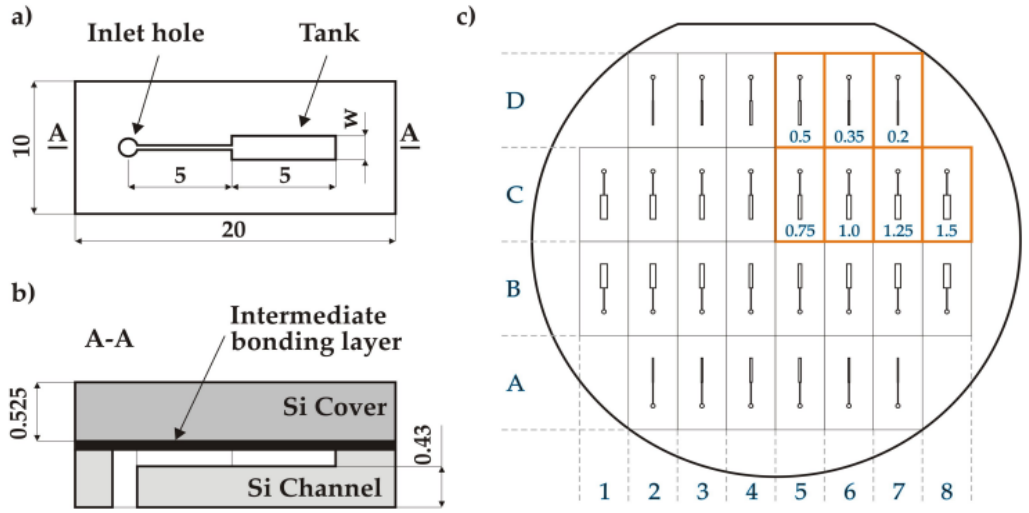
Bonding strength evaluated through a series of destructive pressure burst tests, recording the maximum pressure reached in microfluidic test structures before breakage (à la LHCb)

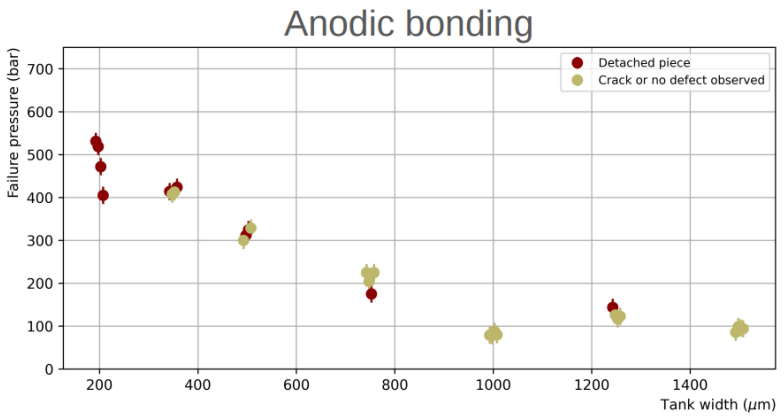
⇒ Test chips produced both with the anodic and with the thermocompression bondings can sustain very high pressure

⇒ Focus on thermocompression as

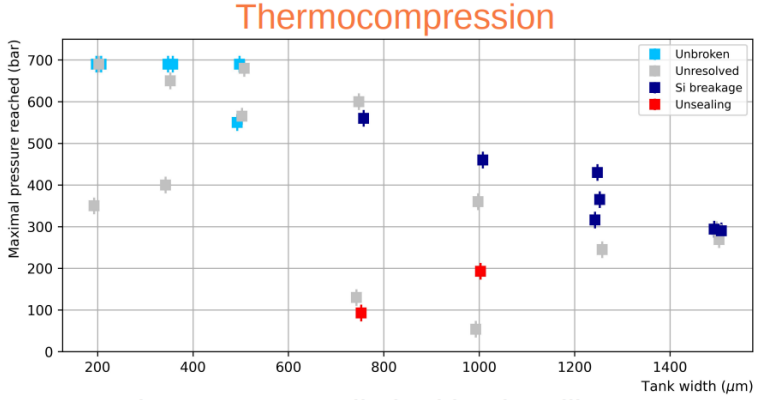
– It generally allows to reach higher maximal pressures

– It is a widespread technique available in most clean room facilities





Maximum pressure limited by the adhesion force of the deposited BF33/SiO_2 layers

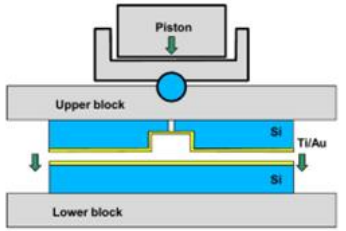


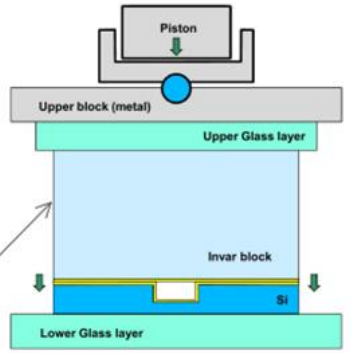
Maximum pressure limited by the silicon strength (except for a few outliers)

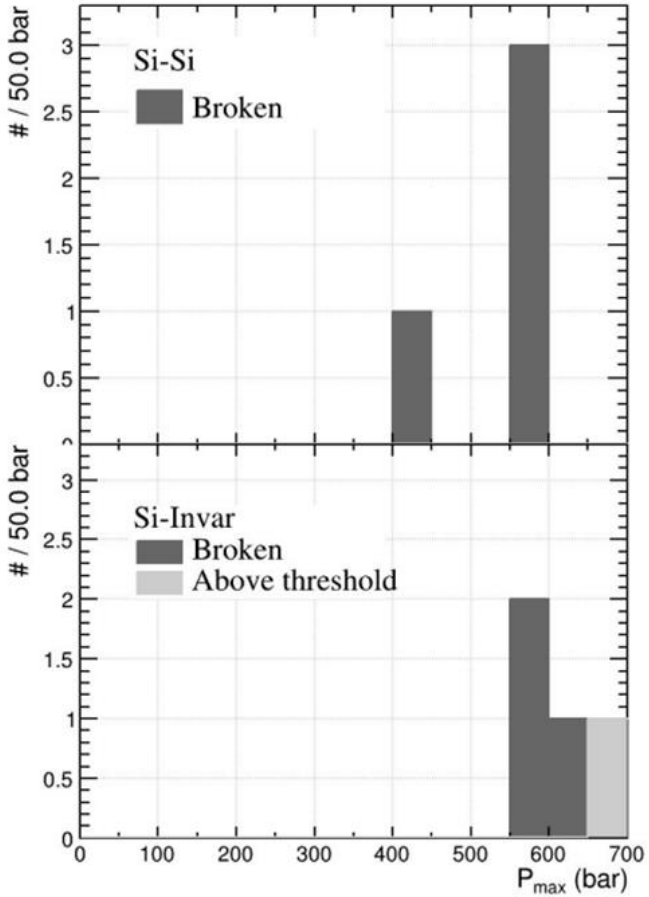
Microchannel cooling manufacturing via thermocompression

- Towards the bonding of a connector using thermocompression process:
  - Investigate chip level bonding replacing the bonder with a mechanical press at atmospheric pressure outside the clean room
- Two configurations tested:
  -Si/Si bonding (for reference)
  -Si/Invar
  → Both types can sustain high pressure
  → Proof of concept validated!

Polished block of Invar mimicking a connector





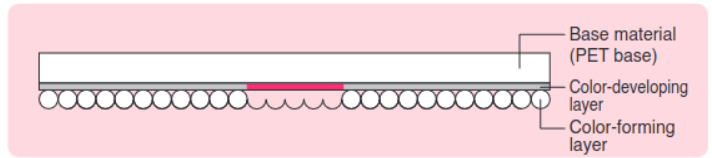


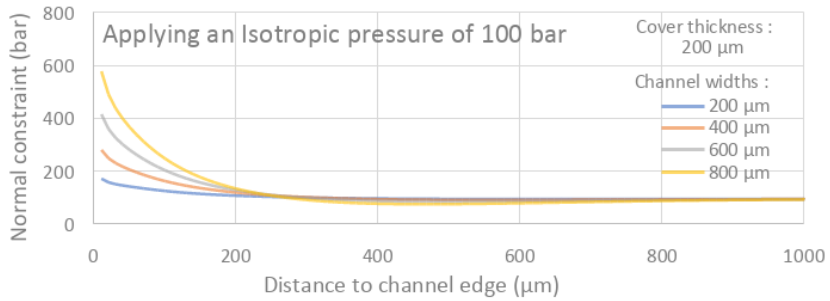
Hyperbar bonding

Replace the mechanical press with an hyperbar chamber

- Allow to reach very high pressure on large surface
  - ≥ 400 bar in chamber
  - Force applied in bonder typically limited to 40kN
  - (i.e. 5.1MPa for 4” wafer, 2.3MPa for 6” wafer)
- Pressure more uniform
- Less stress applied on wafer
- Bonding at room temperature
- Can adapt various geometries

- Visualizing the pressure applied in the hyperbar chamber
- Using a pressure sensitive film
- “Pressure boost” around the channel as expected from numerical simulation





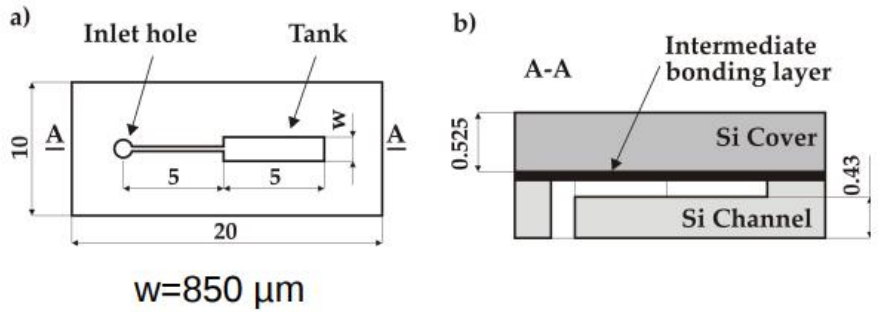
Microchannel cooling manufacturing via thermocompression

- Replace the mechanical press with an hyperbar chamber
  - Allow to reach very high pressure
  - ≥ 400 bar in chamber
  - Force applied in bonder limited to 40kN
  - (i.e. 5.1MPa for 4” wafer, 2.3MPa for 6” wafer)
  - Pressure more uniform
  - Less stress applied on wafer
  - Bonding at room temperature
  - Can adapt various geometries
- Test wafer bonding with fixed width pressure test structures (w=850µm)

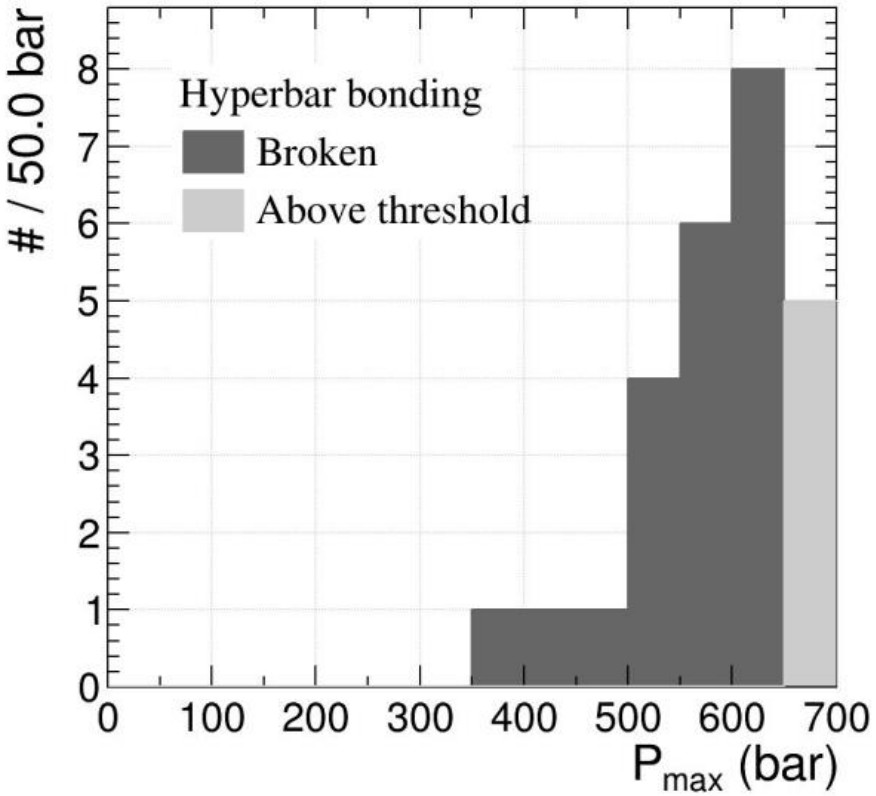
⇒ All samples sustained very high pressure

⇒ All breakage occurred in the silicon (i.e. bonding has held)

⇒ Proof of concept validated !



w=850 µm



Microchannel cooling manufacturing via thermocompression

R&D to develop low-cost micro-channel production process is being pursued at CPPM

Currently focusing on the bonding process, very appealing technique identified:
– “Hyperbar” bonding with thin intermediate Au layers
– Can be used to bond wafer
– Bonding of connector in hyperbar chamber being investigated

Goal is a functional prototype in the coming years

Part of a global R&T effort in CNRS/IN2P3, shared among 3 French laboratories and including developments on boiling flow modelling and testing.

DRD7/DRD8:Cooling and cooling plates

B.4.3 Project 7.4c: Cooling and cooling plates

This project focuses on the development of the next generation of cooling plates for front-end electronics and sensors based on different materials/techniques. The main goal is to explore manufacturing techniques while improving electronics integration with a cost-effective solution. This project groups different topics covered by different collaborations which will be presented in the coming sections.

Note that depending on the evolution of the forming DRD8 Collaboration, some cooling-related projects may be best integrated in DRD8. This will be fine tuned in due-time to best match the needs of the projects.

Project Name	Cooling and cooling plates (WG7.4c)
Project Description	Development of the general purpose next generation of microchannels cooling structures to deliver excellent cooling performance, minimal material budget, and better electronics integration. Duration about 2+ years.
Innovative/strategic vision	Better integration of electronics features to the cooling plates especially in dense electronics applications. Better scalability considering alternative manufacturing techniques (more cost-effective). Thermal performance numerical simulation tools for new applications.
Performance Target	Different topics will explore different combinations of the following parameters: power dissipation (up to $2W/cm^2$), material budget ($\leq 0.5\%X_0$), integration and/or cost. Different experiments will be able to profit from the portfolio created and optimize those solutions for their final application. The progress will be tracked via public reports in the form of presentations, public notes and/or papers.
Multi-disciplinary, cross-WG content	Communication with DRD8 (Mechanics) and DRD3 (Semiconductor detectors) via liaisons and workshops (e. g.: Forum on tracking mechanics) and 7.6b project (common access 3D and advanced integration) within the DRD7.
Contributors	CERN DE: DESY ES: IMB-CNM, IFIC-Valencia UK: Manchester FR: French Collaboration

- Common understanding among all collaborators
  - Split the project between DRD7 and DRD8
  - Move “mechanics” to DRD8
  - Keep “electronics” on DRD7
- DRD8 project will be created
  - Design optimization
  - Resistance to high pressure
  - Fluidic connector integration, …
- DRD7 project will be descoped
  - Focus on electronics integration on cooling plates
  - CMOS process compatibility

Timeline:

- The first version of the project in the DRD8 by end of September
- Prepare a proposal for the DRD7 descoping

Conclusion (1/2)

- Ceramics
  - It has also the potential to include electronic features
  - Fully validated initial prototypes in the coming years to high pressure, leak tightness and cooling performance in the following years
  - LHCb VELO Upgrade 2 as benchmark requirements (High pressure, CO_2 evaporative cooling)

- Metal 3D printing
  - X-ray tomography indicates issue with the fill factor
  - Distortion observed created a choke point
  - New run printed
    - focus on improving distortion and fill factor and investigation of electropolishing (material reduction/easier integration?)

- Microchannel cooling and active interconnection developments (CNM, DESY, IFIC)
  - Aiming to bring more functionalities to the cooling plate
    - Redistribution layer could be an interesting solution for ASICs with through-silicon vias
  - CMOS compatible process to integrate the cooling to the sensor

Conclusion (2/2)

- Microchannel cooling manufacturing via thermocompression (CPPM)
  - Main motivation to reduce the manufacturing cost
    - Very promising results “hyperbar” chamber (resistance to high pressure)
  - Techniques developed can be also explored for integration (chips and connecturization)

- DRD7/8: Cooling and cooling plates
  - *“Mechanics”* in DRD8 and *“Electronics”* in DRD7
  - First version of the draft by end of September in the DRD8
  - Request for descoped DRD7 proposal afterwards

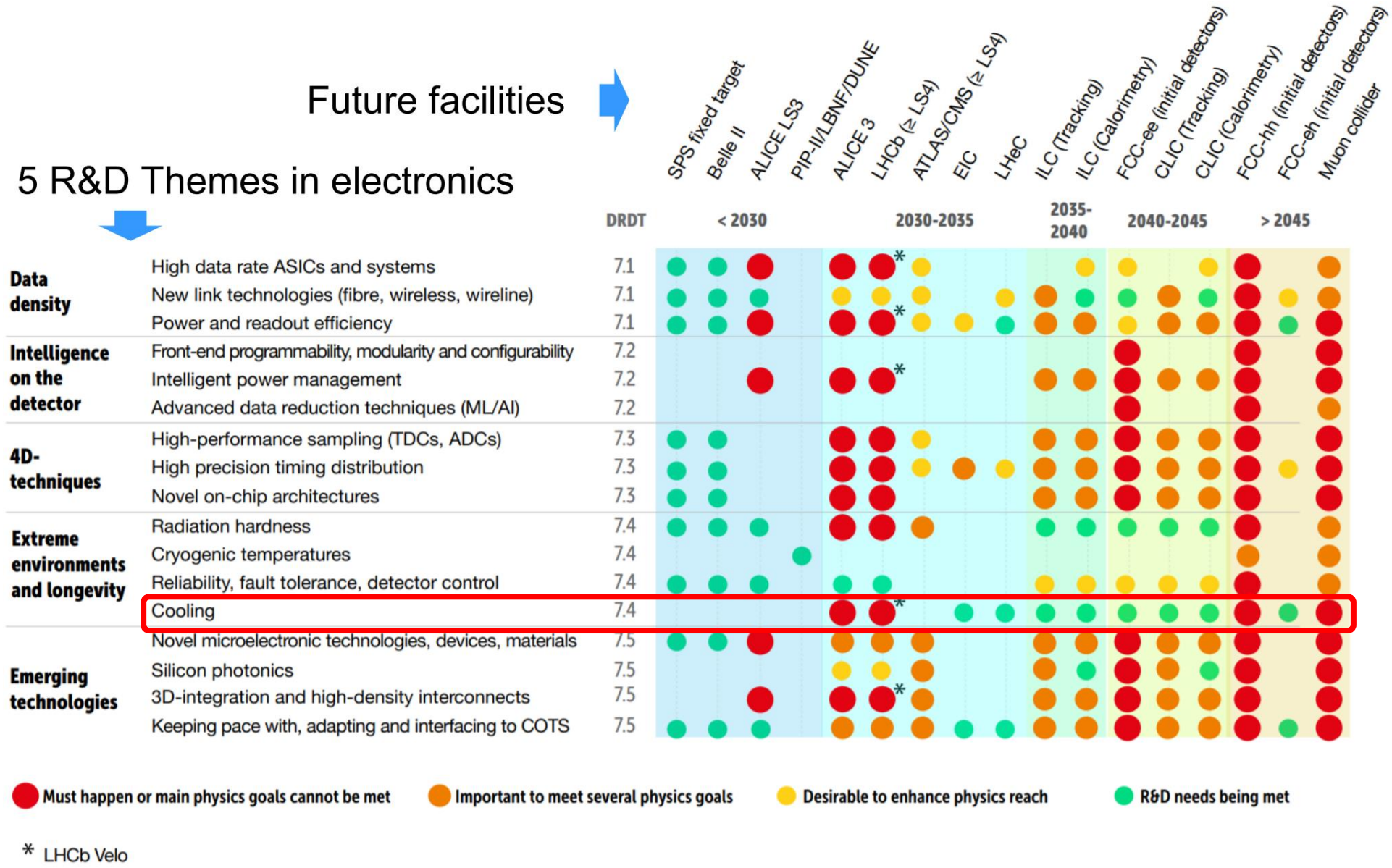
Contacts

- Microchannel cooling and active interconnection developments (CNM, DESY, IFIC)
  - Miguel Ullan (miguel.ullan at imb-cnm.csic.es)
- Microchannel cooling manufacturing via thermocompression (CPPM)
  - Julien Cogan (cogan at cppm.in2p3.fr)
- Ceramics and Metal 3D printing
  - Oscar Augusto de Aguiar Francisco (oscar.augusto at manchester.ac.uk)

Backup slides

Future facilities

5 R&D Themes in electronics



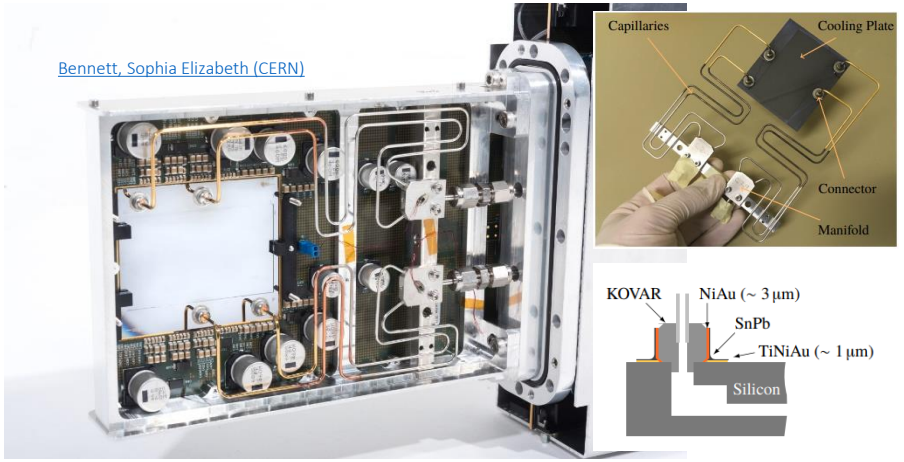
Cooling

- Vacuum
- Operating Temperature
- Material Budget
- Power density
- Thermal figure of merit
- Integration
- Area/Cost

NA62 GTK

JINST **14** P07010

Bennett, Sophia Elizabeth (CERN)

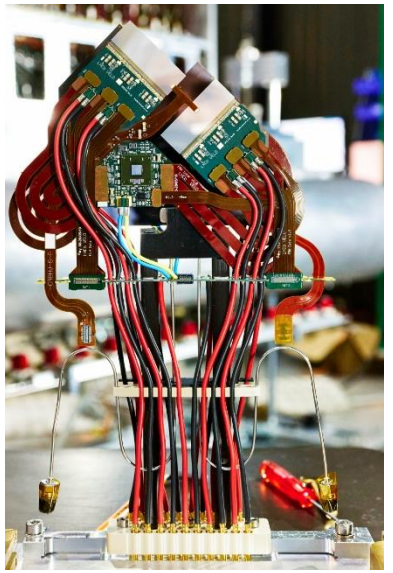


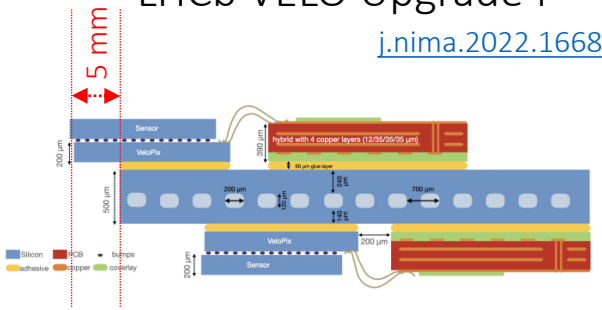
0.5% X_0, 200 × 70 μm^2 micro-channels, C6F14 liquid coolant, vacuum, $0.32\ W/cm^2$ in the pixel matrix, < 5C

LHCb VELO Upgrade I

Brice, Maximilien; Ordan, Julien Marius (CERN)

j.nima.2022.166874

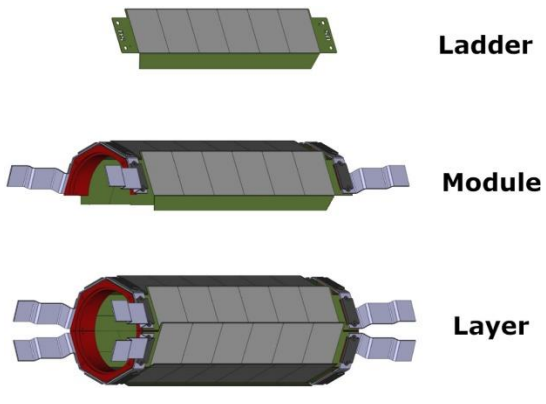




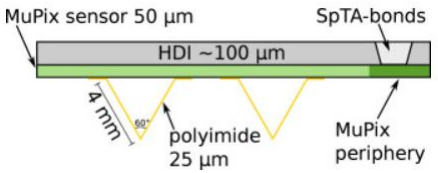
0.4-0.9% X_0 (innermost region)
ASIC/Sensor overhangs by 5 mm,
Micro-channels 120x200 μm^2,
CO2 bi-phase, 1W/cm^2, Sensor < $-20°C$, vacuum

Mu3e

SciPost Phys. Proc. 5, 020 (2021)

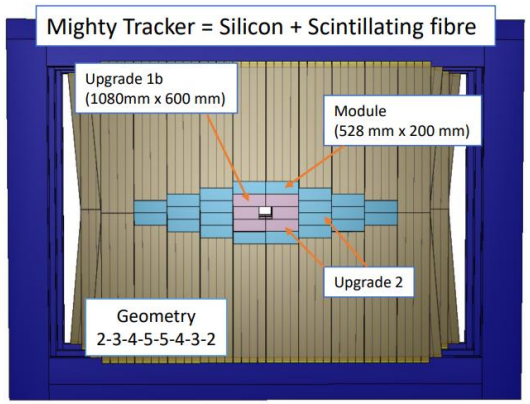


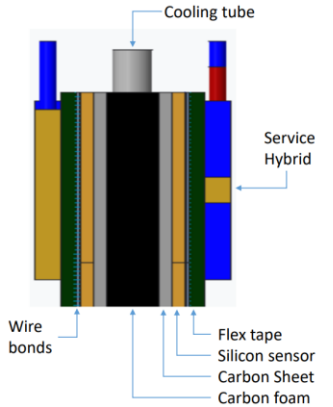
0.1% X_0, Helium gas cooling, $0.4W/cm^2$, Temperature < $70°C$



LHCb Mighty Tracker (2032)

FTDR





$18m^2$, 1-2% X_0, Kapton tubes, Liquid cooling (?), $0.3W/cm^2$, Temperature $\leq 0°C$