EXTREME ENVIRONMENTS

WP7.4b: Radiation Resistance of Advanced CMOS Nodes

DRD7: AN R&D COLLABORATION ON ELECTRONICS AND ON-DETECTOR PROCESSING

3rd WORKSHOP

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This project investigates the radiation response of CMOS technologies from the 28nm node onwar for use in the next generations of ASICs for particle detectors.

Project Name	Radiation Resistance of Advanced CMOS Nodes (WP7.4b)
Project Description	This project aims to evaluate the radiation response (total ionizing dose TID, single event effects SEE, and displacement damage DD) of commercial CMOS technologies more advanced than the 65nm node for use in the next generations of ASICs for particle detectors. Duration 4-5 years.
Innovative/strategic vision	Understanding the effects of radiation on CMOS technologies is essential for the design of ASICs used in particle detectors. This project represents a first and crucial step in evaluating the performance of advanced CMOS nodes for the unique environment of particle detectors.
Performance Target	Deepen the knowledge of the radiation response of 40nm and 28nm technologies and begin to study finFETs technologies.
Milestones and Deliverables	**D7.4b.1** (M12) Deliver a 28nm CMOS front-end (FE) circuits for pixel sensors prototype; TID test of IP-blocks in 28nm node **D7.4b.2** (M18) Deliver a chip in 28nm CMOS including matrices of FE channels for readout of pixel sensors **M7.4b.3** (M24) Radiation test of FE structures; Design and testing of rad-hard memory elements in 28nm node **D7.4b.4** (M36) Deliver a prototype in FinFET technology including IP blocks for pixel readout circuits.
Multi-disciplinary, cross-WP content	In order to ensure the success of projects involving ASIC design for particle detectors, it is imperative to consider the radiation resistance of the technologies used. On the other hand, the definition of radiation qualification would greatly benefit from the input of the designer. For example, ASICs developed in WP7.3a must be radiation tolerant and could also serve as valuable test vehicles to evaluate radiation effects.
Contributors	CERN AT: TU Graz IT: INFN Pavia, Uni. Bergamo, Uni. Padova, Uni. Pavia FR: CPPM

7.4.b: EXTREME ENVIRONMENT AND LONGEVITY - RADIATION HARDNESS

Project: radiation resistance of advanced CMOS nodes

[CH]

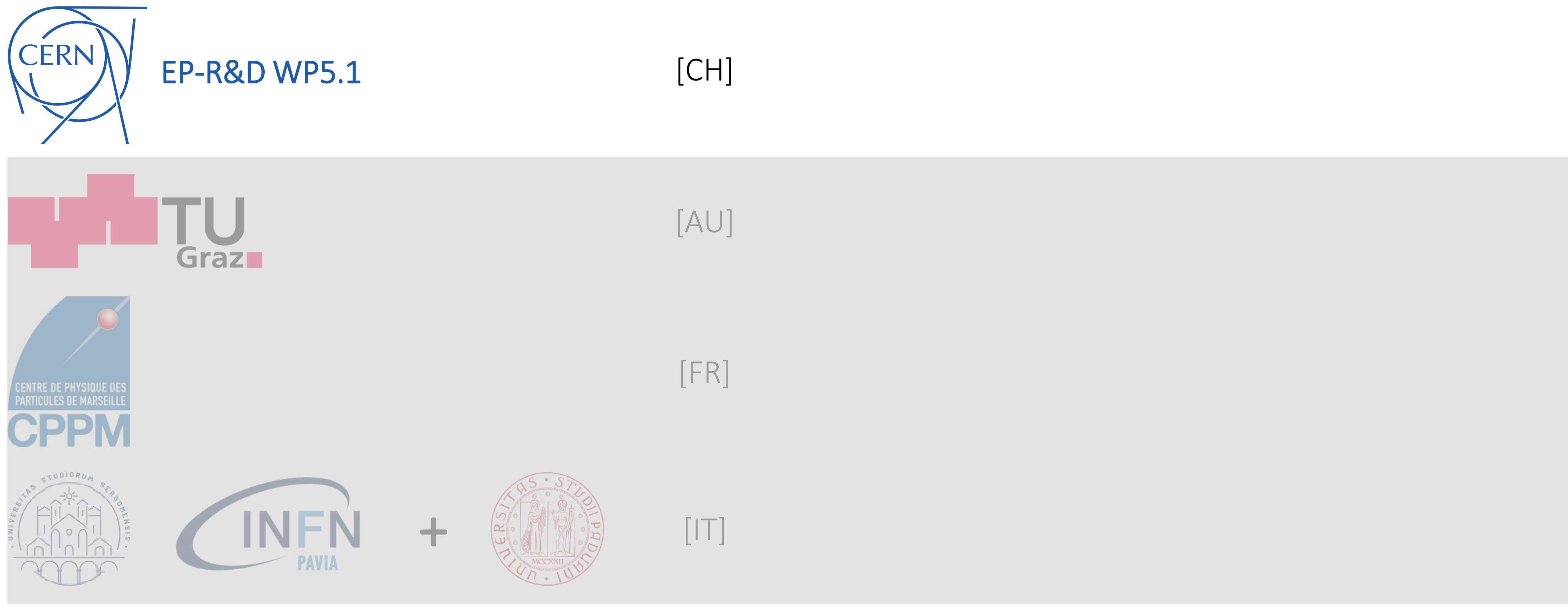
[AU]

[FR]

[IT]

7.4.b: EXTREME ENVIRONMENT AND LONGEVITY - RADIATION HARDNESS

Project: radiation resistance of advanced CMOS nodes



EP-R&D WP5.1

- vast experience on radiation-effects on CMOS technology
  - 250nm, 130nm, 65nm, 40nm 28nm, 22FDSOI

- 2 X-ray machines (AsteriX and ObeliX)

~50 pages of report on SEE in 28nm technology

SEE Characterization
Of A Commercial
28nm CMOS Technology

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March 18, 2024

- 2 chips (EXP28:SEE, EXP28:ANA)
- Heavy ions and proton tests

  - SRAM
  - DFF
  - SET detector
  - SEL detector

    - SBU
    - MBU
    - SET
    - SEL

https://asic-support-28.web.cern.ch/tech-docs/assets/radtol_reports/SEE_characterization_of_a_commercial_28nm_CMOS_technology.pdf

EP-R&D WP5.1

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Figure 3.1: Cross section for the 7 matrices of DFF exposed to all available HI with an incident angle $\theta = 0°$ (left) and $\theta = 45°$ (right). The fluence is $\Phi \simeq 5 \times 10^6$ ions/cm^2 for all tests. On top of the figure, the sum of errors in all matrices is reported for each LET.

https://asic-support-28.web.cern.ch/tech-docs/assets/radtol_reports/SEE_characterization_of_a_commercial_28nm_CMOS_technology.pdf

EP-R&D WP5.1

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    - SRAM
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        - SBU
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It will be soon updated with new data collected this June.

(SEL only measured for VDD > 1.8V)

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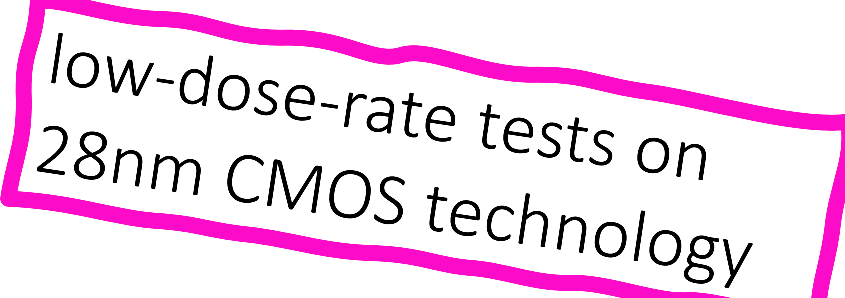
EP-R&D WP5.1



H-4

ELDRS in a commercial 28nm CMOS technology

G. Borghello[1], G. Termo[2], F. Faccio[1], D. Ceresa[1], R. Pejasinovic[1], G. Bergamin[1], F. Piernas Diaz[1], K. Kloukinas[1]

1. CERN (Switzerland), 2. EPFL (Switzerland)

Evidence of ELDRS in TID-induced leakage current increase was observed in ring-oscillators, SRAMs, and single transistors in 28nm CMOS technology. The influence of bias and temperature was evaluated, and a proposed qualification procedure is discussed.

EP-R&D WP5.1

low-dose-rate tests on
28nm CMOS technology

H-4

ELDRS in a con

G. Borghello[1], G. T
K. Kloukinas[1]
1. CERN (Switzerlan

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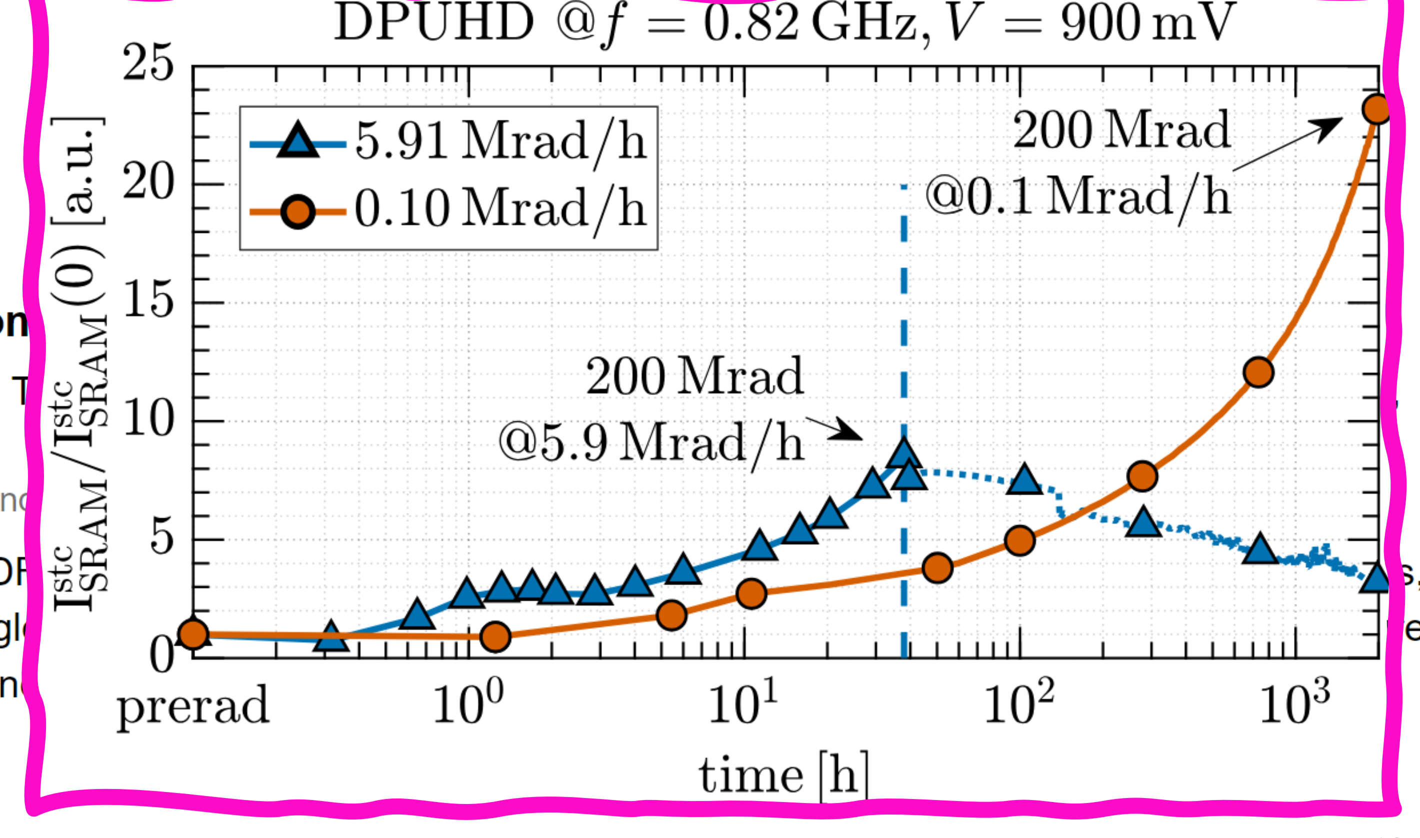


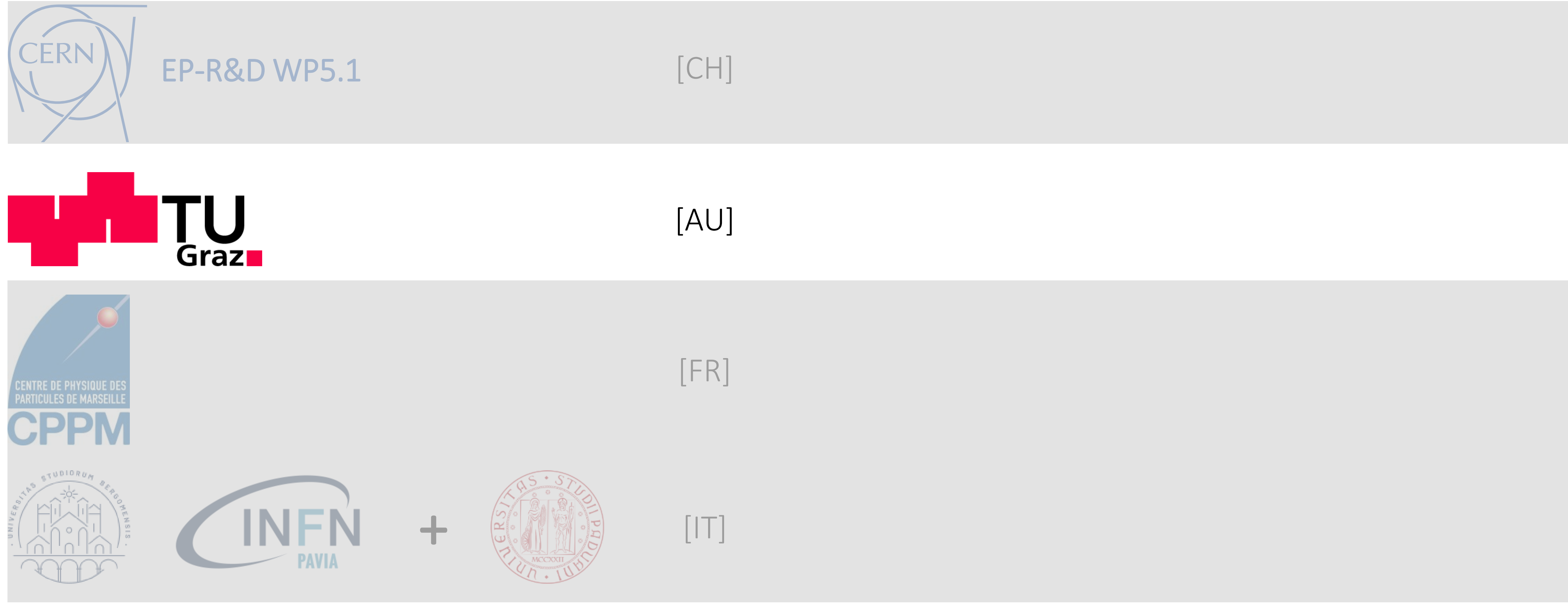
EP-R&D WP5.1

- TID effects on ESD protections
- TID effects on PN junction
- Simulations (and measure) on dose-enhancement effect
- ....

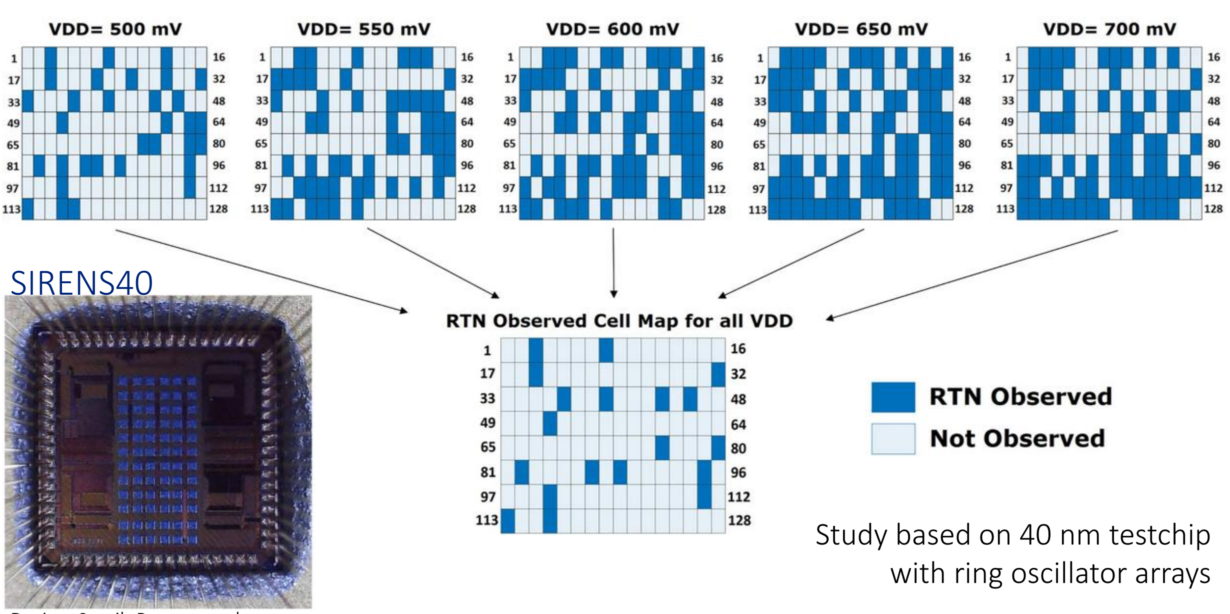
chip to submit in October 2024

7.4.b: EXTREME ENVIRONMENT AND LONGEVITY - RADIATION HARDNESS

Project: radiation resistance of advanced CMOS nodes



40nm CMOS technology

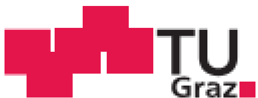


Design: Semih Ramazanoglu

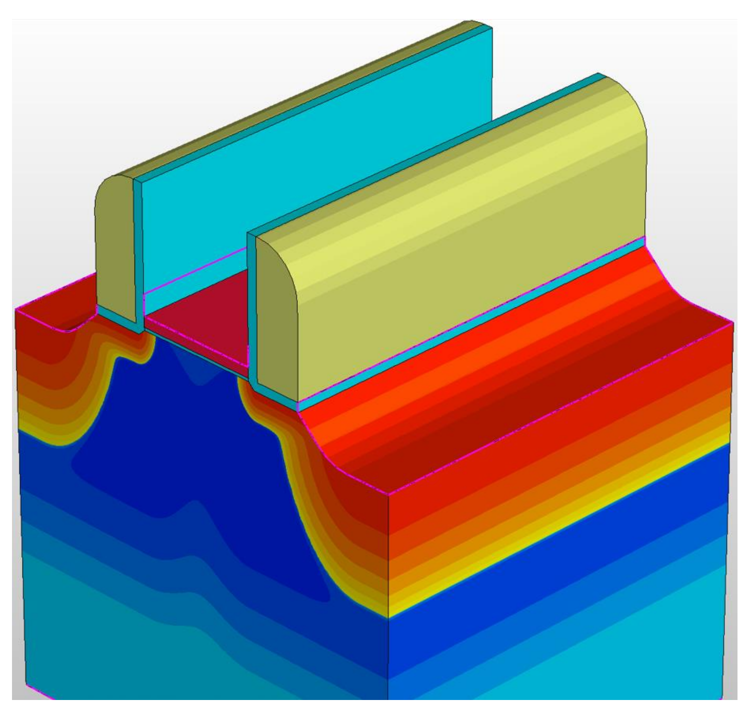
Study based on 40 nm testchip with ring oscillator arrays

Statistics of RTN evolution with TID

- **Test Setup**: Characterization of 128 differential inverter-based Ring Oscillators (ROSCs) under TID exposure up to 100 Mrad for power supply levels 600 mV … 800 mV.
- **Monitoring Set**: RTN tracked in 24 preselected ROSCs at each TID increment.
- **Samples**: 72 ROSCs analyzed across three chip samples (24 ROSCs per sample).
- **Final Characterization**: Re-assessment of full chip post-100 Mrad across power supply levels (600 mV to 800 mV).



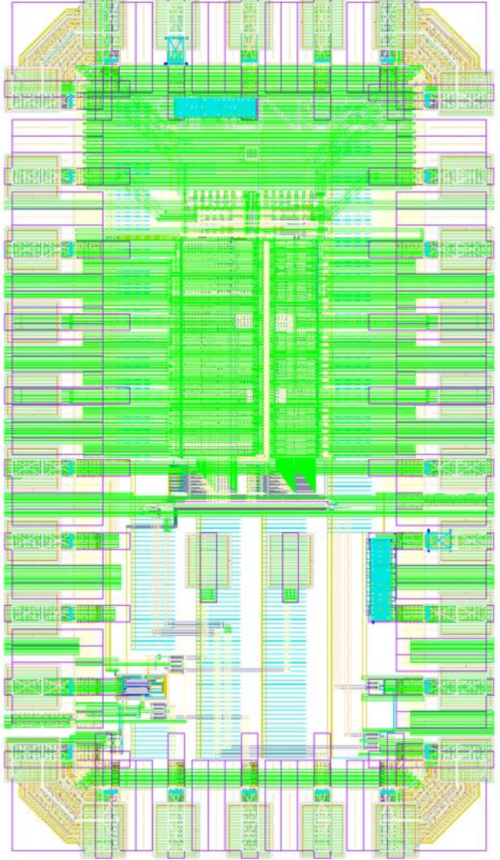
TCAD modelling of radiation effects



- Good fit with 28nm measurements, with special attention to subthreshold
- Modelled effects of individual traps
- Working on extension towards radiation effects

Single device – noise under TID

SIRENS28



Top Design: Semih Ramazanoglu
And Alicja Michalowska-Forsyth

- Measurements TID influence on noise – single devices
- Transistors array (multiple identical transistors) submission to July 2024 run
- Working on extension to statistical results (noise and RTN) on single-devices

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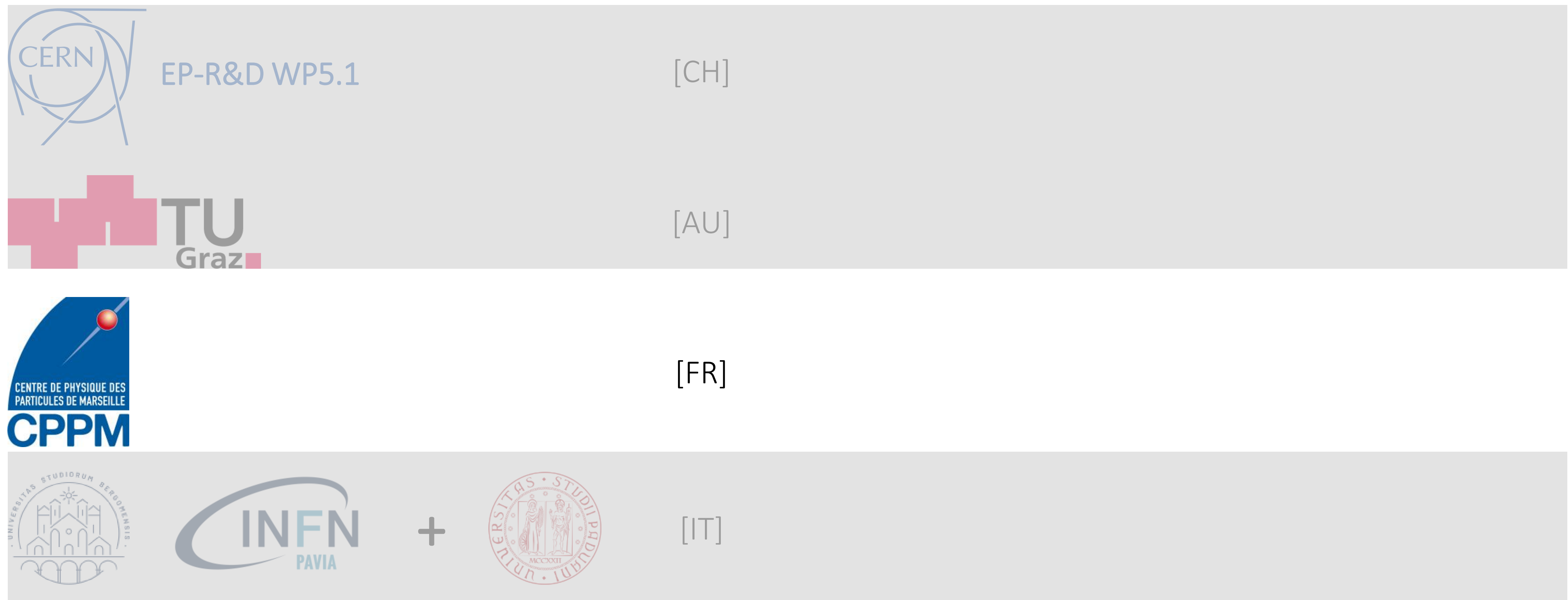
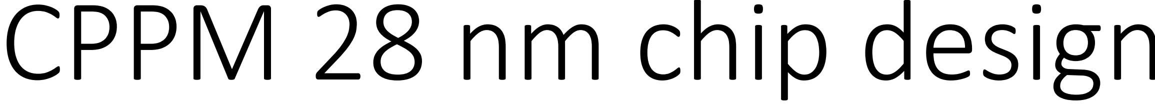
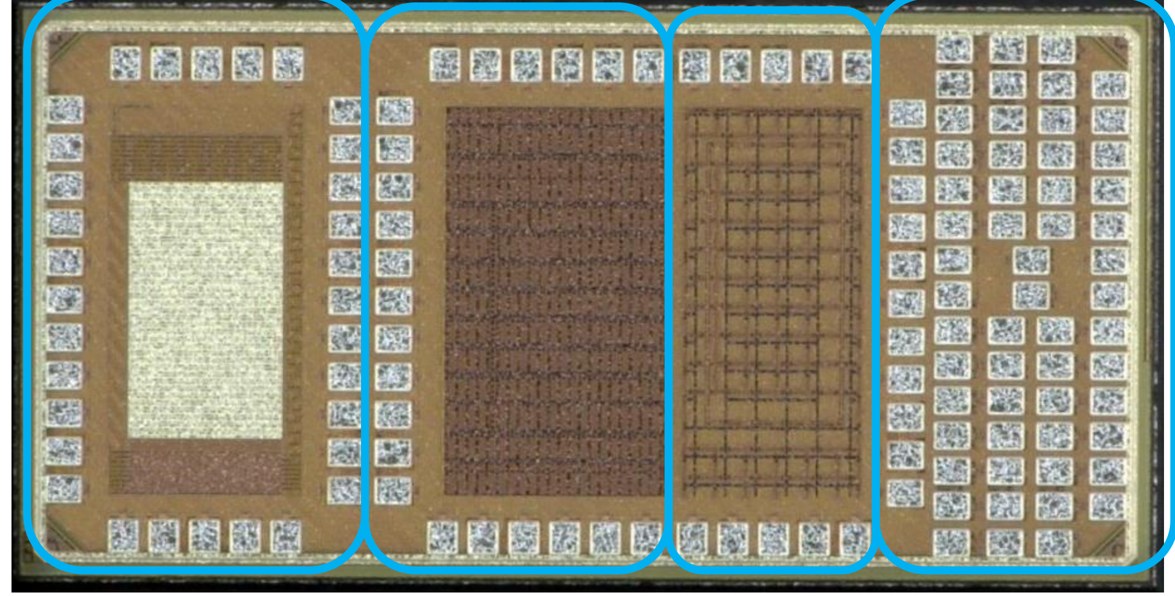




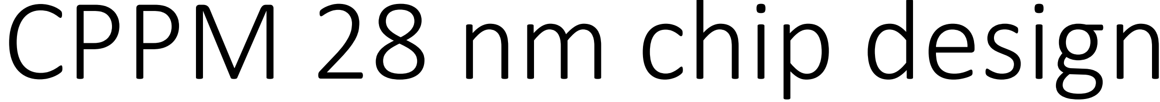
CPPM 28 nm chip design

- R&D on hybrid pixels
  - Process qualification in terms of performance for analog, low-power and low-noise circuits
  - Architecture studies
    - Fast charge amplifier array
- Mini@sics of 2×1 mm2 received June 2023, consisting of 4 main blocks
- Array of 12×36 pixels (432 pixels)
  - Analog pixel array with Fast charge amplifiers for high time resolution
  - Only the analog part is implemented (25×12 μm^2)
- SET test structures
  - Measure the SET pulse width with a good resolution < 20 ps
- Ring Oscillators for TID tests on digital standard cells
- Test structures for TID tolerance studies

Pixel array | SET | RO - TID | Single devices



- **Collaboration and exchange between CPPM and Graz University on various aspects of design and testing**



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Pixel array

SET

RO - TID

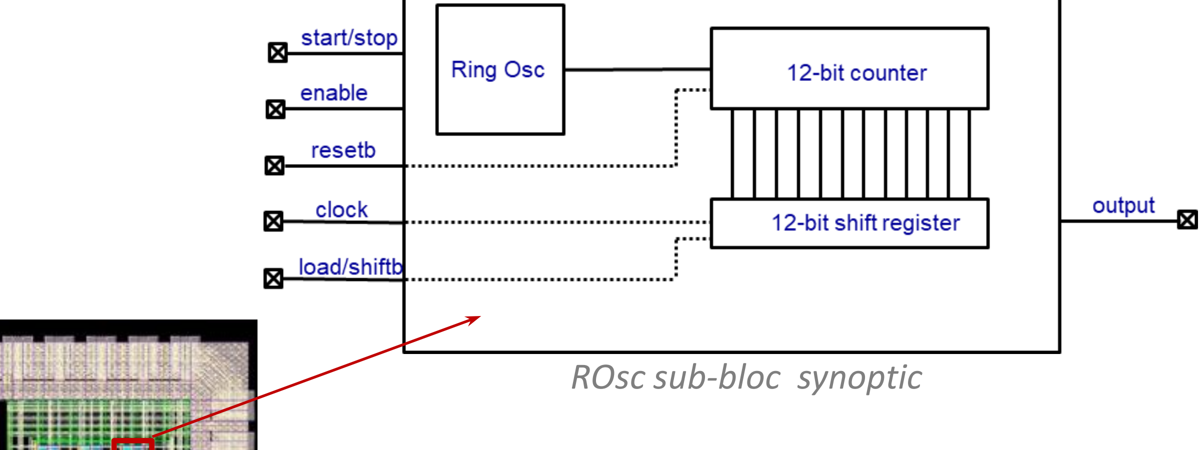
Single devices

- **Collaboration and exchange between CPPM and Graz University on various aspects of design and testing**

- Study of the effect of TID on the performance of digital standard cells
- Timing of combinatorial or sequential cells
- Leakage currents and static power
- Effects of device size on TID tolerance
- Design based on the digital flow
- 96 Rosc sub-bloc
    - Cell size (7T, 9T,12T)
    - Driving (D0, D2, D4)
    - SVT, LVT, HVT

Basic cells	Frequency (MHz)
INVD0	154
INVD2	222
NAND0	118
NAND2	143
NOR0	111
NOR2	139

Simulation



ROsc sub-bloc synoptic

First results

- 2 chips tested
  - Similar results
- Results seems coherent
  - 12T cell faster than 7T
  - LVT faster than HVT
- Issue observed on NAND0
  - check for the firmware and test set-up

cell RO TSMC28nm vs Tp - CHIP1

Propagation Time [s]

2,5E-11
2E-11
1,5E-11
1E-11
5E-12
0

7T measured
9T measured
12T measured

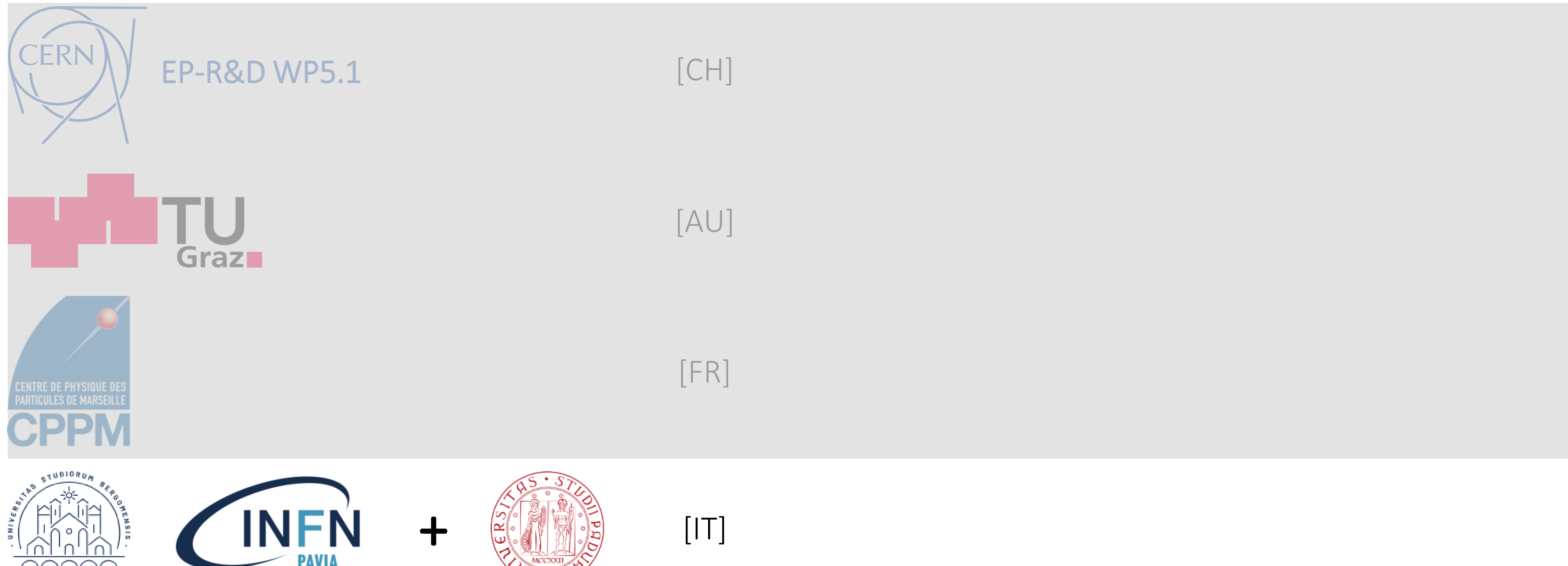
INV0_SVT
INV0_HVT
INV0_LVT
INV2_SVT
INV2_HVT
INV2_LVT
INV4_SVT
INV4_HVT
INV4_LVT
NAND0_SVT
NAND0_HVT
NAND0_LVT
NAND2_SVT
NAND2_HVT
NAND2_LVT
NOR0_SVT
NOR0_HVT
NOR0_LVT
NOR2_SVT
NOR2_HVT
NOR2_LVT

Cell name

Propagation delay versus Cell

7.4.b: EXTREME ENVIRONMENT AND LONGEVITY - RADIATION HARDNESS

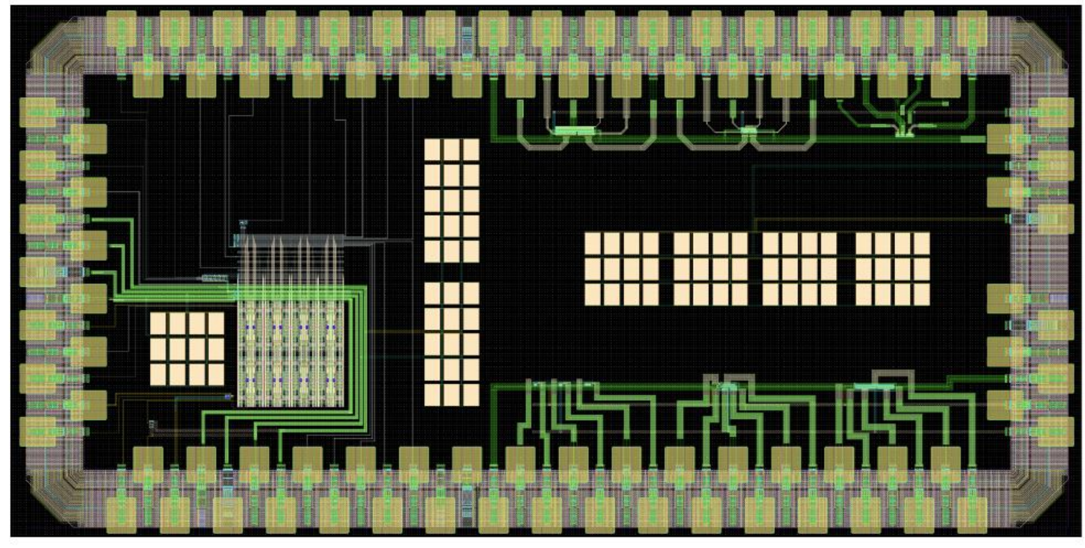
Project: radiation resistance of advanced CMOS nodes

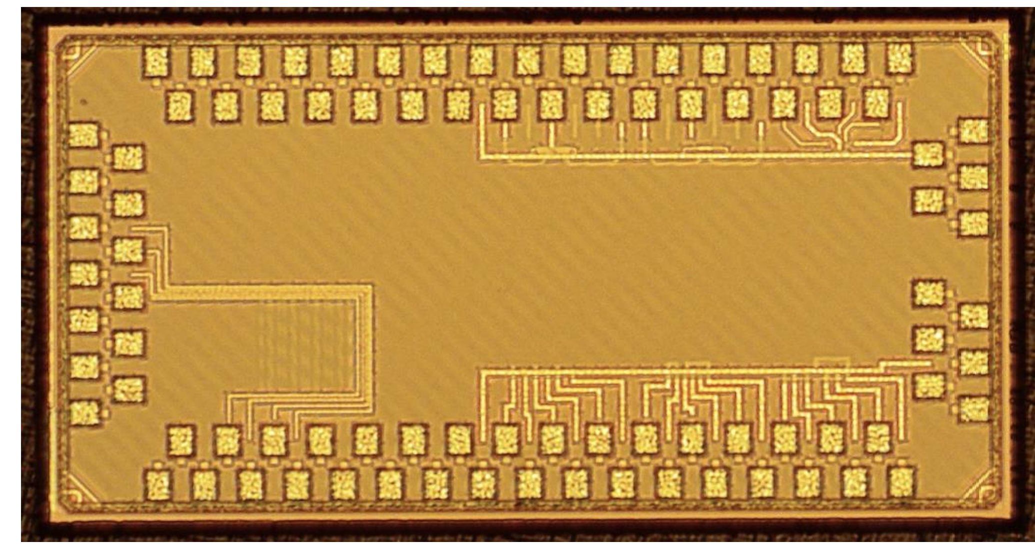


- **Contributors**: Luigi Gaioni[1], Massimo Manghisoni[1], Valerio Re[1], Elisa Riceputi[1], Gianluca Traversi[1], Lodovico Ratti[2], Simone Gerardin[3]
  - 1 University of Bergamo and INFN Pavia
  - 2 University of Pavia and INFN Pavia
  - 3 University of Padova

- **Area of competence**: design of analog front-end circuits and IP blocks for radiation detectors; study of noise and radiation effects in electronic devices and circuits; nanoscale CMOS technologies.

1st submitted prototype





- **Includes:**
  - **standalone NMOS and PMOS** transistors for static and noise characterization
  - **a standalone charge sensitive amplifier (CSA)** for the evaluation of main analog performance parameters
  - **a 4x8 pixel readout matrix** featuring simple digital configuration and readout (shift registers)

TID effects on 28nm MOS transistors

- Investigated devices **irradiated up to 3 Grad(SiO_2)** total dose with X-rays (5.5 Mrad/h dose rate)
- MOSFETs biased during irradiation in the **worst-case condition**
- Slight increase in drain leakage current after irradiation
- **Limited threshold voltage changes** (depending on MOS polarity and geometry)
- Up to 1 Grad, NMOS and PMOS do not feature significant change in their **noise properties** after irradiation

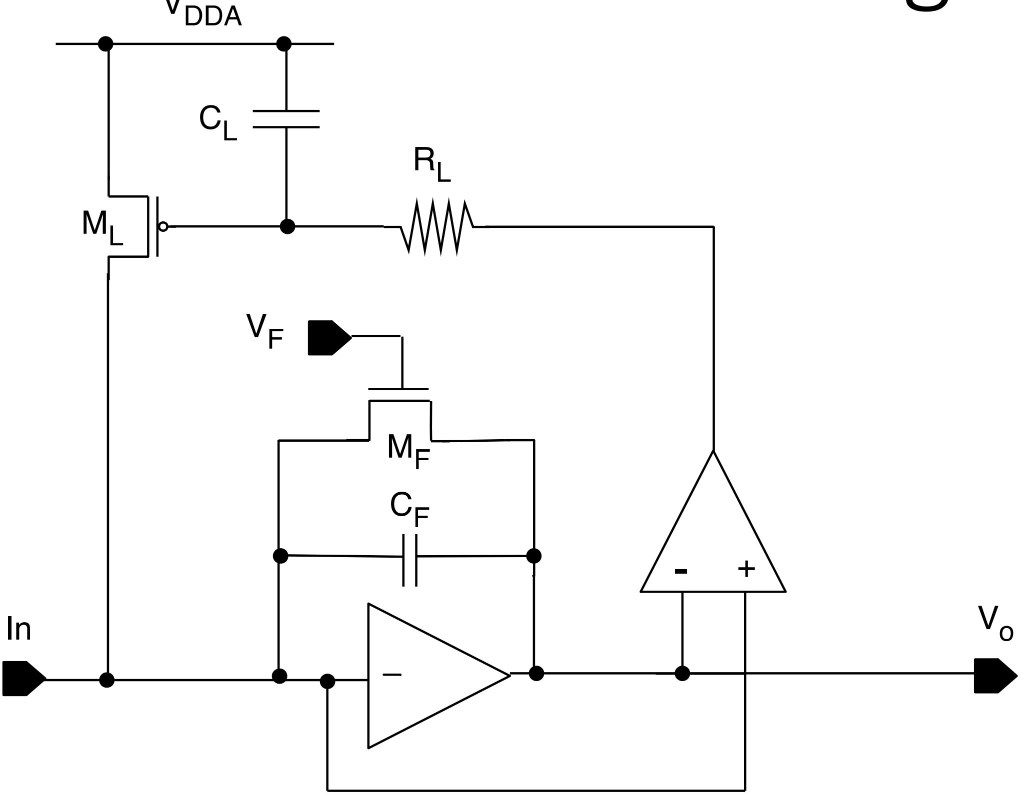
NMOS 100/0.030 V_{DS} = 0.45 V; pre rad, 1 Grad; I_D [A] vs V_{GS} [V]

PMOS 100/0.030 $|V_{DS}|$ = 0.45 V; Pre rad, 1 Grad; $|I_D|$ [A] vs $|V_{GS}|$ [V]

NMOS 200/0.180 I_D = 500 μA; noise_500uA_pre, noise_500uA_1Grad; Noise Voltage Spectrum [nV/Hz$^{1/2}$] vs Frequency [Hz]

PMOS 100/30 I_D = 500 μA; pre rad, 1Grad; Noise Voltage Spectrum [nV/Hz$^{1/2}$] vs Frequency [Hz]

Charge sensitive amplifier design



Auxiliary circuits (not shown in the figure) were integrated to emulate the presence **of detector capacitance** and **leakage current**

- Regulated cascode gain stage + source follower
- Two **independent feedbacks**, one for the discharge of the feedback capacitor and the other for the detector leakage compensation.

Charge sensitive amplifier design

- An **irradiation campaign** has been performed with a target TID of **1 Grad**
- Irradiation at **room temperature**, with a **dose rate** of 5.4 Mrad/h
- No dramatic effects observed:
  - Slight increase in the **ENC**
  - Moderate variation of the **discharge current** associated with a threshold change in the MF feedback transistor

ToT-based front-end: chip layout

- 8x32 matrix of readout channels
- 100 x 25 μm² pixels
- Shared 8-bit Time of Arrival Counter (640 MHz)
- Shared 5-bit Time-over-Threshold Counter (40 MHz)
- SPI controller
- Submitted in July

7.4.b: EXTREME ENVIRONMENT AND LONGEVITY - RADIATION HARDNESS

Project: radiation resistance of advanced CMOS nodes

[CH]

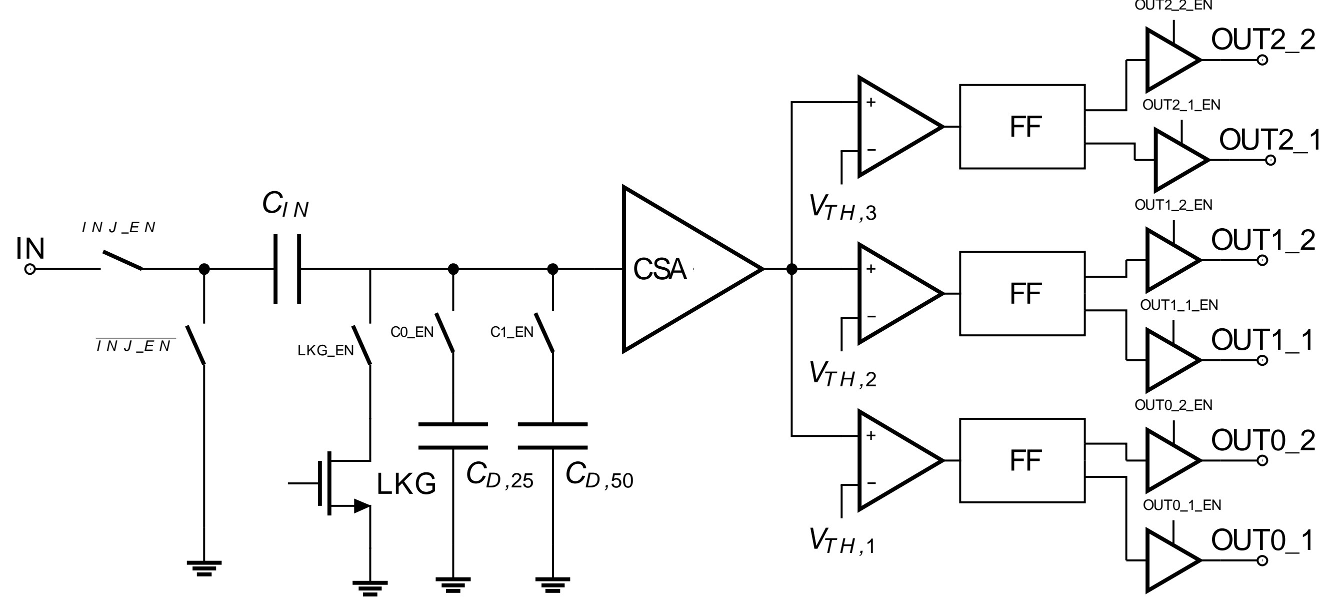
[AU]

[FR]

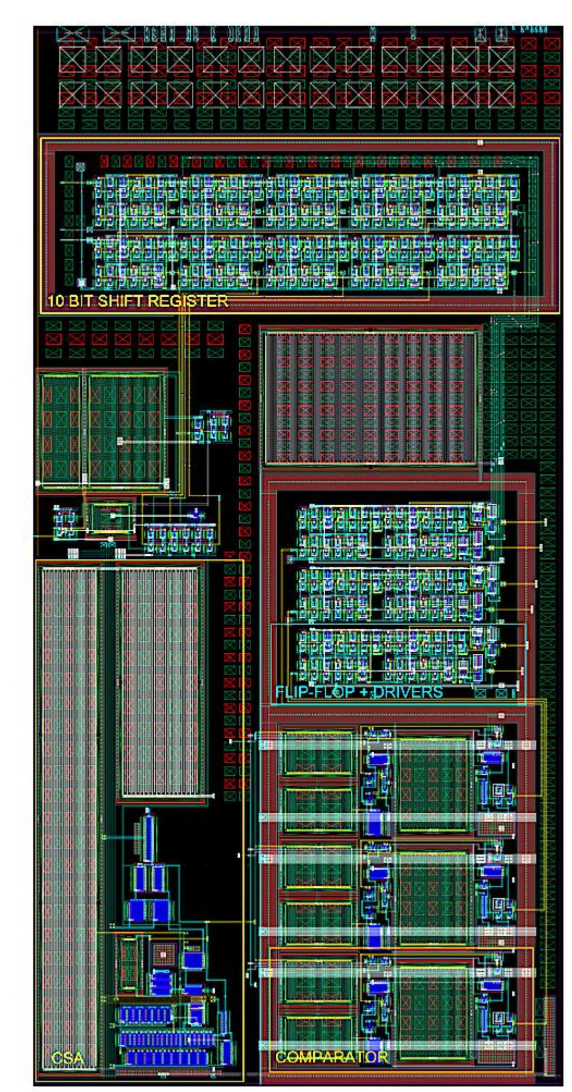
[IT]

BACKUP SLIDES

Flash ADC based front-end

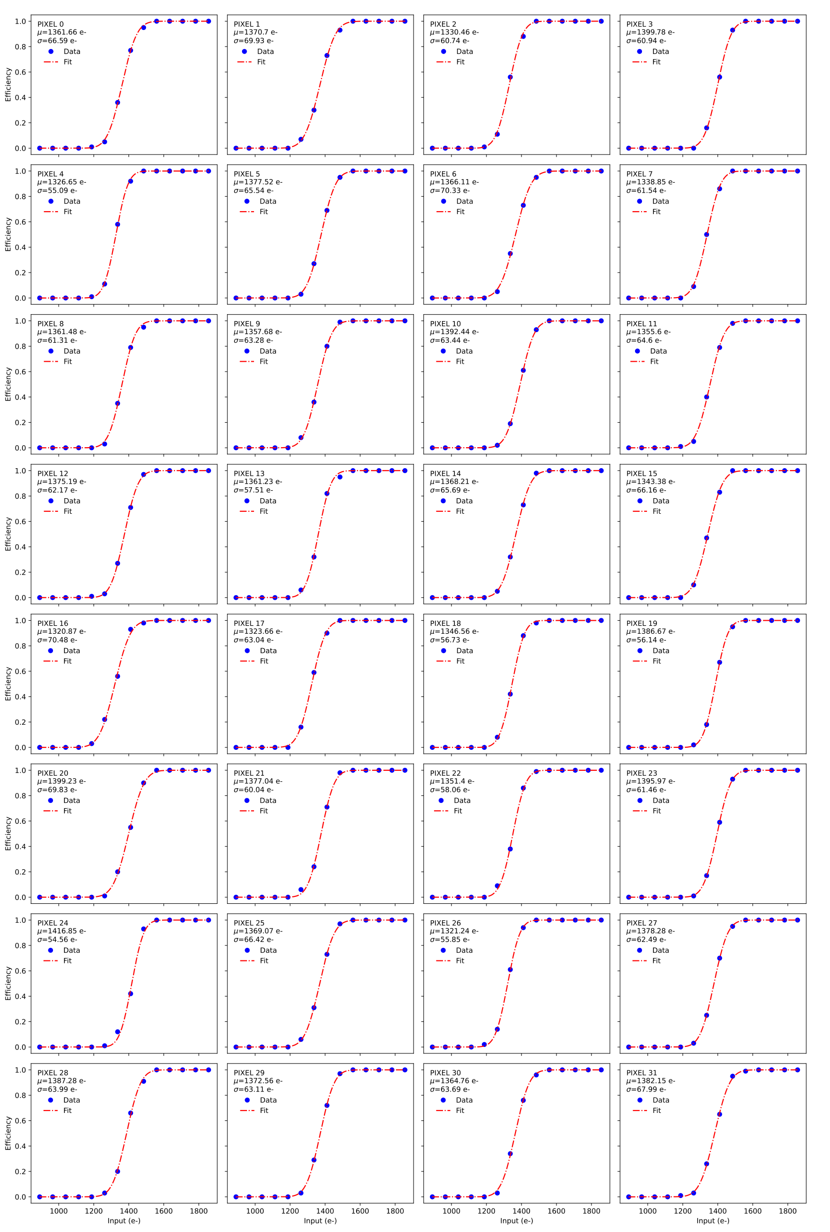


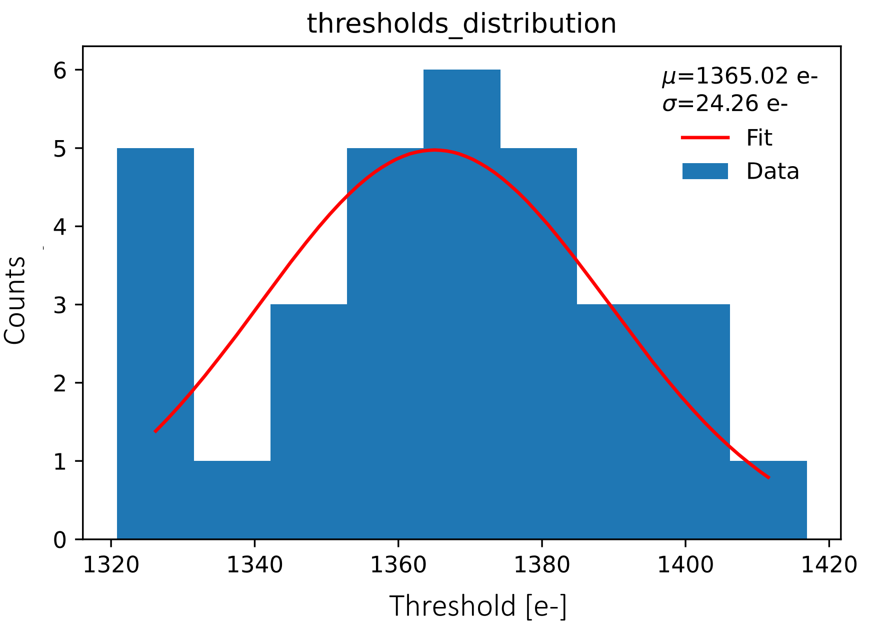
- Preamp (**regulated cascode**) two independent feedbacks
- Ancillary blocks for **detector emulation**

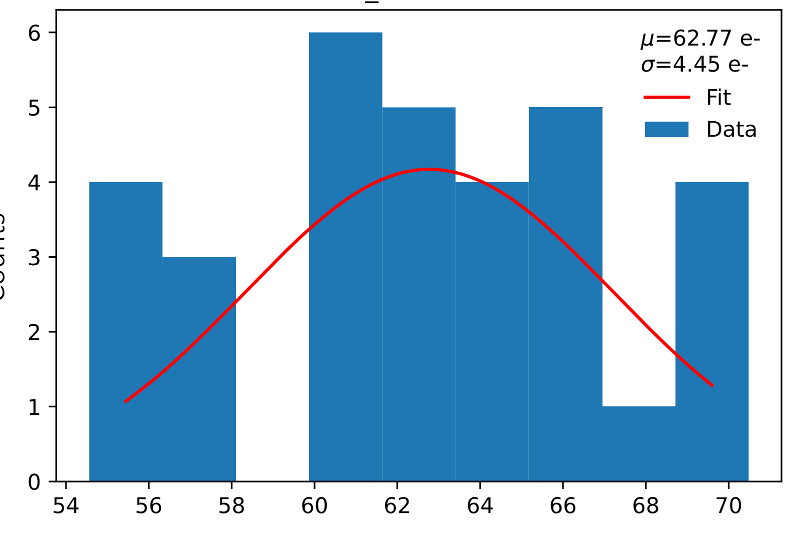


- **AC coupled, auto-zeroed comparators**, operated with 40 MHz clock, implementing a **2-bit flash ADC.** The design is ideally insensitive to device threshold voltage mismatch → threshold tuning DAC not required
- Overall **current consumption**: 5.4 uA → 4.9 µW **power consumption** @ V_{DD}=0.9 V
- Elementary cell size: 25 x 50 µm^2 (analog+digital)
- Submitted in a **8x4 matrix**

Flash ADC front end - Test results







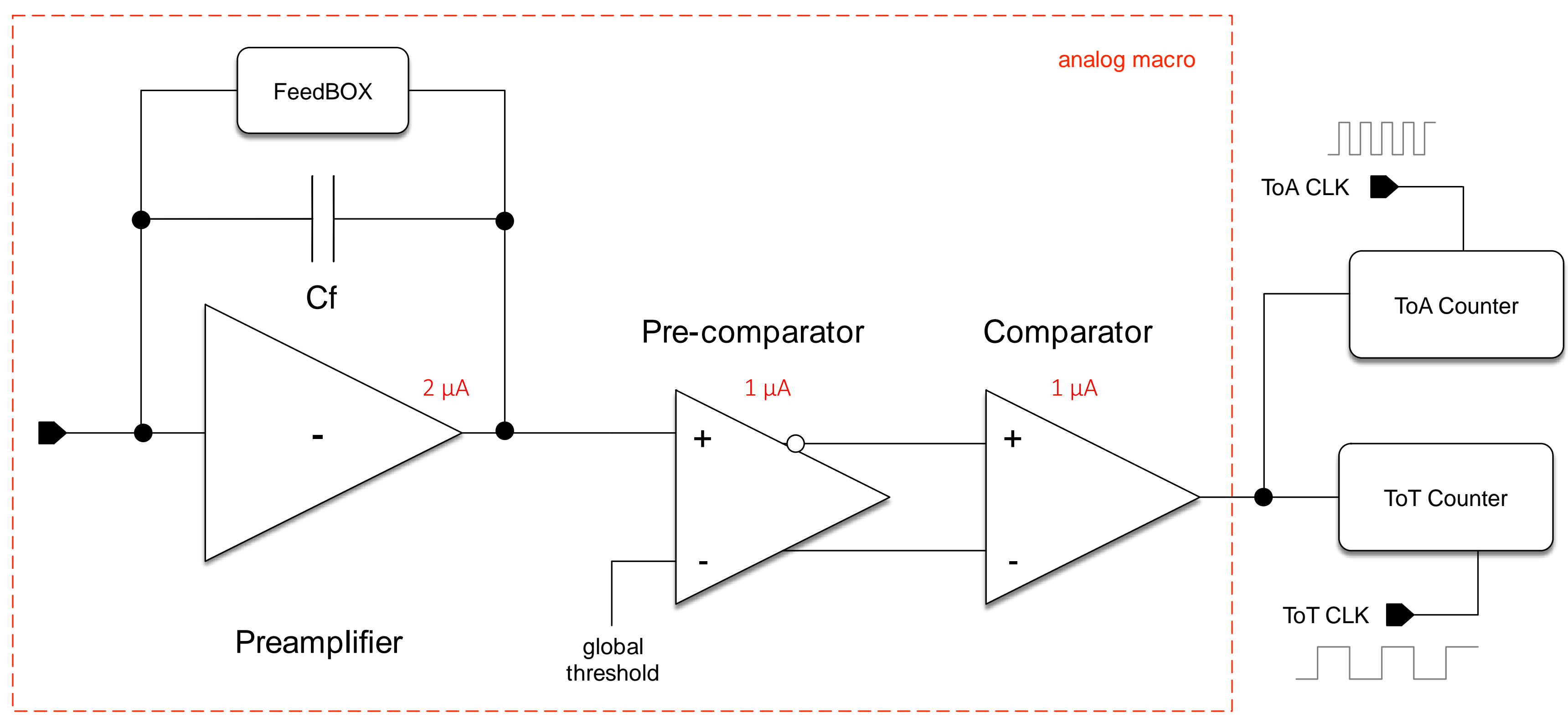
Test @ f_{CLK} = 10MHz

Threshold dispersion ≈ 24 e r.m.s.

ENC ≈ 63 e r.m.s.

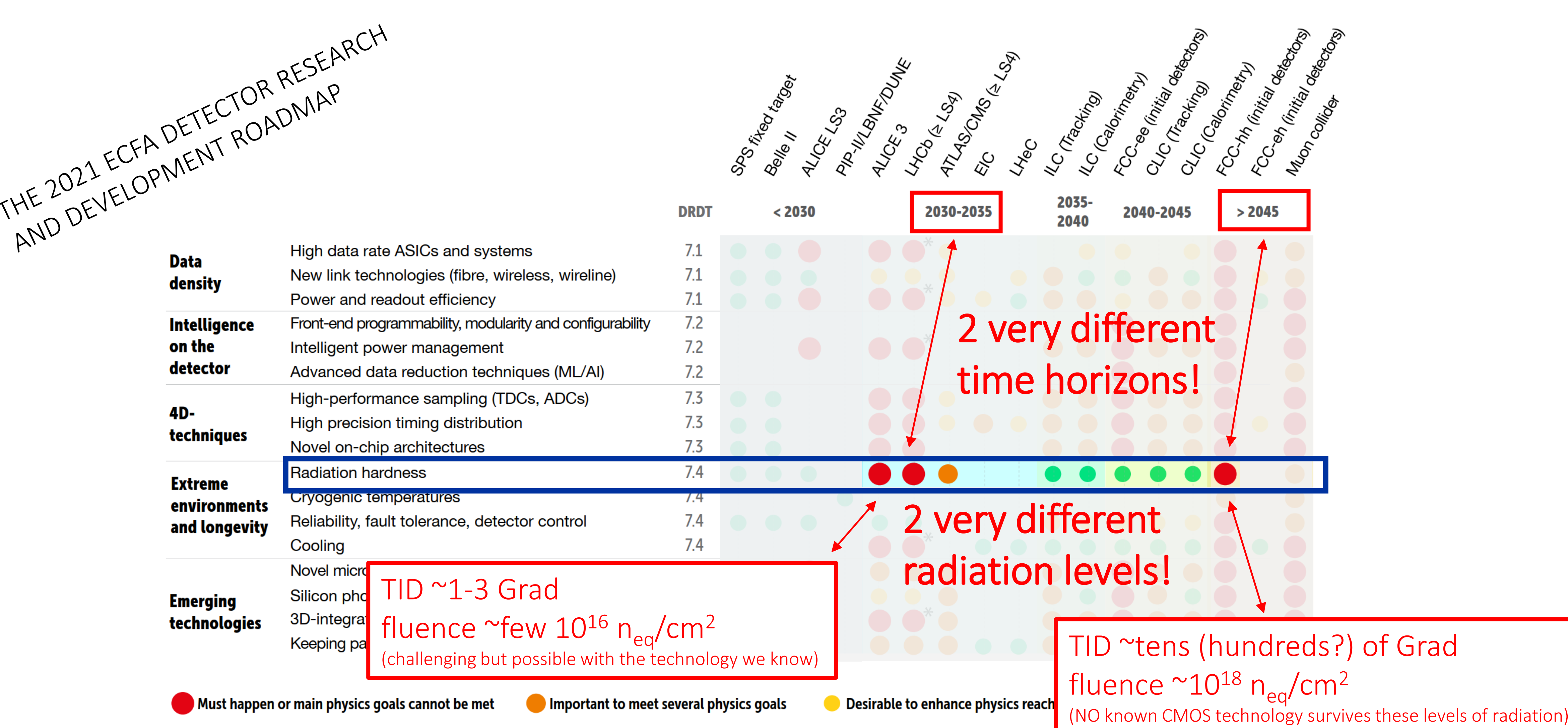
ToT-based front-end

- **A front-end architecture (optimized for very low threshold)** is being developed, based on **Time-over-Threshold (ToT)** → preamp + DC coupled comparator + threshold tuning DAC
    - Self-cascode preamp gain stage
    - Differential comparator architecture to improve the immunity to interferences



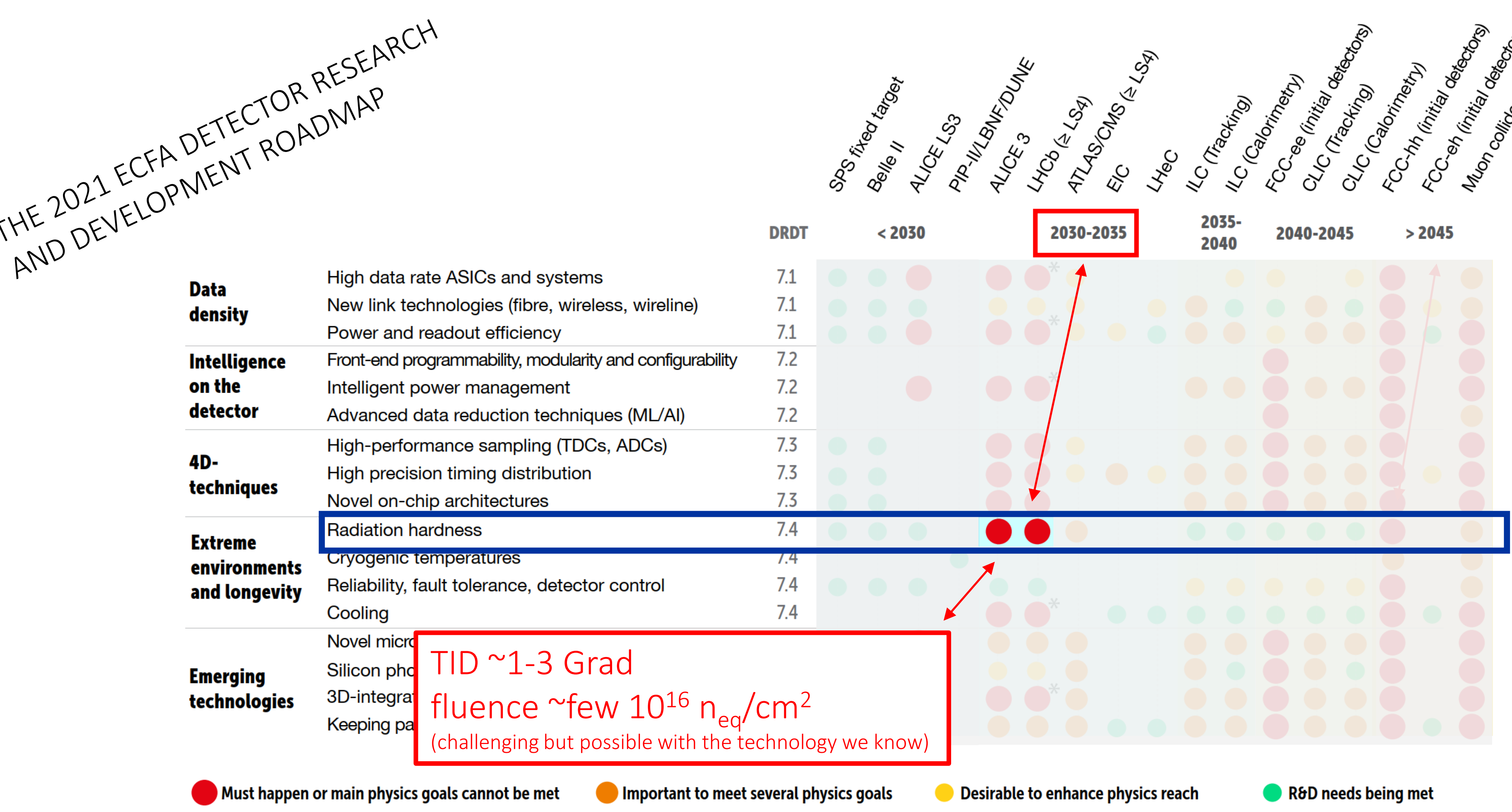
Future steps

- Development of the test setup for the characterization of the ToT-based front-end
- Characterization and radiation qualification of the ToT-based front-end
- Design and characterization of a 28 nm front-end for X-ray imaging applications (ToT conversion with a bi-linear input/output characteristics)
- Development of prototype chip(s) including single devices and IP-blocks with a FinFET technology



EDRRP Group. *The 2021 ECFA detector research and development roadmap*. Tech. Rep. CERN-ESU-017, Geneva, 2020. (https://cds.cern.ch/record/2784893)

THE 2021 ECFA DETECTOR RESEARCH AND DEVELOPMENT ROADMAP



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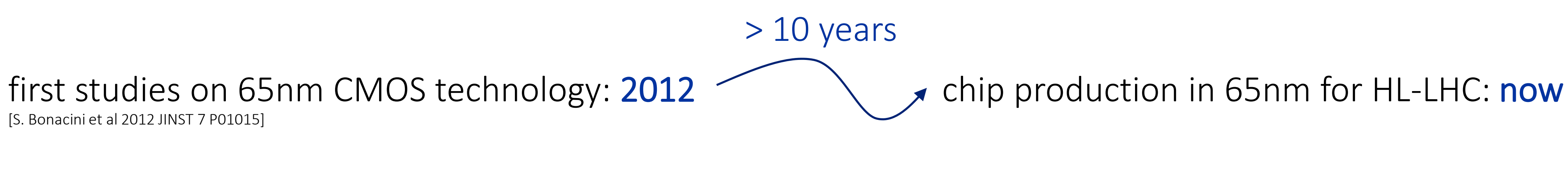


> 10 years

first studies on 65nm CMOS technology: **2012** → chip production in 65nm for HL-LHC: **now**

[S. Bonacini et al 2012 JINST 7 P01015]

chips ready for **2030 - 2035** → the study on radiation effects should have already been started…

… and it was!

TID tests on **28nm CMOS** technology started in 2014!

TID tests on **65nm** imaging technology for **monolithic** started in 2022!

DCDC GaN, iPOL, etc…

research on commercial CMOS technologies is essential!

THE 2021 ECFA DETECTOR RESEARCH AND DEVELOPMENT ROADMAP

SPS fixed target, Belle II, ALICE LS3, PIP-II/LBNF/DUNE, ALICE 3, LHCb (≥ LS4), ATLAS/CMS (≥ LS4), EIC, LHeC, ILC (Tracking), ILC (Calorimetry), FCC-ee (initial detectors), CLIC (Tracking), CLIC (Calorimetry), FCC-hh (initial detectors), FCC-eh (initial detectors), Muon collider

< 2030 | 2030-2035 | 2035-2040 | 2040-2045 | > 2045

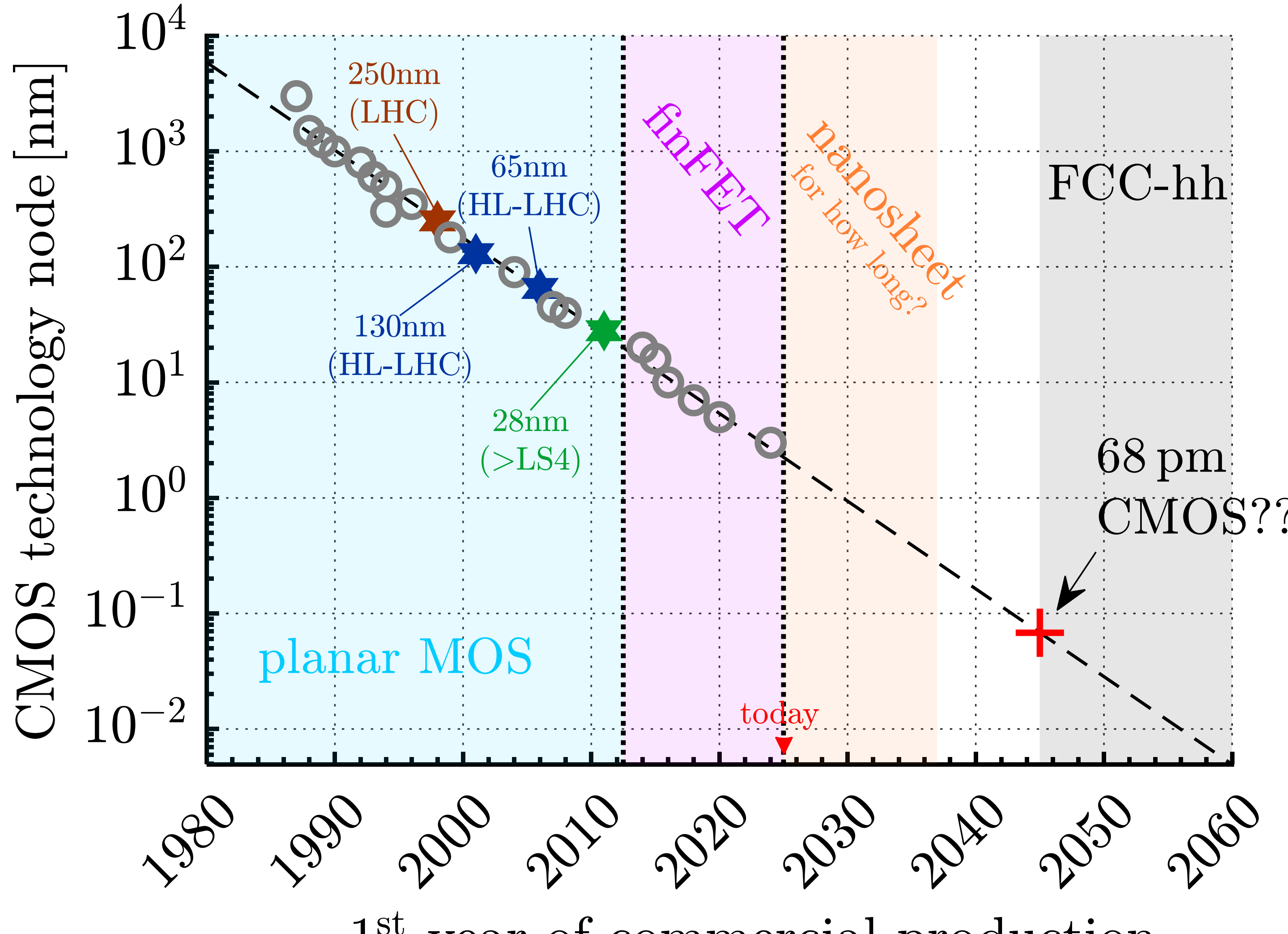
		DRDT
Data density	High data rate ASICs and systems	7.1
	New link technologies (fibre, wireless, wireline)	7.1
	Power and readout efficiency	7.1
Intelligence on the detector	Front-end programmability, modularity and configurability	7.2
	Intelligent power management	7.2
	Advanced data reduction techniques (ML/AI)	7.2
4D-techniques	High-performance sampling (TDCs, ADCs)	7.3
	High precision timing distribution	7.3
	Novel on-chip architectures	7.3
Extreme environments and longevity	Radiation hardness	7.4
	Cryogenic temperatures	7.4
	Reliability, fault tolerance, detector control	7.4
	Cooling	7.4
Emerging technologies	Novel microelectronic technologies, devices, materials	7.5
	Silicon photonics	7.5
	3D-integration and high-density interconnects	7.5
	Keeping pace with, adapting and interfacing to COTS	7.5

Must happen or main physics goals cannot be met | **Important to meet several physics goals** | **Desirable to enhance physics reach**

TID ~tens (hundreds?) of Grad
fluence ~10^{18} n_{eq}/cm^2
(NO known CMOStechnology survives these levels of radiation)

* LHCb Velo

EDRRP Group. *The 2021 ECFA detector research and development roadmap*. Tech. Rep. CERN-ESU-017, Geneva, 2020. (https://cds.cern.ch/record/2784893)



data from:
https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm
https://irds.ieee.org/editions/2022/more-moore

7.4.b: EXTREME ENVIRONMENT AND LONGEVITY - RADIATION HARDNESS

Project: radiation resistance of advanced CMOS nodes

More specific projects are expected to form around:

Specific nodes (e.g., 7nm finfets, 3nm LGAA, etc.)

Specific effects (e.g., low-dose-rates at ultra-high-doses, NIEL scaling, noise, etc.)

Other possible projects:

- “new” or different technologies (e.g., GaN, InGaAs, etc.)
- facilities (how to irradiate to tens of Grad in a reasonable amount of time)
- qualification (how to qualify chips for ultra-high doses)

difficulties: technology accessibility, facility accessibility