WG7.2b
Radiation Tolerant RISC-V SoC

3rd DRD7 workshop

9 September 2024

Project Description

Project Name	Radiation Tolerant RISC-V System-On-Chip (WP7.2b)
Project Description	Develop a radiation-hardened SoC based on the RISC-V ISA standard according to the roadmap defined in M7.2b.1. Topics: 1- SoC architectures 2- Radiation Tolerance design methodology, 3- Verification methodology, 4- SoC generator toolchain. Duration 5-6 years.
Innovative/strategic vision	Develop a technology and a design platform to anticipate and adapt the challenges and opportunities of the future Electronic systems and IC design.
Performance Target	The following targets will be defined in M7.2b.2: Processing Speed Power Consumption Radiation Tolerance Memory and Storage Communication Interfaces Scalability and Flexibility Verification and Testing
Milestones and Deliverables	**M7.2b.1** (M12) Rad-Tol RISC-V SoC roadmap **M7.2b.2** (M24) SoC architectures proposal **D7.2b.3** (M36) Delivery of Rad-Tol SoC building block test chip
Multi-disciplinary, cross-WP content	Electronics Engineering - Digital Design Computer Science - Embedded Systems Systems Engineering - Integration and Testing
Contributors	DE: FH Dortmund BE: KU Leuven CERN UK: UKRI-STFC RAL UK: Royal Holloway University Of London UK: University of Warwick UK: University of Bristol US: Fermilab

Coordinators (1st year)

- Levi Van Der Elst (KU Leuven)
- Kostas Kloukinas (CERN)

Status and Plans reported


Thank You

Milestones & Deliverables

- M7.2b.1 Radiation Tolerant RISC-V SoC roadmap, target 12M
  The target specification of the Radiation-Tolerant System-On-Chip hardware will be defined and a development roadmap will be outlined, and Milestones and Deliverables will be stipulated

- M7.2b.2 SoC architecture and core choice proposals, target 24M
  System-On-Chip topologies, including selected processing cores, will be proposed for implementation and Radiation-Tolerant design and verification methodologies will be established

- D7.2b.3 Rad-Tol SoC building block test chip, target 36M
  Silicon prototyping of the SoC building blocks (processing cores, memories, interconnects, peripherals, auxiliary IP blocks). The SoC prototype test chip will make use of the SoC generator toolchain