DRD7: R&D Collaboration on Electronics and On-detector Processing

Monday 9TH September 2024

Radiation Tolerant RISC-V SoC

TOOLKIT DEVELOPMENT, PROTOTYPE AND APPLICATIONS

Alessandro Caratelli on behalf of the CERN EP R&D WP5.3 team:

Marco Andorno, Alessandro Caratelli, Davide Ceresa, Anvesh Nookala, Kostas Kloukinas

alessandro.caratelli@cern.ch

System-on-Chip (SoC) motivation

With the increasing complexity and manufacturing cost of designs in high energy physics, a shift towards an abstract design methodology will provide:

Introduce Programmability in the detectors

- Allows retargeting an ASIC for different applications
- Change the algorithms at runtime

Simplify system integration and reduce design time

- Introduce modularity with self-contained blocks
- Accelerate digital design and speedup verification
- Accelerate physical implementation

Provide a RadTol Digital IP blocks library

- Provide pre-verified building blocks
- All IPs are coherent with a standardize interconnect
- Helps design reusability within the community

Examples of applications in HEP

Control and monitoring applications

- Stand-alone radiation-tolerant microcontroller – architecture and peripherals customised for application
  - LHC beam monitoring
  - Power management
  - On-detector slow-control operations
  - Detectors monitoring
  - Others…
- Controller embedded in front-end ASICs as pixel read-out chips
  - Dynamic power management
  - Take over and automatise task from the back-end:
  - Possibility to reprogram it in any moment, making it very flexible for new applications

Data processing application – future target

- Data elaboration and pre-processing
- Replace fixed state machines and data pipelines with programmable logic
- Offload performance critical functions to specialized accelerators

A single architecture can't fit all applications!

The SOCRATES - SoC RAdiation Tolerant Eco-System

Open-source kit of tools for generating highly-customizable systems that can be integrated in custom radiation-tolerant ASICs

- automates SoC assembly and verification
- provides a radiation-tolerant verified IPs library
- supports fault-tolerant extensions for redundancy and error correction.
- hardware, verification and software toolchain support

In development within the CERN EP R&D WP5

- Marco Andorno
- Alessandro Caratelli
- Davide Ceresa
- Benoit Denkinger
- Kostas Kloukinas
- Risto Pejasinovic
- Anvesh Nookala

A single architecture can't fit all applications!

The SOCRATES - SoC RAdiation Tolerant Eco-System

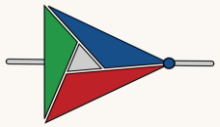
Develop tools to automatise a good part of the design phase

Develop an open-source library of verified fault-tolerant IP blocks

Formulate best practices for SoC design and verification for the HEP community

- By inspiration of what others have done
- By our own experience

The SOCRATES platform



SoCMake
Build System

Pre-verified
IP-blocks library

DEVELOPMENT STAGE:
- ✓ Advanced
- ● Early
- ○ Future developments

Hardware composition

- ✓ Generate the top-level SoC
- ✓ Integrate IP blocks
- ✓ Infer interconnects (crossbars, adapters)

Software generation

- ✓ Invoke RISC-V toolchain
- ✓ Generate hardware abstraction layer (HAL)
- ✓ Generate linker scripts

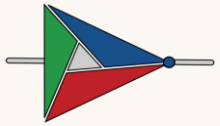
Verification

- ✓ Functional testing environment
- ● SystemC-UVM environment
- ✓ FPGA prototyping

Implementation

- ● Run synthesis and physical implementation flow on targets
- ○ Generate constraints

The SOCRATES platform



SoCMake
Build System

Pre-verified
IP-blocks library

Radiation
Hardening

DEVELOPMENT STAGE:
- ✓ Advanced stage
- ● Early stage
- ○ Future developments

Hardware composition

- ✓ Generate the top-level SoC
- ✓ Integrate IP blocks
- ✓ Infer interconnects (crossbars, adapters)
- ✓ Fault tolerant interconnects
- ✓ radiation-hardened blocks

Software generation

- ✓ Invoke RISC-V toolchain
- ✓ Generate hardware abstraction layer (HAL)
- ✓ Generate linker scripts
- ○ Software fault tolerance

Verification

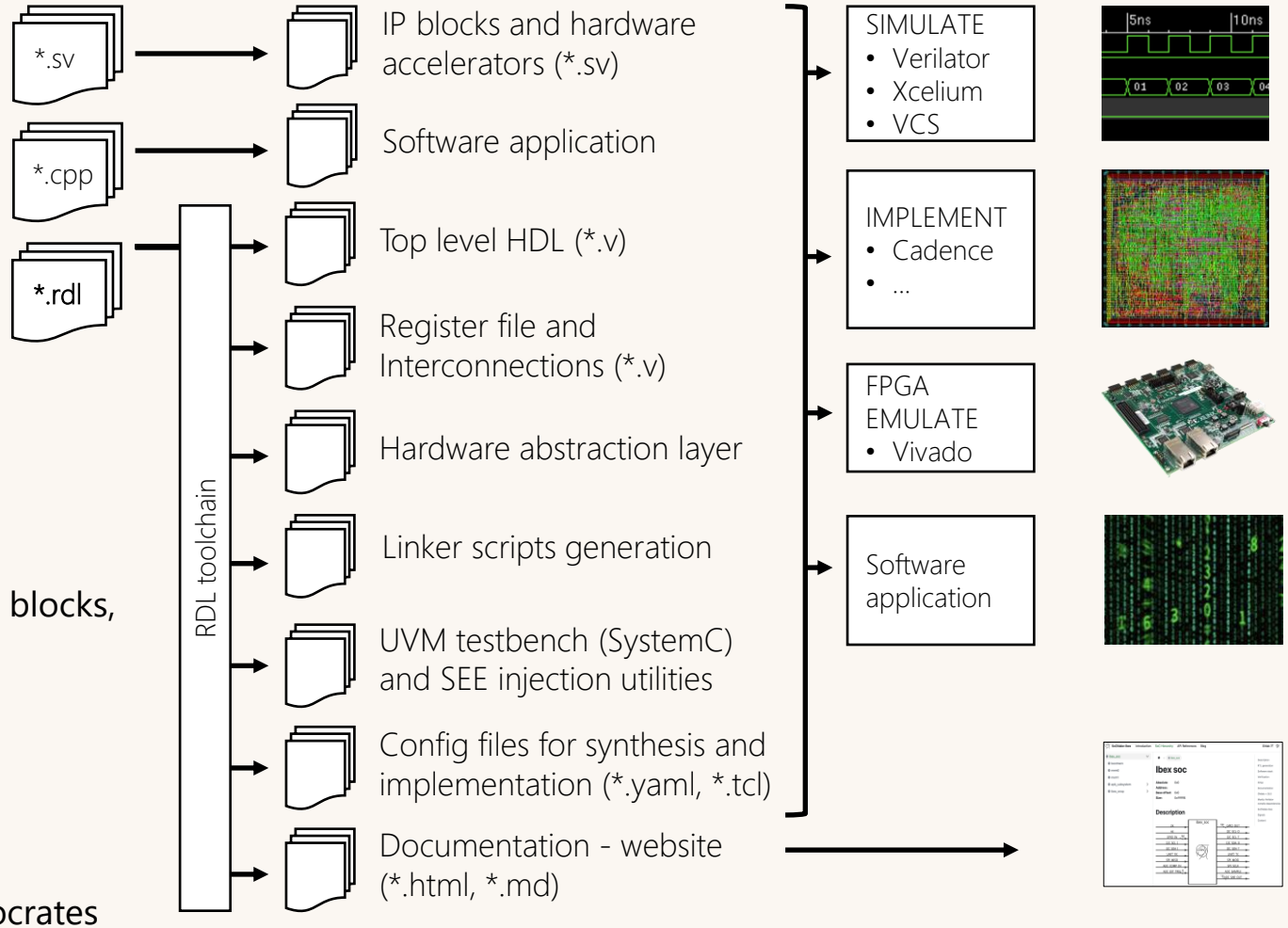
- ✓ Functional testing environment
- ● SystemC-UVM environment
- ✓ FPGA prototyping
- ✓ Fault injection framework
- ○ Formal verification for TMR

Implementation

- ● Run synthesis and physical implementation flow on targets
- ○ Generate constraints
- ○ Constraints for fault tolerance

SoCMake: a HW/SW Build System

- CMake based HW/SW build system for SoCs
- Input configuration in SystemRDL
  - Register Description Language extended for supporting SoC description
  - Used as top-level architecture description
- Rapid prototyping of SoCs:
  - Quick composition of IP blocks into full systems
  - Quickly build different architectures with different IP blocks, hardware accelerators or different CPUs
- Open-source
  - SoCMake:
  - Toolkit and implementation: https://gitlab.cern.ch/socrates



TriglaV – a fully generated prototype ASIC

Goals:

- Demonstrate (and develop) SOCRATES capabilities
- Validate the toolkit and demonstrate the feasibility of using programmable logic inside front-end ASICs.
- Test-drive the HEP 28nm Common Design Platform
- Test the radiation performance and validate the design choices

Design strategy:

- Fully generated with the SOCRATES toolkit
- Target architecture: embedded controller for pixel readout ASICs
- Radiation tolerant design
- Implemented in 28nm bulk CMOS
- focus on introducing observability and testability features to evaluate the radiation tolerance of the design under irradiation testing

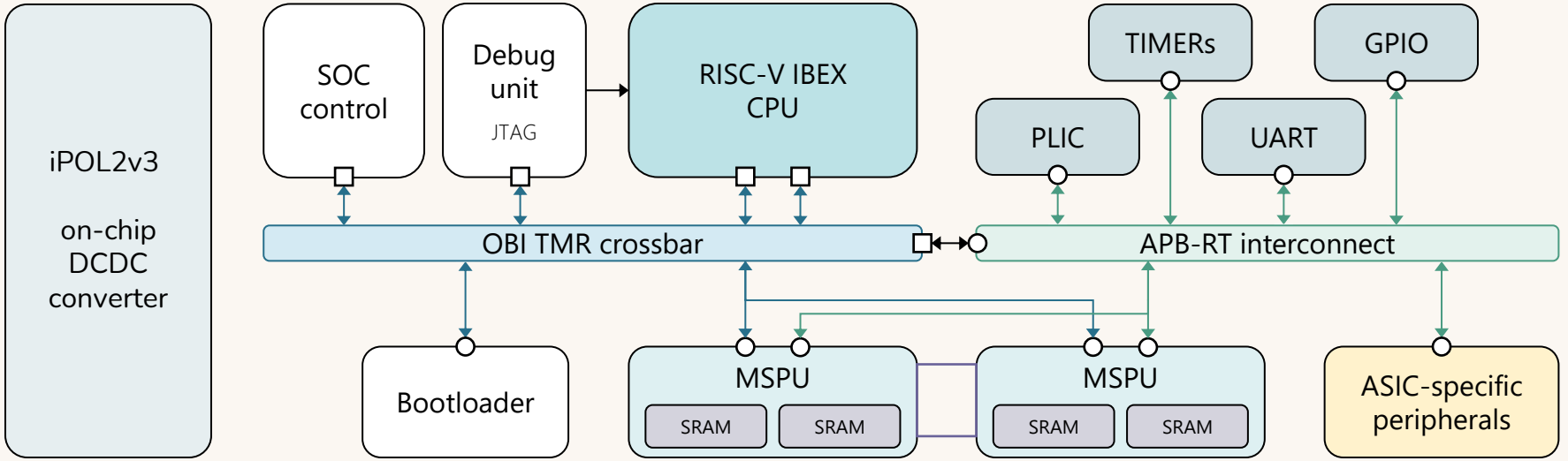
Design submission:

- MPW run in 28nm scheduled for the 30th October 2024

TriglaV – a fully generated prototype ASIC

CPU choice: IBEX (Zero-risky) [1] maintained by LowRISC
- Fully triplicated in TriglaV – TMR formal verification and fault-injection
- In parallel studies for selective protect CPU components and handle faults [2]

Minimum set of peripherals is included
- SoCMake handle triplication, integration and HAL generation



On-chip resonant DCDC converter
- Designed by the EP R&D WP5.2
- Possibility to disable it to power TriglaV via dedicated pads

ASIC-specific peripherals
- SoCMake handle the integration of custom peripherals needed for the target ASIC

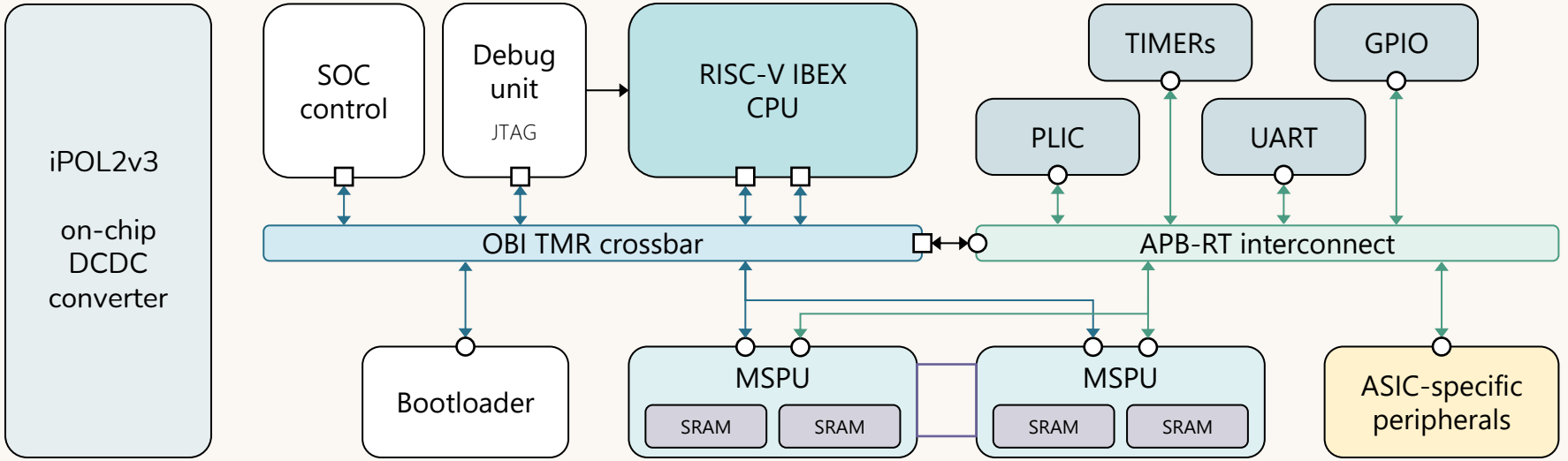
[1] P. Davide Schiavone et al., *Slow and steady wins the race? A comparison of ultra-low-power RISC-V69cores for Internet-of-Things applications*, *PATMOS* (2017) pp. 1-8.70

[2] A. Nookala et al., *Soft-error Reliability Analysis and Error Rate Estimation for RISC-V Processors in High Energy Physics Environments*, NSREC (2024), draft for IEEE TNS 2025

TriglaV – a fully generated prototype ASIC

OBI-TMR crossbar
- Fully triplicated
- multi-master

APB-RT interconnect
- encoded data and address busses – triplicated control
- Single-error correction double-error handling in software



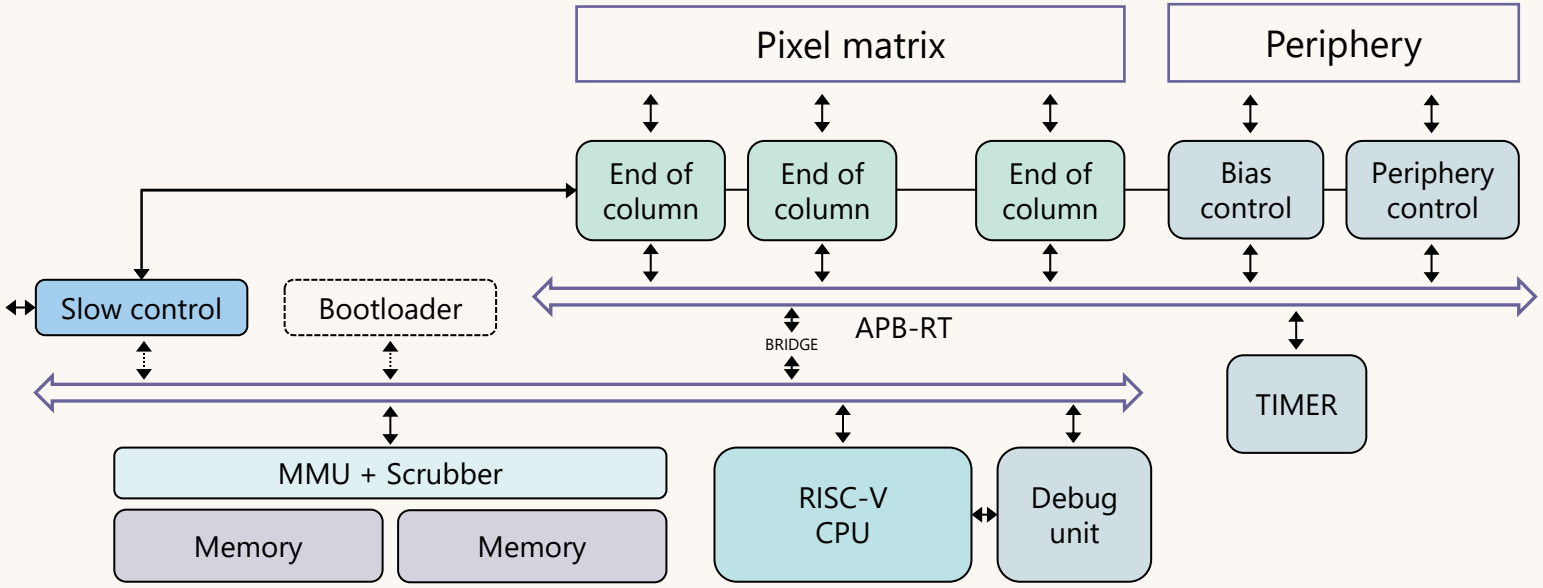
Memory Scrubbing and Protection Unit (MSPU)
- Dual-port commercial SRAM
- Bit interleaving, ECC (Hamming encoded 13-8)
- Periodic scrubbing
- Status: design, implementation and verification complete

Example of application: Picopix

Picopix is a large-area Particle Tracking detector ASIC with < 30 ps_{RMS} timing resolution, on-chip clustering support, and output bandwidth of 102.4 Gb/s

The design targets requirements for: ▪ LHCb VELO detector ▪ rad-hard monitoring systems ▪ beam-gas monitoring, ▪ X-ray and Neutron imaging ▪ Time-resolved photon processing science (Mass spectrometry, X-ray photon correlation spectroscopy, etc.)

A programmable controller, generated with SOCRATES, will take over several back-end low-computational tasks:



- Automatize recurrent monitoring and control operations
- Bias monitoring
- Calibration, threshold trimming
- Send "commands" instead of accessing directly configuration registers
- Reprogram it in any moment, making it very flexible for new applications

Next steps

Prototype milestones:

- Complete design, simulation and implementation in 28nm of the TriglaV chip
- MPW run in 28nm scheduled for the 30th October 2024
- Testbench development and characterization of the TriglaV radiation tolerance and fault protection performance

Road to SOCRATES platform release reediness:

- Expand SoCMake capabilities and make it user-friendly for people to use and contribute
- Expand and maintain an open-source radiation tolerant IP library
- Deliver open-source toolkit to the HEP community
- Formulate best practices on verification and fault-injection verification
- Continues studies on fault-protection on programmable components and develop strategies
  - Selective triplication
  - Fault tolerant hardware architectures
  - Software/hardware error handling
- Maintain and support integration in other front-end ASICs / stand-alone controllers

KU LEUVEN

DRD7 Workshop

Radiation Tolerant RISC-V Processors

Stefan De Raedemaeker

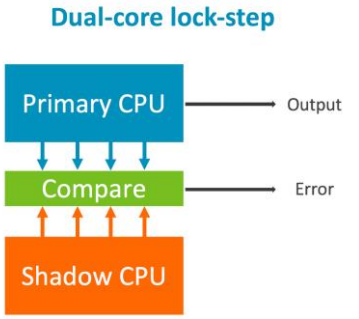
Electronic Circuits and Systems (ECS ESAT)
Advanced Integrated Sensing Lab (ADVISE)

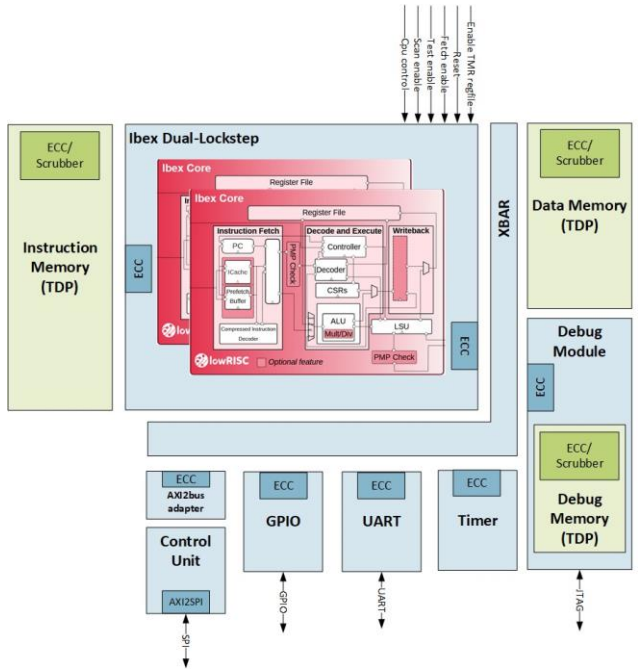
Radiation Tolerant Dual-Lockstep Ibex SoC

- Open source 32-bit RISC-V CPU
- Ibex security features
  - **Dual Lockstep,** Alert outputs, ECC, Bus integrity checking, Glitch detection, Hardened PC, …

“Can these built-in security features be used to detect SEUs within the Ibex core?”

- 2 identical Ibex Cores, ECC on bus and memories





https://iiw.kuleuven.be/onderzoek/advise

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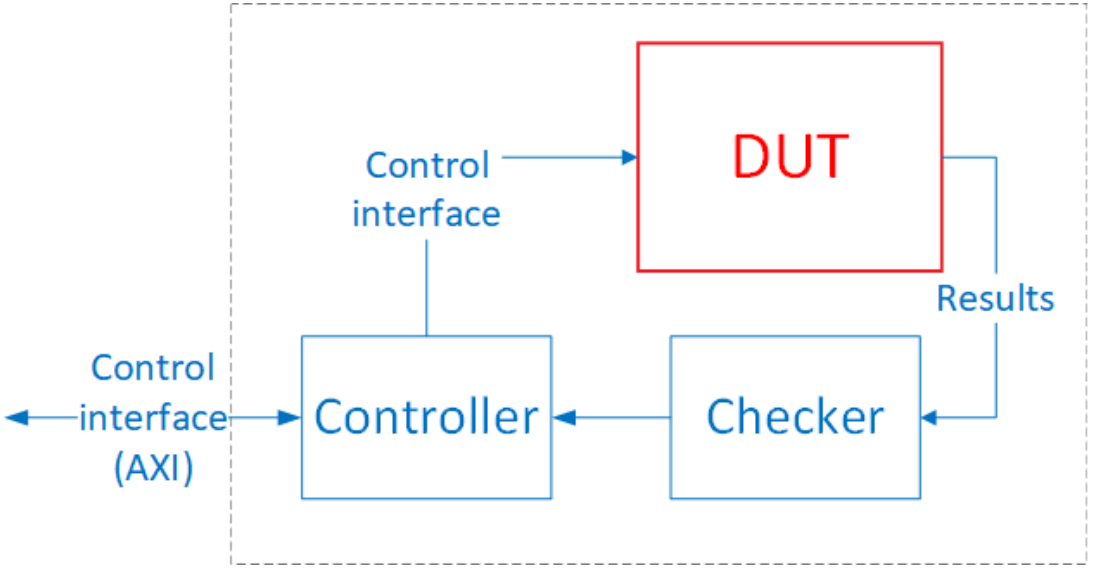
SEE (SET/SEU) verificatie

- SEU inject test platform
  - In simulation testing
  - At runtime (FPGA) testing
  - Formal verification
  - Reduce Fault Space
    - STA (e.g. SET in setup-hold window)
    - PnR (MBU, MCU, ...)

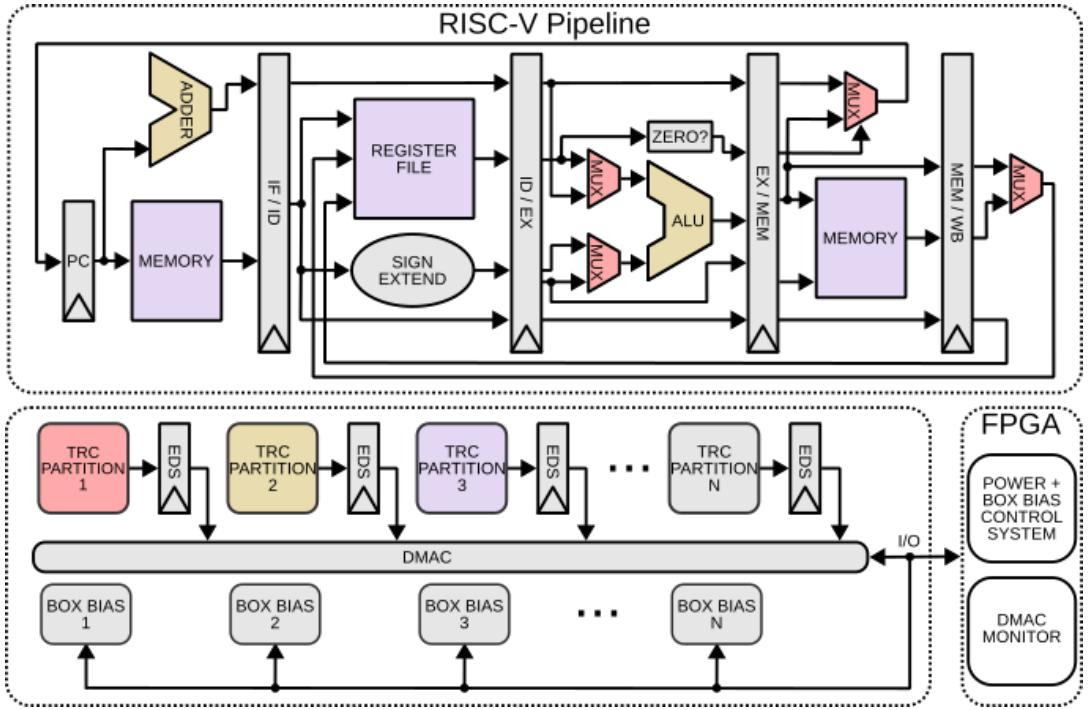


“Can a SEU inject platform formally verify correct behavior in RISC-V processors?”

Tunable Replica Circuits in RISC-V

- Positional or logical grouping for TID monitoring
  - Failing Tunable Replica Circuits (TRC) paths predics TID related timing errors
  - TRC informs error detection system to take action before TID effects happen.
  - Dynamic Voltage and Frequency Scaling (DVFS) to mitigate TID effects.
- Implement in deep-nm FinFET

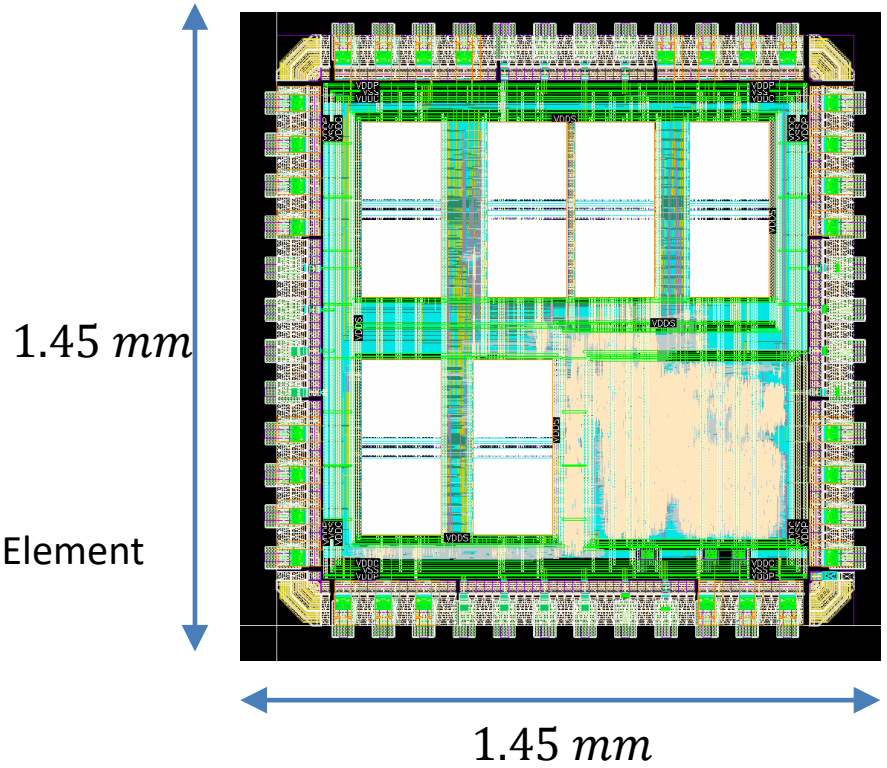
“Can TRC reliably predict TID related errors and can we prevent it with DVFS?”

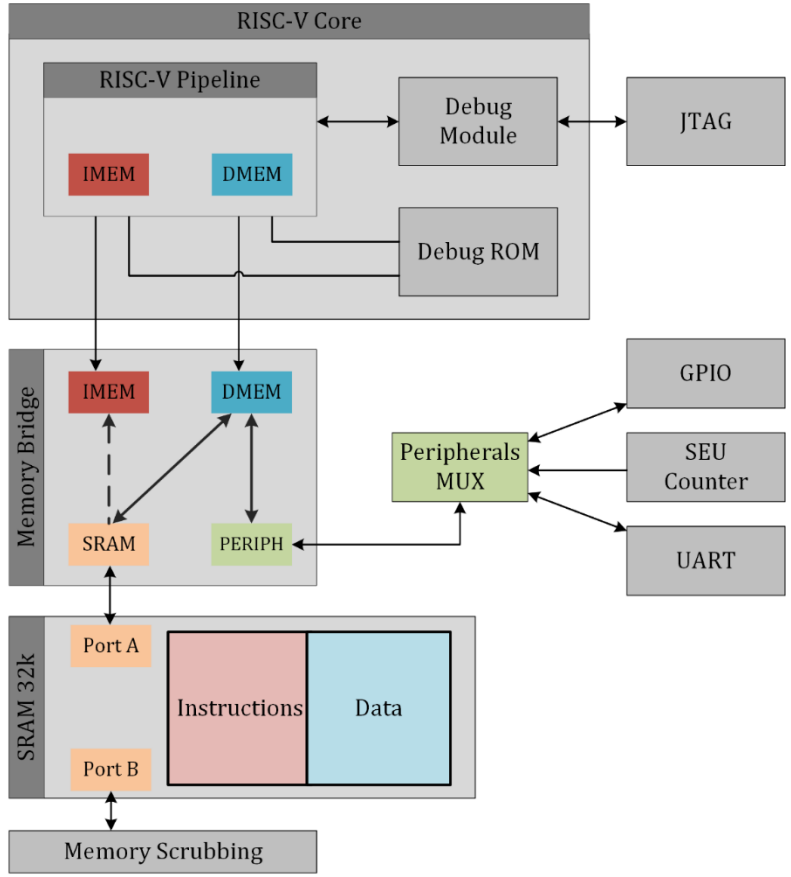


Fachhochschule Dortmund
University of Applied Sciences and Arts

STRV-R2 Radiation Hard RISC-V Microcontroller in 28nm

- 1.45mm x 1.45mm in 28nm Technology
- RV32-IMC Core
  - 3 stage pipeline
  - Multiplication extensions
  - 100 MHz @ 0.9V
  - Fully triplicated core
- TMR Strategy in RISC-V Core:
  - Triplication of
    - All sequential elements
    - All combinational logic
  - Majority voters after each sequential Element
  - Additional feedback path
  - Three separate clock-trees
  - SEU Detection Counters
- TMR SRAM Strategy:
  - 3 Dual-Port SRAM Instances
  - Scrubbing on second SRAM port
  - 3x 32Kbyte

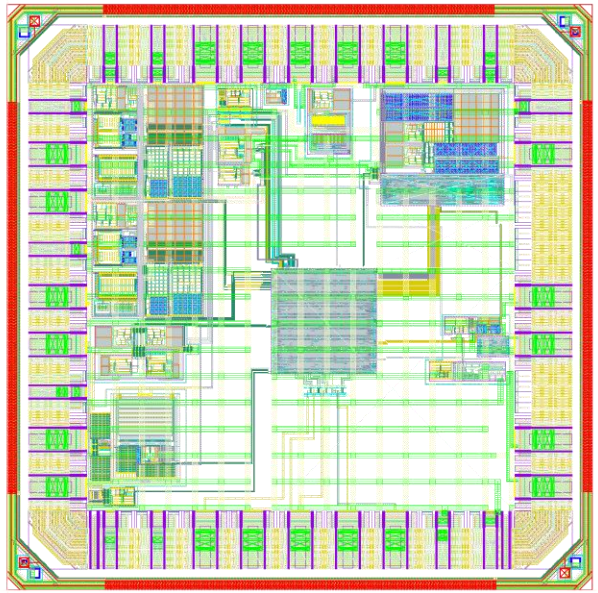


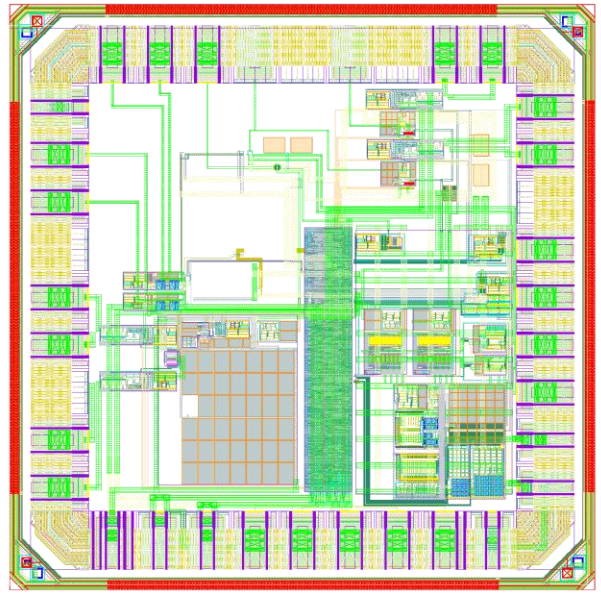


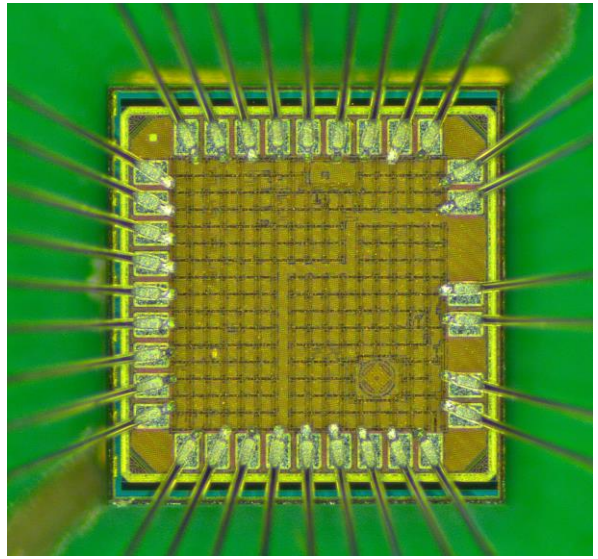
Submitted to production in early September 2024

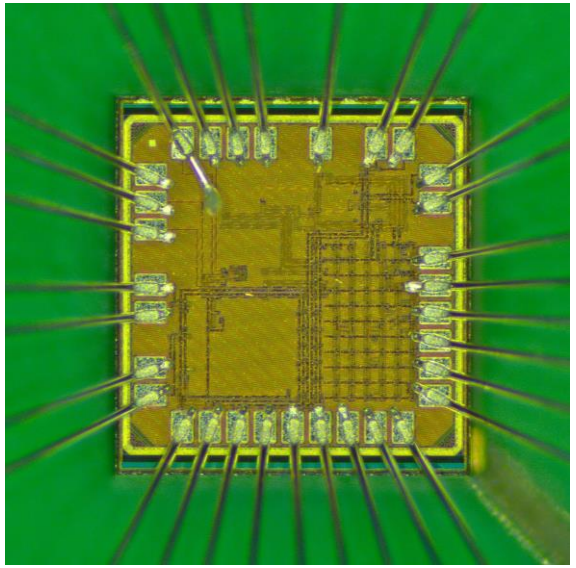
Science and Technology Facilities Council

DRD-UK Update







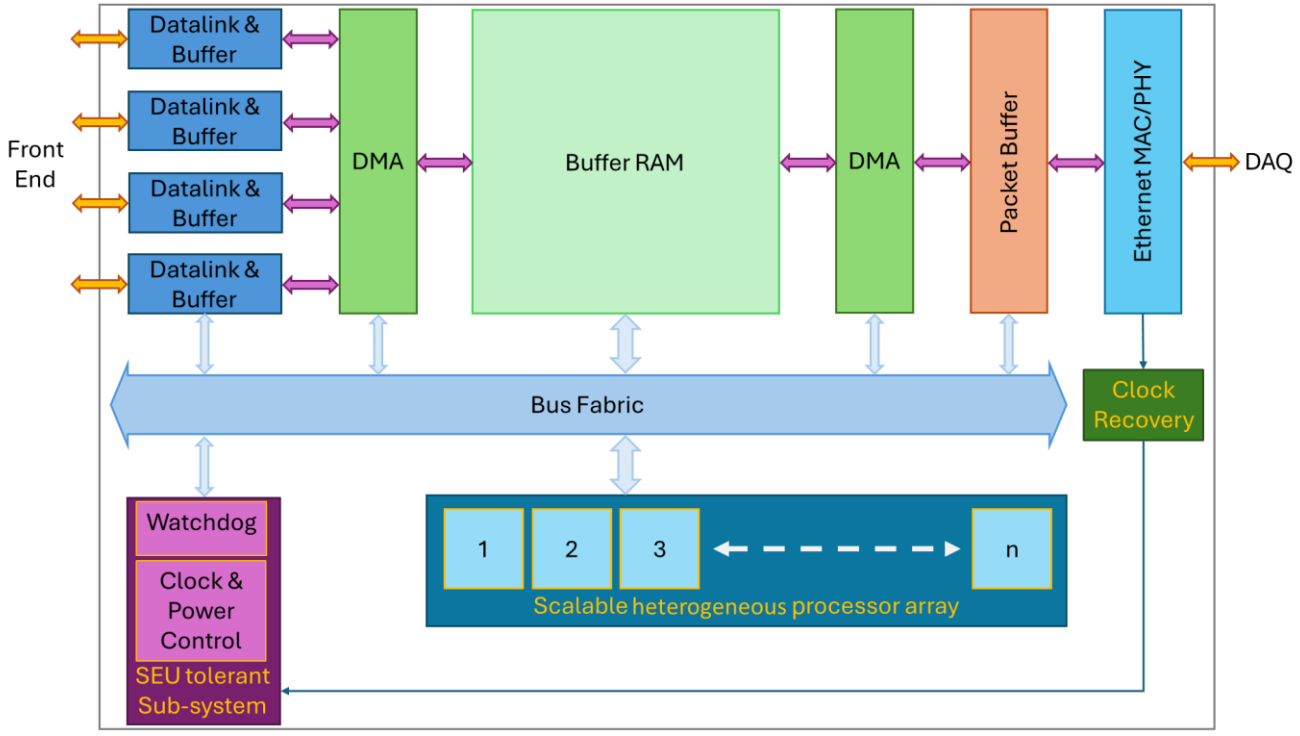


Mark Prydderch – RAL ASIC Design Group Leader

on behalf of the collaboration

mark.prydderch@stfc.ac.uk

DRD-UK: Common Interface ASIC proposal



Proposed common interface ASIC for detector readout, timing, & control

Reminder:

- Aim to couple a range of specialised FE ASICs to a common industry-standard off-detector interface.

Progress:

- ✓ DRD-UK Steering Committee selection ← Pass
- ✓ STFC Early-Stage R&D sifting ← Pass
- ✓ STFC Early-Stage R&D full proposal submitted
  - ❑ Review panel meets in November 2024.
  - ❑ Funding for 1.5 FTE/year & two test structures + PCBs.
  - ❑ 5 to 10% contribution of effort from RAL PPD & university partners.
- Existing 28nm IP test structures work as expected – Next step irradiation by Birmingham & Oxford
- Brunel joined consortium

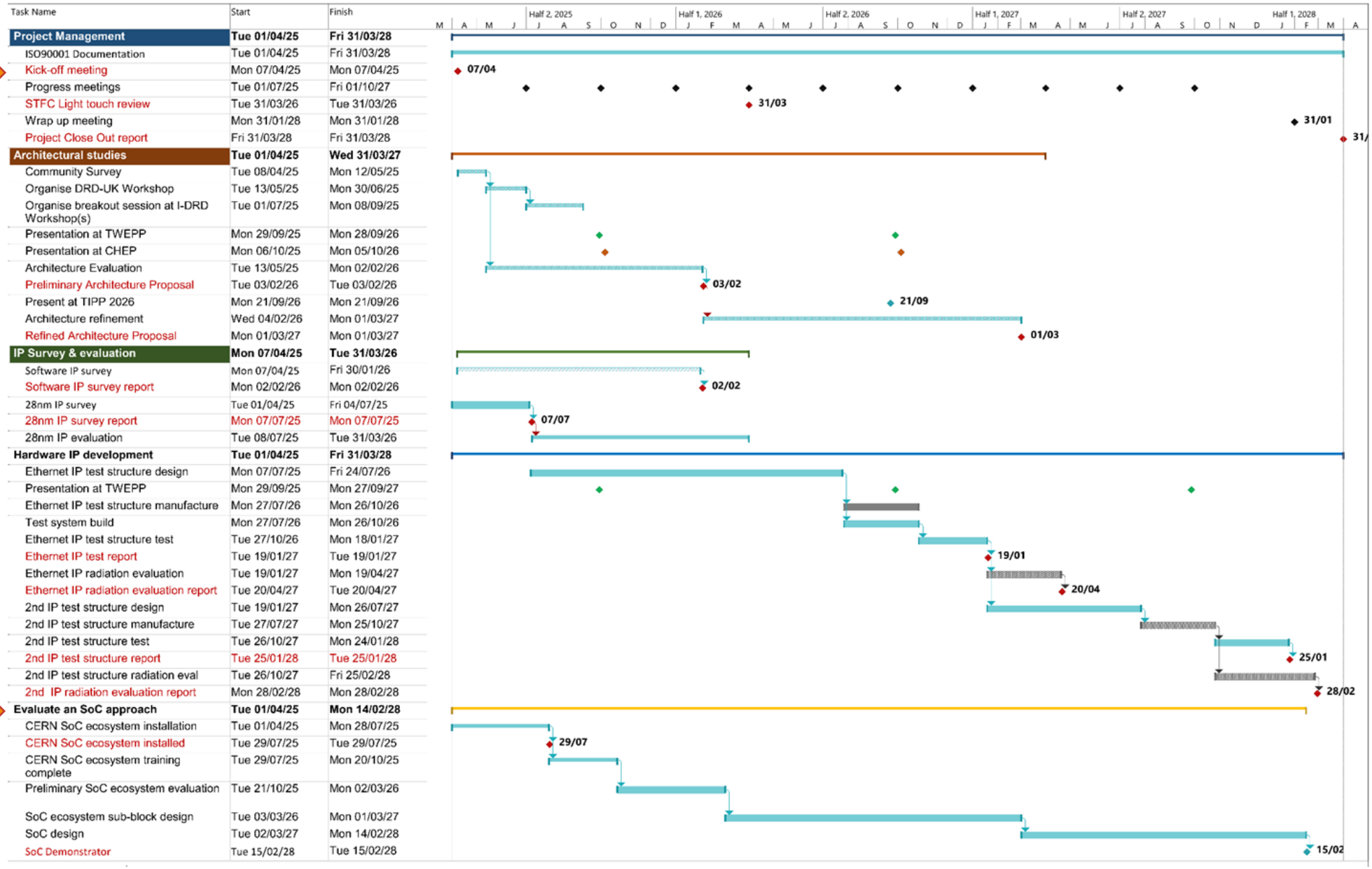
UKRI Science and Technology Facilities Council · The University of Manchester · The University of Warwick · University of Birmingham · University of Oxford · Brunel University London

DRD-UK: Common Interface ASIC plans

- Early-stage proposal start April 2025

SoC ecosystem evaluation one WP of the project

Task Name	Start	Finish
Project Management	**Tue 01/04/25**	**Fri 31/03/28**
ISO90001 Documentation	Tue 01/04/25	Fri 31/03/28
Kick-off meeting	Mon 07/04/25	Mon 07/04/25
Progress meetings	Tue 01/07/25	Fri 01/10/27
STFC Light touch review	Tue 31/03/26	Tue 31/03/26
Wrap up meeting	Mon 31/01/28	Mon 31/01/28
Project Close Out report	Fri 31/03/28	Fri 31/03/28
Architectural studies	**Tue 01/04/25**	**Wed 31/03/27**
Community Survey	Tue 08/04/25	Mon 12/05/25
Organise DRD-UK Workshop	Tue 13/05/25	Mon 30/06/25
Organise breakout session at I-DRD Workshop(s)	Tue 01/07/25	Mon 08/09/25
Presentation at TWEPP	Mon 29/09/25	Mon 28/09/26
Presentation at CHEP	Mon 06/10/25	Mon 05/10/26
Architecture Evaluation	Tue 13/05/25	Mon 02/02/26
Preliminary Architecture Proposal	Tue 03/02/26	Tue 03/02/26
Present at TIPP 2026	Mon 21/09/26	Mon 21/09/26
Architecture refinement	Wed 04/02/26	Mon 01/03/27
Refined Architecture Proposal	Mon 01/03/27	Mon 01/03/27
IP Survey & evaluation	**Mon 07/04/25**	**Tue 31/03/26**
Software IP survey	Mon 07/04/25	Fri 30/01/26
Software IP survey report	Mon 02/02/26	Mon 02/02/26
28nm IP survey	Tue 01/04/25	Fri 04/07/25
28nm IP survey report	Mon 07/07/25	Mon 07/07/25
28nm IP evaluation	Tue 08/07/25	Tue 31/03/26
Hardware IP development	**Tue 01/04/25**	**Fri 31/03/28**
Ethernet IP test structure design	Mon 07/07/25	Fri 24/07/26
Presentation at TWEPP	Mon 29/09/25	Mon 27/09/27
Ethernet IP test structure manufacture	Mon 27/07/26	Mon 26/10/26
Test system build	Mon 27/07/26	Mon 26/10/26
Ethernet IP test structure test	Tue 27/10/26	Mon 18/01/27
Ethernet IP test report	Tue 19/01/27	Tue 19/01/27
Ethernet IP radiation evaluation	Tue 19/01/27	Mon 19/04/27
Ethernet IP radiation evaluation report	Tue 20/04/27	Tue 20/04/27
2nd IP test structure design	Tue 19/01/27	Mon 26/07/27
2nd IP test structure manufacture	Tue 27/07/27	Mon 25/10/27
2nd IP test structure test	Tue 26/10/27	Mon 24/01/28
2nd IP test structure report	Tue 25/01/28	Tue 25/01/28
2nd IP test structure radiation eval	Tue 26/10/27	Fri 25/02/28
2nd IP radiation evaluation report	Mon 28/02/28	Mon 28/02/28
Evaluate an SoC approach	**Tue 01/04/25**	**Mon 14/02/28**
CERN SoC ecosystem installation	Tue 01/04/25	Mon 28/07/25
CERN SoC ecosystem installed	Tue 29/07/25	Tue 29/07/25
CERN SoC ecosystem training complete	Tue 29/07/25	Mon 20/10/25
Preliminary SoC ecosystem evaluation	Tue 21/10/25	Mon 02/03/26
SoC ecosystem sub-block design	Tue 03/03/26	Mon 01/03/27
SoC design	Tue 02/03/27	Mon 14/02/28
SoC Demonstrator	Tue 15/02/28	Tue 15/02/28



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