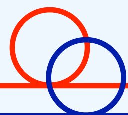
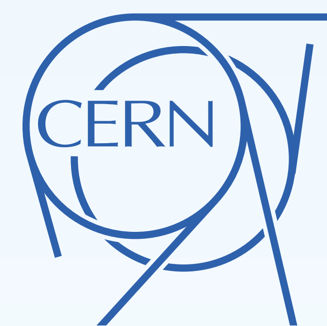
DRD7.1a
Silicon Photonics Transceiver Development





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on behalf of the project team

Reminder: ID Card

Project Name	Silicon Photonics Transceiver Development (WG7.1.a)
Project Description	Develop high-speed optical transceivers based on Silicon Photonics technology. Initial duration 3 years.
Innovative/Strategic Vision	First opportunity to design and operate custom optical data transmission systems in HEP detectors.
Performance Target	100 Gb/s per fibre optical readout with 2.5 Gb/s control optical link operating at a BER of 10^{-12}. Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy and power consumption of 250 mW. Cryogenic temperature operation for some lower-speed variants.
Multi-Disciplinary, cross-WG content	Silicon Photonics combines data-density, timing distribution, Back-end, as well as 2.5/3D integration, with the need for foundry access to specialist processes.
Contributors	CA: Sherbrooke CERN DE: DESY, KIT, Wuppertal ES: IGFAE UK: Birmingham, Imperial IT: INFN Milano, INFN Pisa, Sant'Anna, Uni. Trento US: Argonne, Fermilab

Work Topics and Areas of Contribution

- Silicon Photonic Integrated Circuit (PIC) design
    - Argonne, CERN, DESY, Fermilab, KIT, Pisa, Sant'Anna, Sherbrooke, Trento
- Silicon Photonics modulator driver design
    - CERN, DESY, Fermilab, KIT, Milano, Sherbrooke, Trento
- Silicon Photonics photodiode TIA design
    - CERN, DESY, Fermilab
- Silicon Photonics device environmental effects (Temperature, Radiation)
    - Argonne, Birmingham, CERN, DESY, Fermilab, IGFAE, Pisa, Sant'Anna, Sherbrooke, Trento
- Silicon Photonics packaging
    - CERN, DESY, Fermilab, KIT, Sherbrooke
- Silicon Photonics system integration and testing
    - Argonne, Birmingham, CERN, DESY, Fermilab, IGFAE, Imperial, KIT, Trento, Wuppertal

Proposed Milestones and Deliverables

- D7.1a.1 (M12) WDM test PIC:
  - a PIC that demonstrates the use of 4-channel Wavelength Division Multiplexing (WDM) to transmit multiple Gb/s datastreams onto one optical fibre.
- M7.1a.1 (M12) Cryogenic test of SiPh PIC:
  - testing of a PIC will be carried out at cryogenic temperatures to establish feasibility and/or determine areas of future work.
- M7.1a.2 (M12) Submission of Ring Modulator Driver:
  - the design of a Ring Modulator driver will be submitted for fabrication.
- M7.1a.3 (M24) Radiation test of WDM PIC:
  - radiation testing (at multiple sources) will be carried out to show the feasibility of the various WDM components and system to operate in radiation environments.
- D7.1a.2 (M24) Packaged WDM PIC:
  - a PIC will have optical fibres attached to it with minimal loss, ready for integration into larger systems.
- M7.1a.4 (M30) Submission of photodiode TIA:
  - the design of a TIA for use with SiPh photodiodes will be submitted for fabrication.
- M7.1a.5 (M36) System test of WDM PIC with Driver:
  - a high-level system test of a WDM PIC integrated with a driver ASIC will be carried out.

PIC *Photonic Integrated Circuit*
SiPh *Silicon Photonics*
TIA *TransImpedance Amplifier*
WDM *Wavelength Division Multiplexing*

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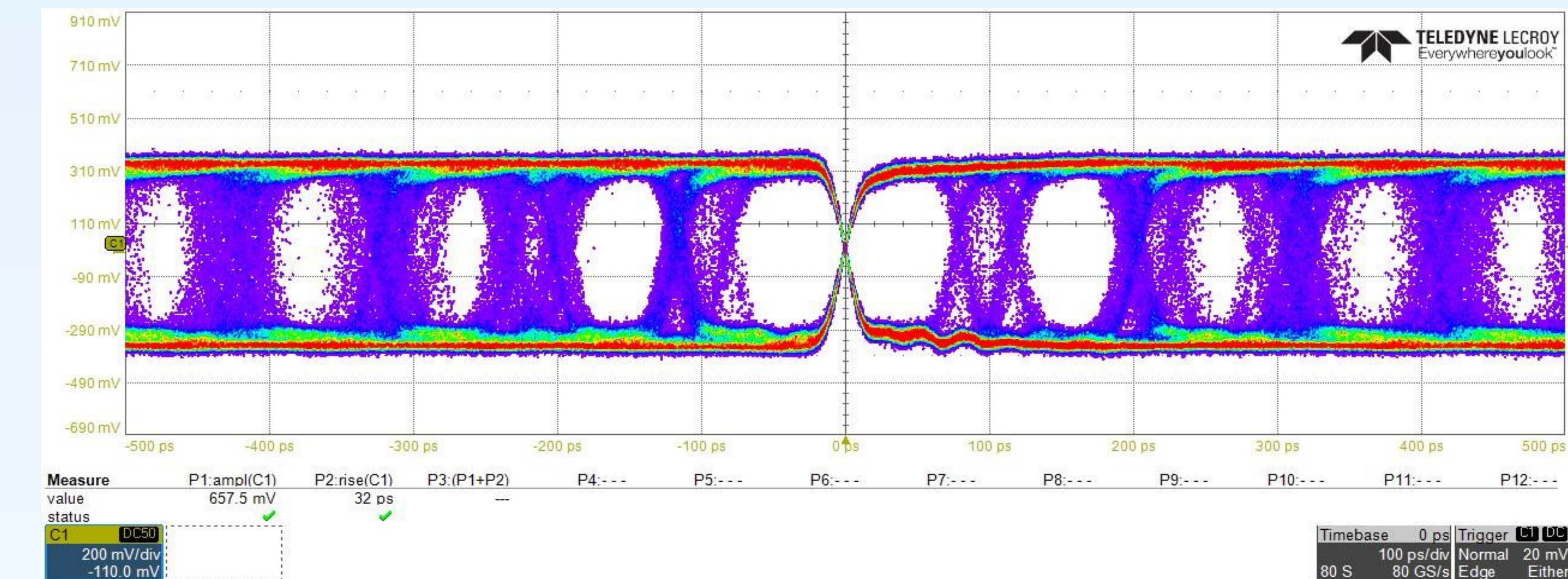
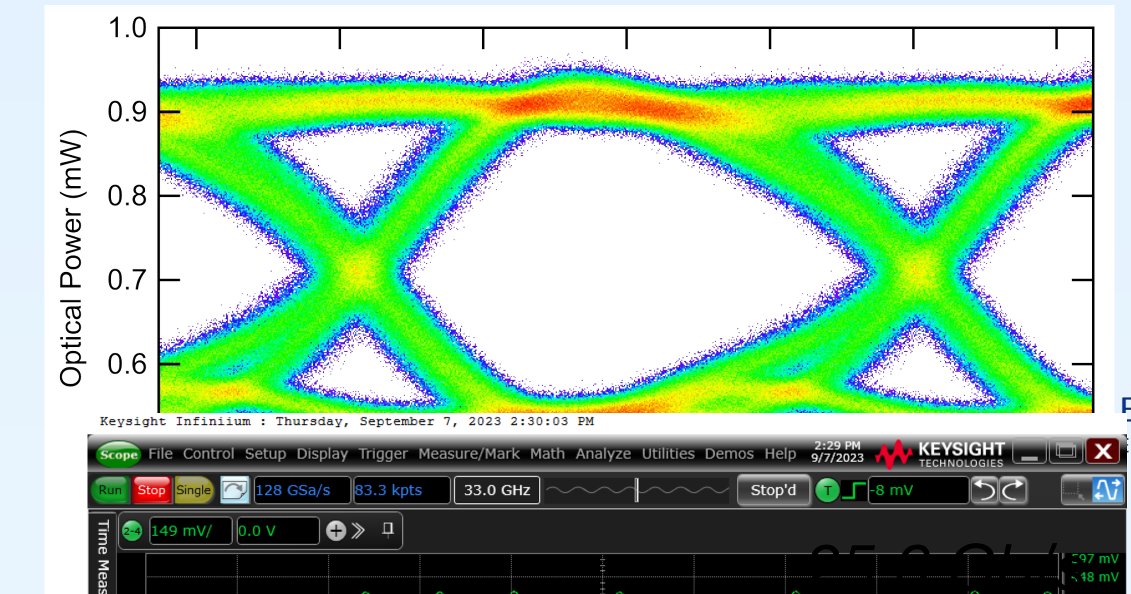
Institute Status: Birmingham

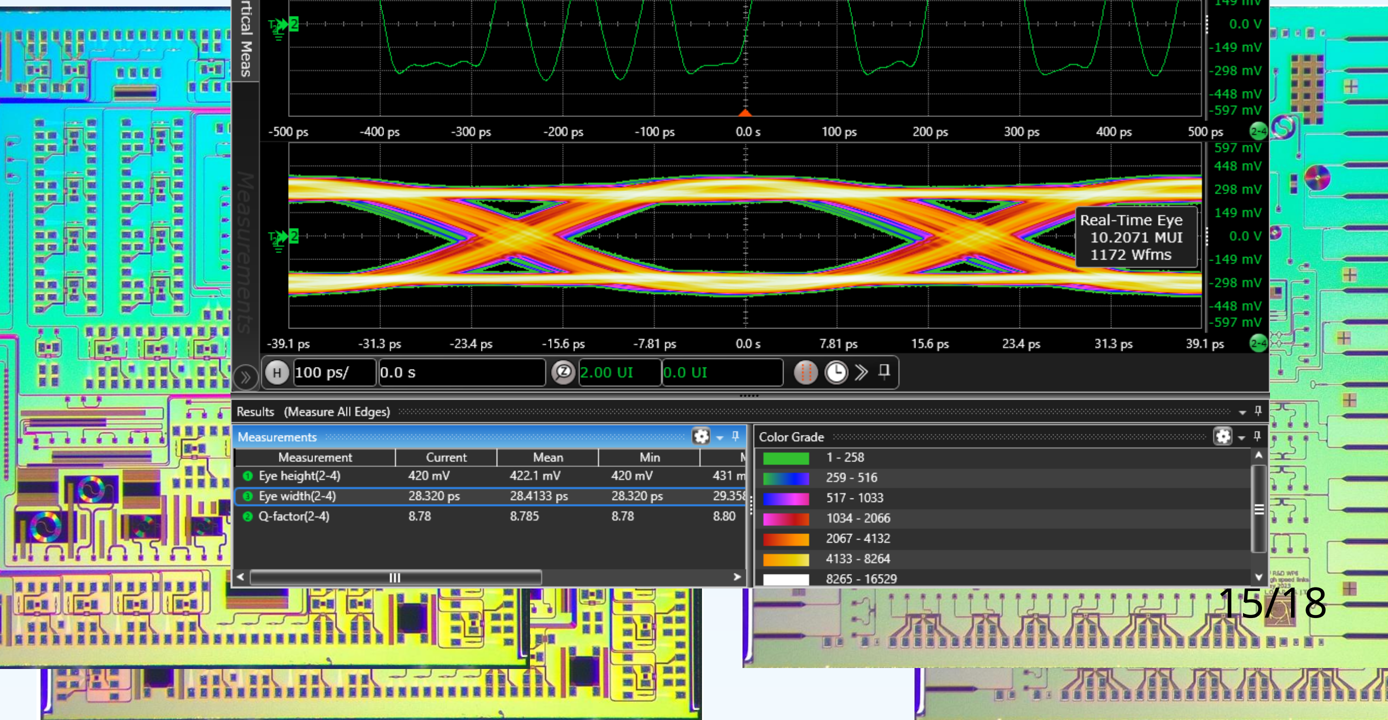
- Participation: Environmental effects; System integration & testing
- Currently commissioning testbench
  - High speed FPGA signal generator, optical interconnects,
  - transceiver, power meter, fast scope
  - Adapting f/w for VPK120
  - To integrate System PIC+DART28 from CERN
- Planning proton irradiation (local 27 MeV cyclotron)
  - Extends neutron and x-ray campaigns by CERN, few ×1015 ~ hours
  - Before/after characterisation routine; readout during irradiation possible
- Environmental testing (vacuum and temperature)
- To investigate MSA QSFP light source
- Exploit synergy with specific use-case: LHCb Upgrade II
  - Makes resources available! recruiting engineer and technician

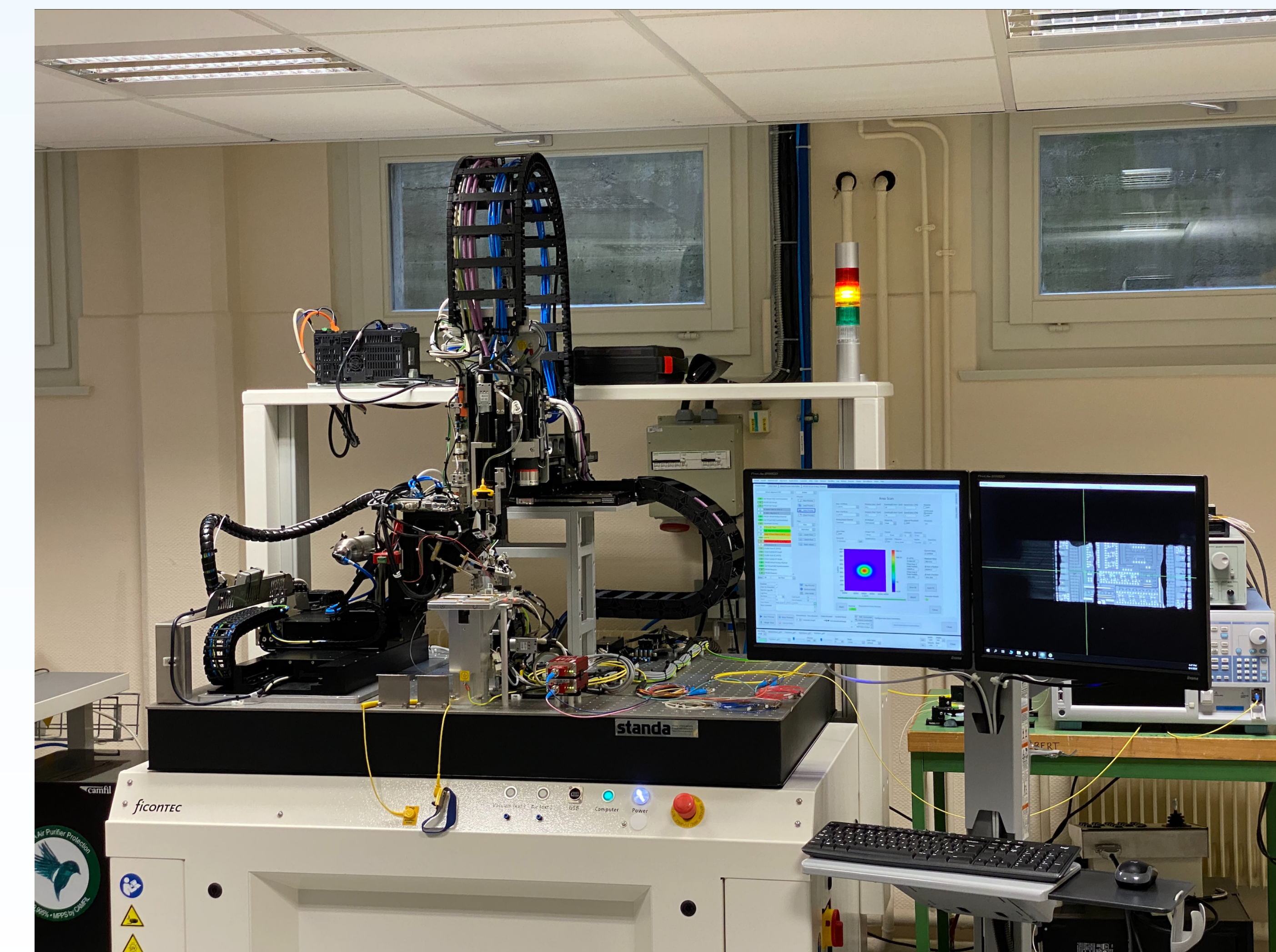


Institute Status: CERN

- Participation: PIC, modulator driver, and TIA design; Environmental effects; Packaging; System integration & testing
- After successful design of first 25G class driver, working on higher voltage RM driver for improved system margin
- Currently evaluating performance of recently received PICs
  - WDM structures with 4 RMs on bus waveguide
  - Polarisation management structures
  - various waveguide and fibre-coupling structures
- Carried out neutron irradiation in June, planning x-ray irradiation in September
  - Provides data for building device simulation models
- Received fibre-alignment machine, working on routines to attach fibre array blocks to PICs, inc. active alignment
- Provided pigtailed PIC to IGFAE as first sample for vacuum & temperature testing

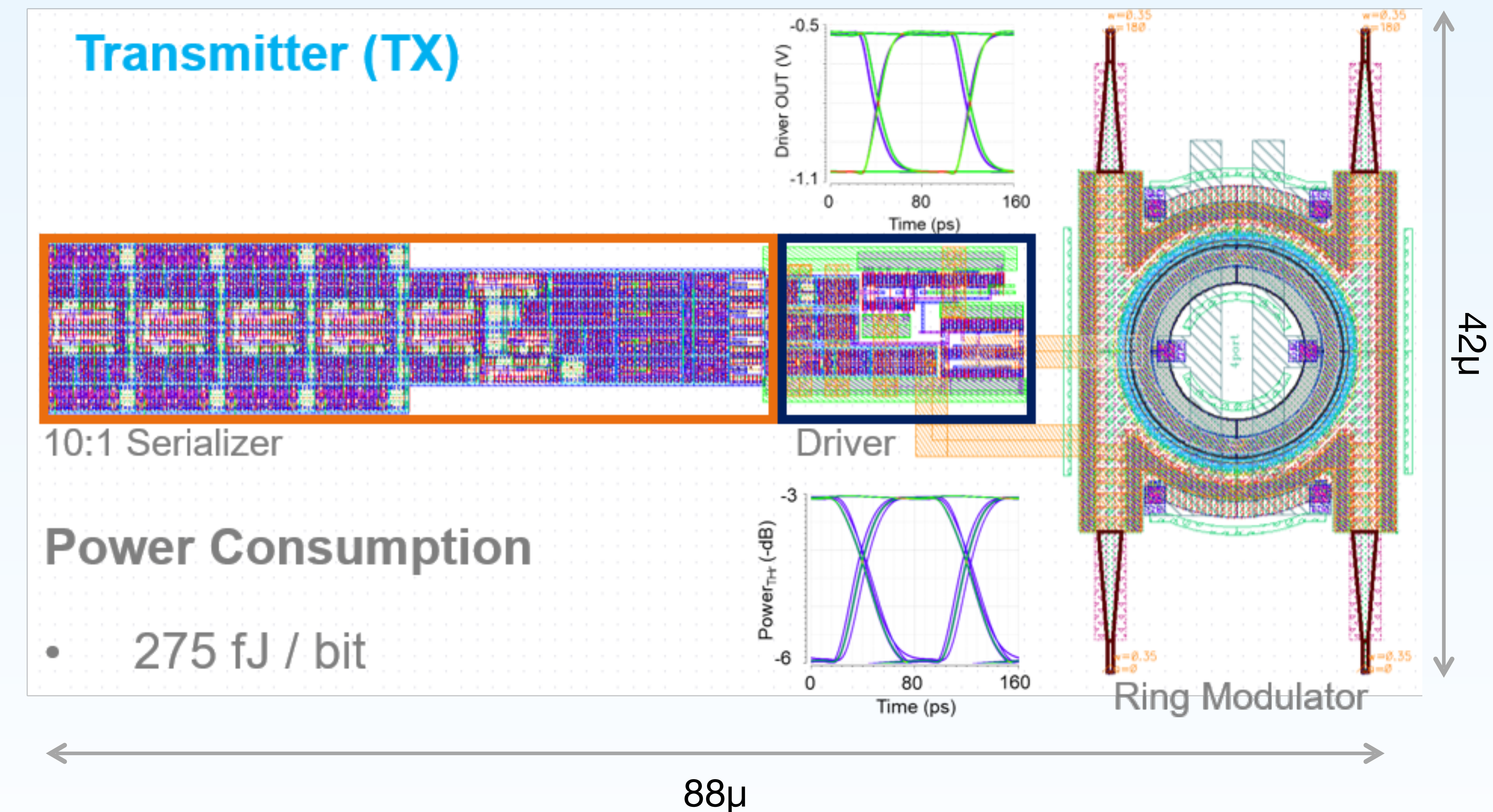






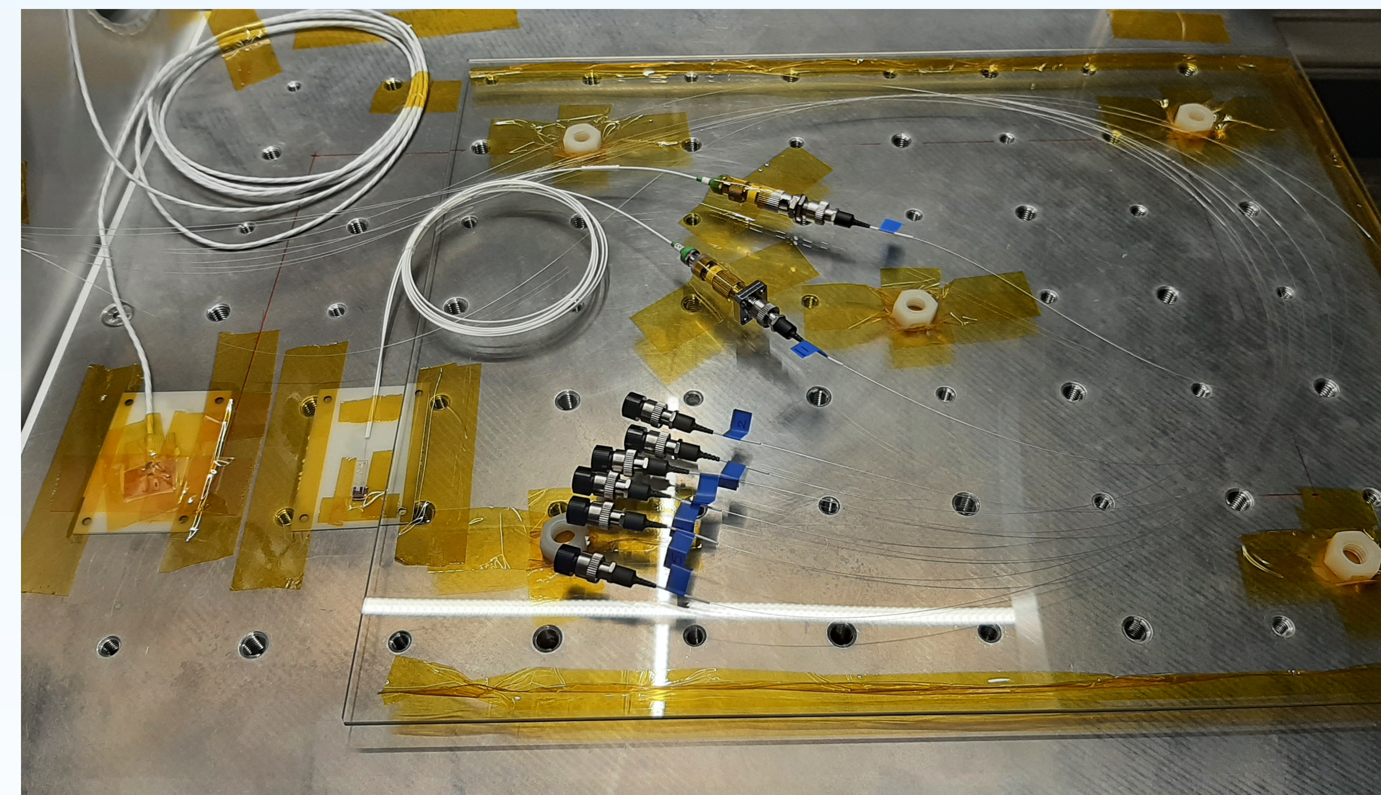
Institute Status: DESY

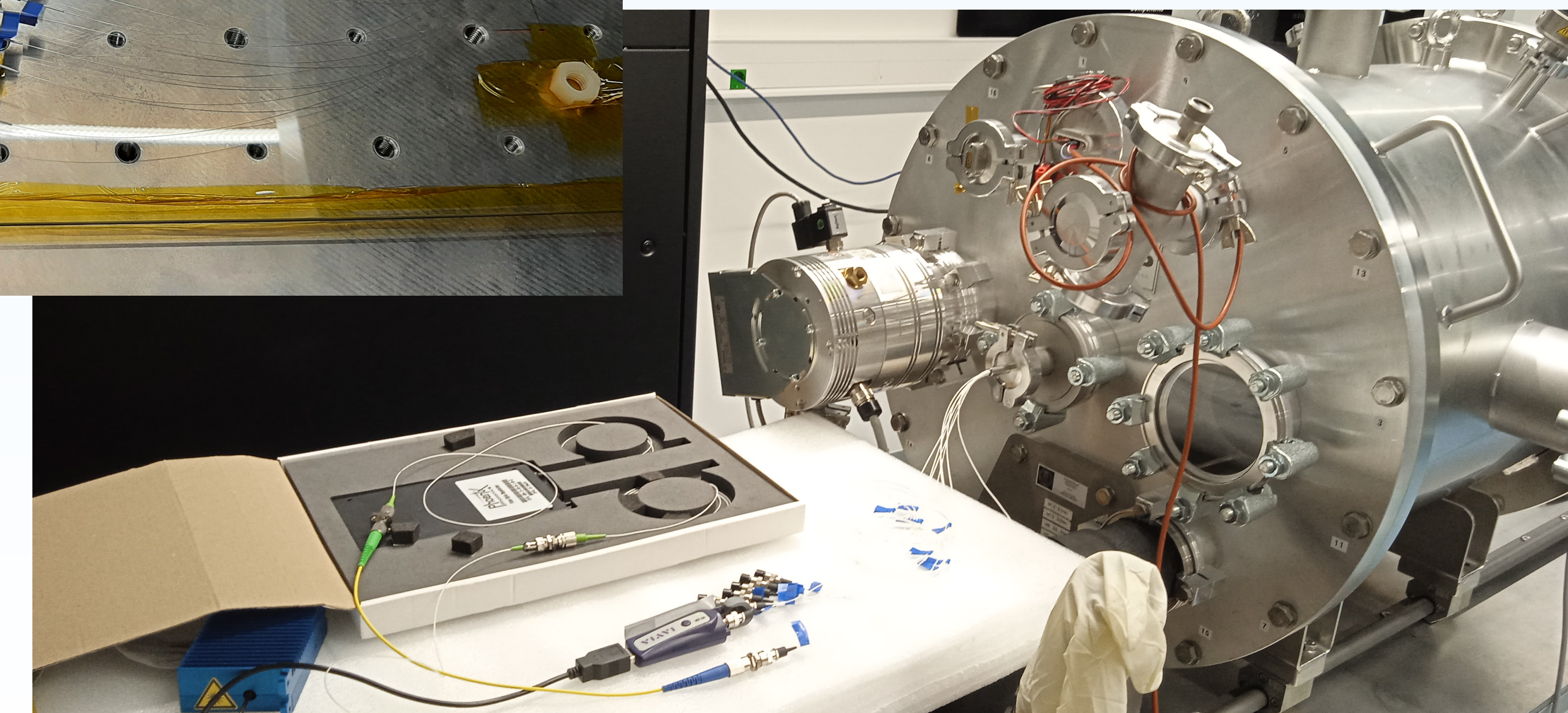
- Participation: Monolithic EPIC with GlobalFoundries Fotonix TM
- Target: Application fields of timing, tracking and imaging detectors
- Current design activities
  - Photonics
    - Multiplexing scheme: Dense WDM (4-channel)
    - Ring modulator / resonator based transceiver
    - Passive edge coupling
  - Electronics:
    - Transmitter (TX) → 8b/10b encoder, serializer, driver
    - Receiver (RX) → TIA, deserializer, CDR, 8b/10b decoder
- Additional funding approval → pending



Institute Status: IGFAE

- Participation: Environmental effects; System integration & Testing
- Personnel involved: 1 Professor, 1 PhD Engineer, 2 technicians
- Resources: vacuum setup (currently down to 10^{-6} mbar, planning an upgrade to 10^{-9} mbar), microelectronics and SMD laboratories, clean room
- Currently: Testing optical power loss of 2 pigtailed PIC assemblies in vacuum (1 bar down to 10^{-6} mbar) and temperature (20ºC down to -70ºC)
- Next steps:
  - Repeat Vacuum + Cold testing:
    - After irradiation (X-ray)
    - (PIC+DART) Data transmission test

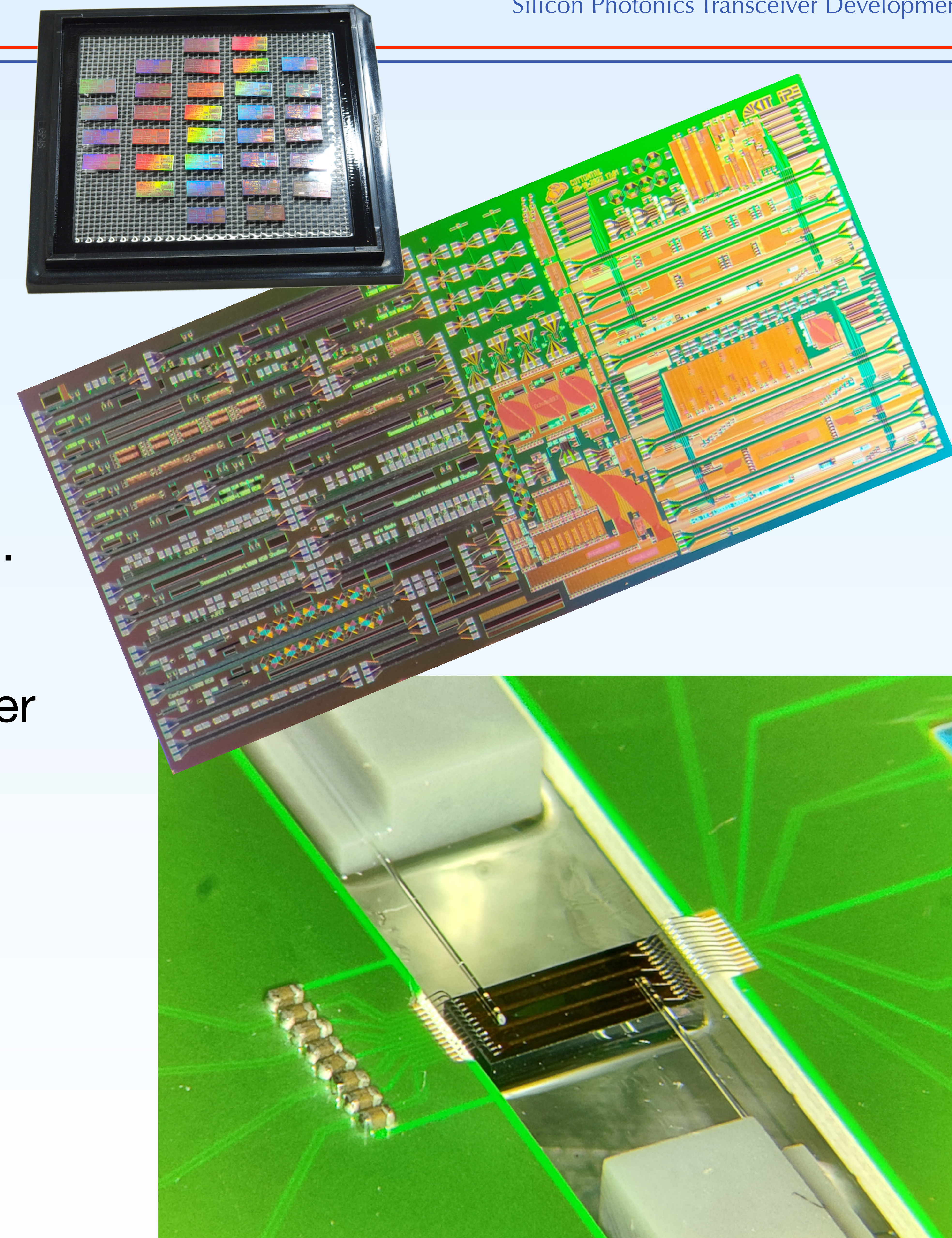




Institute Status: KIT

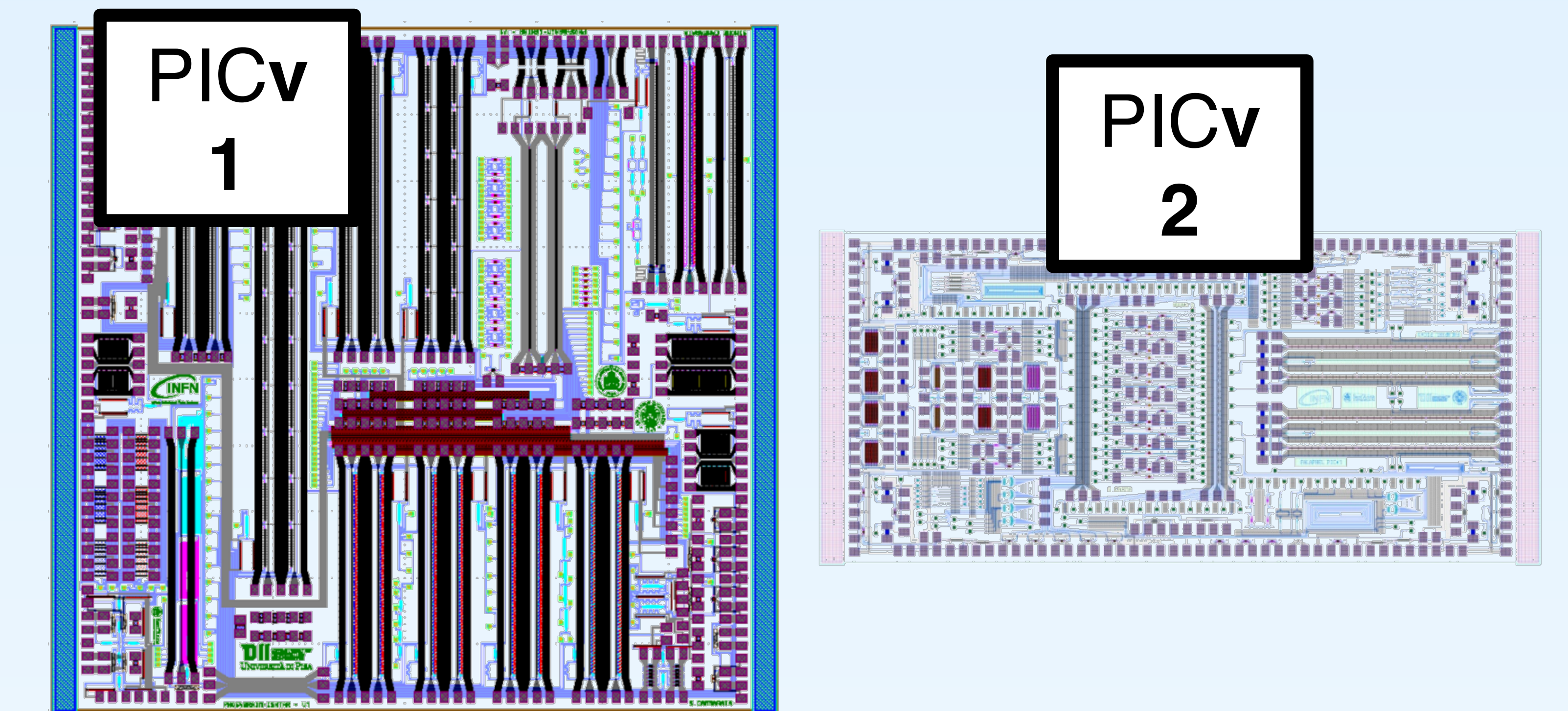
- Participation: PIC and modulator driver design; Packaging; System integration & testing
- Currently evaluating performance of recent PIC
  - 4-channel WDM with MZMs and thermal phase shifters
  - 4-channel WDM with RMs (but without monitor diodes)
  - Several single modulators, optical (de-)mux, photodiodes, …
- Fiber-chip-coupling development ongoing
  - Currently evaluating 3D-printing process for quartz glass fiber mounts
- Funding accepted for new RM chip and driver ASIC development (BMBF Verbundprojekt 05H2024)
- Packaging activities linked to DRD7.6.b

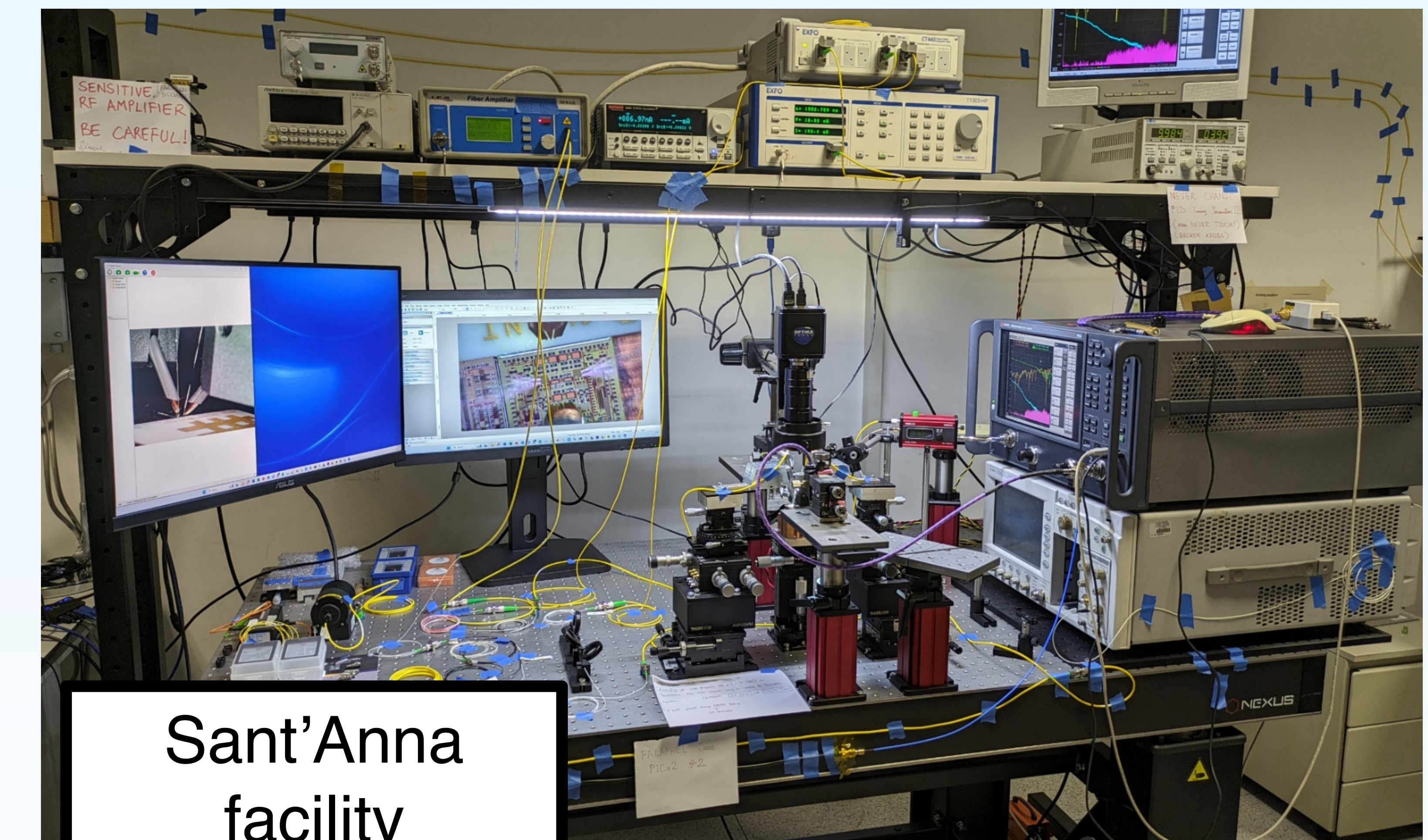
  (presentation tomorrow by Michele Caselle)

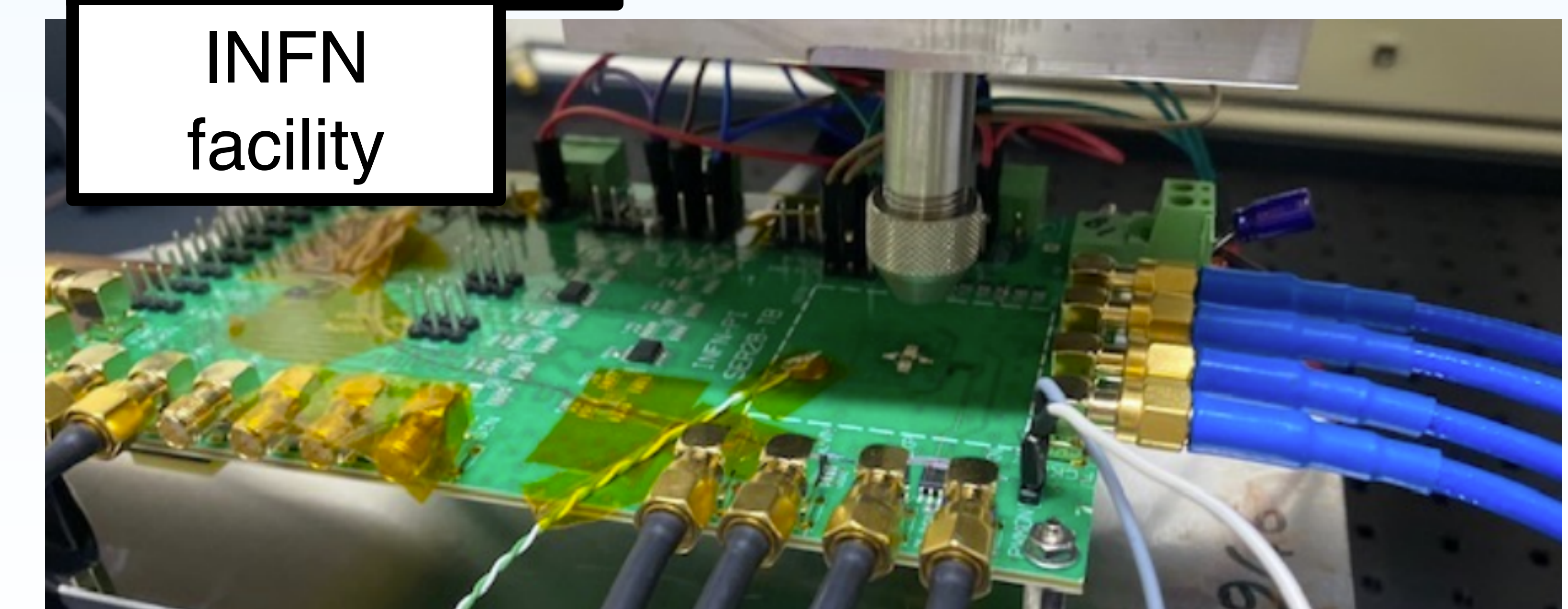


Institute Status: Sant'Anna + INFN Pisa

- Participation: PIC, Environmental effects
- PICs designed for radiation-tolerance and system-level performance evaluation of modulators and C-band transmitters
  - Custom traveling-wave and lumped-element MZMs, RMs and SiGe EAM building blocks (PICv1)
  - Custom RMs and 2-WDM RM-based transmitters (PICv2)
  - 4-WDM transmitter prototypes to be included in PICv3
  - Die-level manual probe station for electro-optical and high-speed measurements available at Sant'Anna
- X-rays irradiation measurements
  - MZMs, RMs and SiGe EAMs exposed to > 12 MGy(SiO_2) TID for radiation-hardness investigation
  - X-rays irradiator available at INFN Pisa





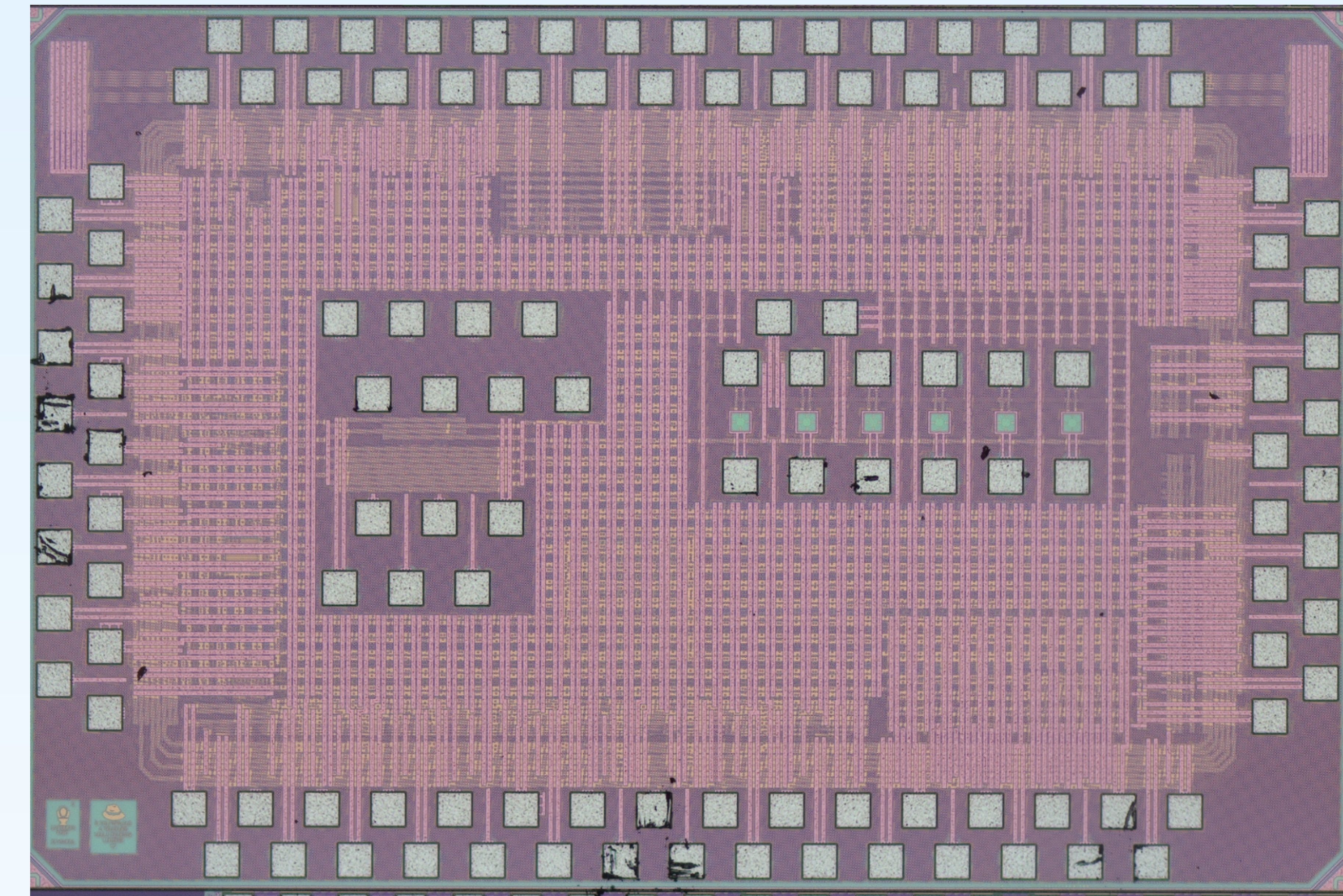


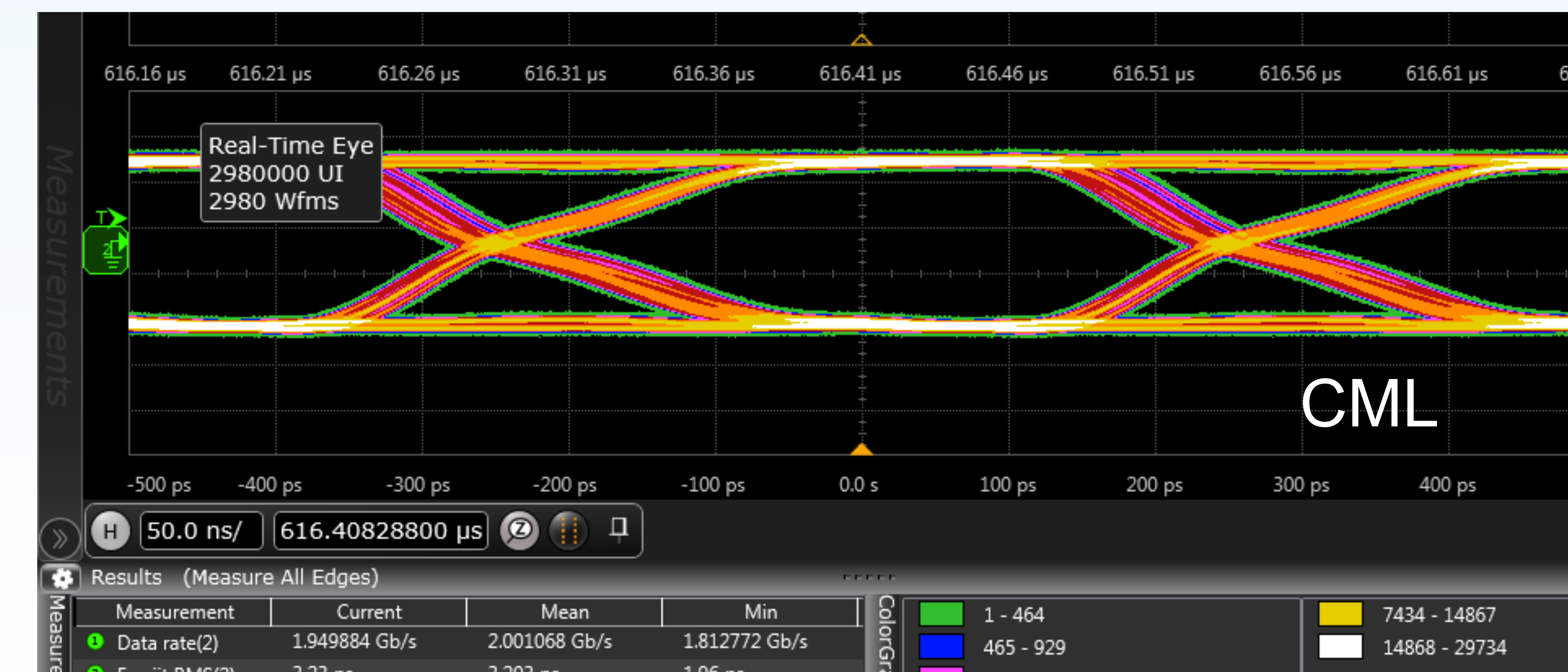
Institute Status: Sherbrooke

- Participation: PIC and modulator driver design; Low Temperature effects; Packaging
- PIC: 2 designs tested
  - Photosensitivity @ 110 K for 1550 nm problematic, need to move to 1310 nm for cryogenic applications.
  - Validated cryogenic operation for photonic wirebonds.
- CMOS low power driver (under characterisation)
  - TIA: circuit functionnal at room temp up to 800 Mbps
  - Driver: inverter-based driver functional up to 1 Gbps
  - CML serialisation working with FPGA for DAQ, up to 2 Gbps
- Article on overall architecture, under review, JINST

  (TechRxiv [10.36227/techrxiv.172565555.56657721/v1](https://doi.org/10.36227/techrxiv.172565555.56657721/v1))
- Project Status:
  - Closing project after CMOS Driver characterisation + publication.
  - Available/interested to participate in design reviews.

CMOS Driver





Next Steps

- Quite some progress has already been made towards our initially defined goals
- Preparing project discussion for early October to refine plans based on participating institutes' current resource levels
  - This will result in an updated overall project plan with refined milestones and deliverables