

DRD7.1b

Powering Next Generation Detector Systems

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F. Arteché, ItA, Spain

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DRD 7.1.b Powering Next Generation Detector Systems

Next-generation, large-area, high-granularity particle detectors consume significantly more power at reduced voltages compared to current systems.

This project aims to improve power efficiency of detector systems at reduced material budget.

For this purpose, two powering options will be investigated:

The project is a joint effort of experts in power electronics, IC and PCB design, thermal management, EMC, reliability and particle detector systems.

This presentation will focus on the development that has been realised in 2024, because the project had already some momentum with internal funds of each institute.

Parallel Powering (DCDC)

Contribution from:

- CERN
- FH Dortmund
- RWTH Aachen
- TU Graz
- UNIUD
- UNIMI+INFN

Serial Powering

Contribution from:

- FH Dortmund
- ITA
- UNIMI+INFN

DRD7.1.b Available and requested funds

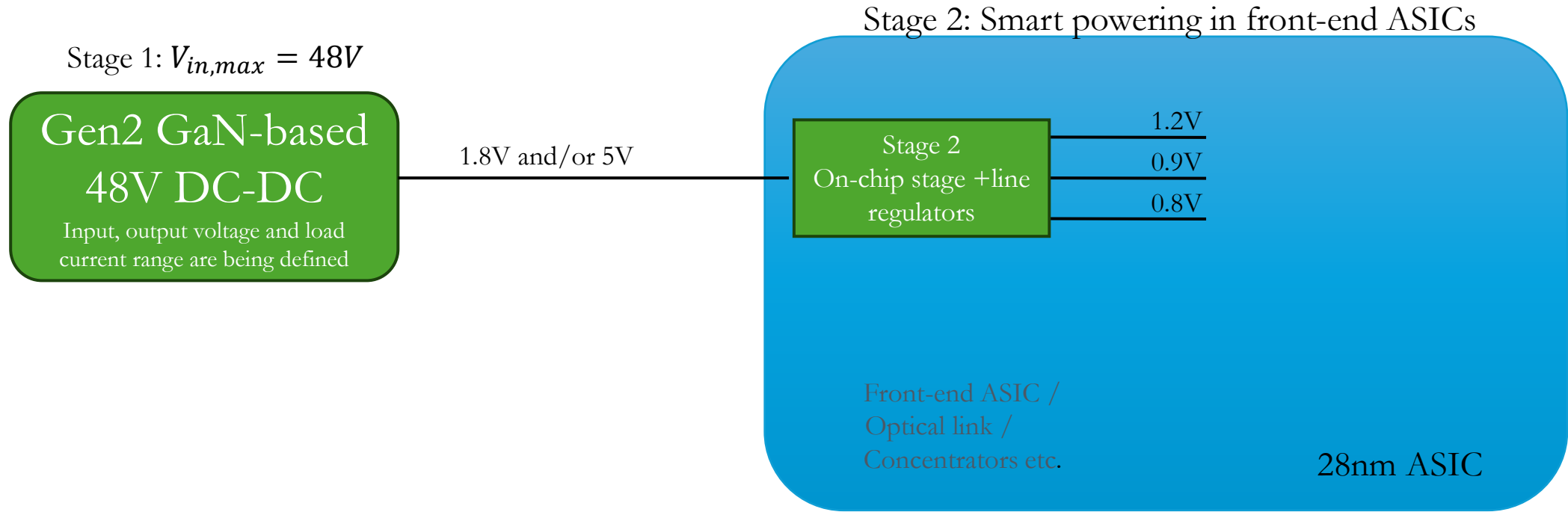
	Granted Funds		Requested funds	
Institute	FTE / Monetary funds	Funds granted by	FTE / Monetary funds	note
CERN	2.5 / 270kCHF (over 5 years)	Granted by CERN EP-RD WP2 and EP-RD WP5.4		
FH Dortmund	1.33 / 110 kCHF (over 3 years)	BMBF as part of two projects (05H21PRCA9 & 05H21PRRD1)	1	Submitted to transnational funding agencies.
ITA	2.0 /200 kCHF (over 5 years)	GanCAP4CMS, PC Fisica-MMR ,AIDAinnova & CMSUPG2	1 / 50 kCHF	ELECTRAF project submitted to Aragon Government, Spain, on March 2024.
RWTH Aachen	0.7 / 45KCHF 0.4 / 0	From BMBF 05H24PA2 From internal funds		
TU Graz	0.33		1 / 50 kCHF	Submitted the Austrian Science Fund FWF
UNIUD	0.7		1	Request will be done to INFN if DRD approved
INFN and UNIMI	0.5		0.5	Request will be done to INFN if DRD approved
Taltech	0.3 / 40kCHF (in total 2023-2024)	Estonian Research Council (RVTT3)	0.8 / 350kCHF (in total over 5 years)	Application will be submitted in February 2025 (MOU needed)

Parallel Powering (DCDC)

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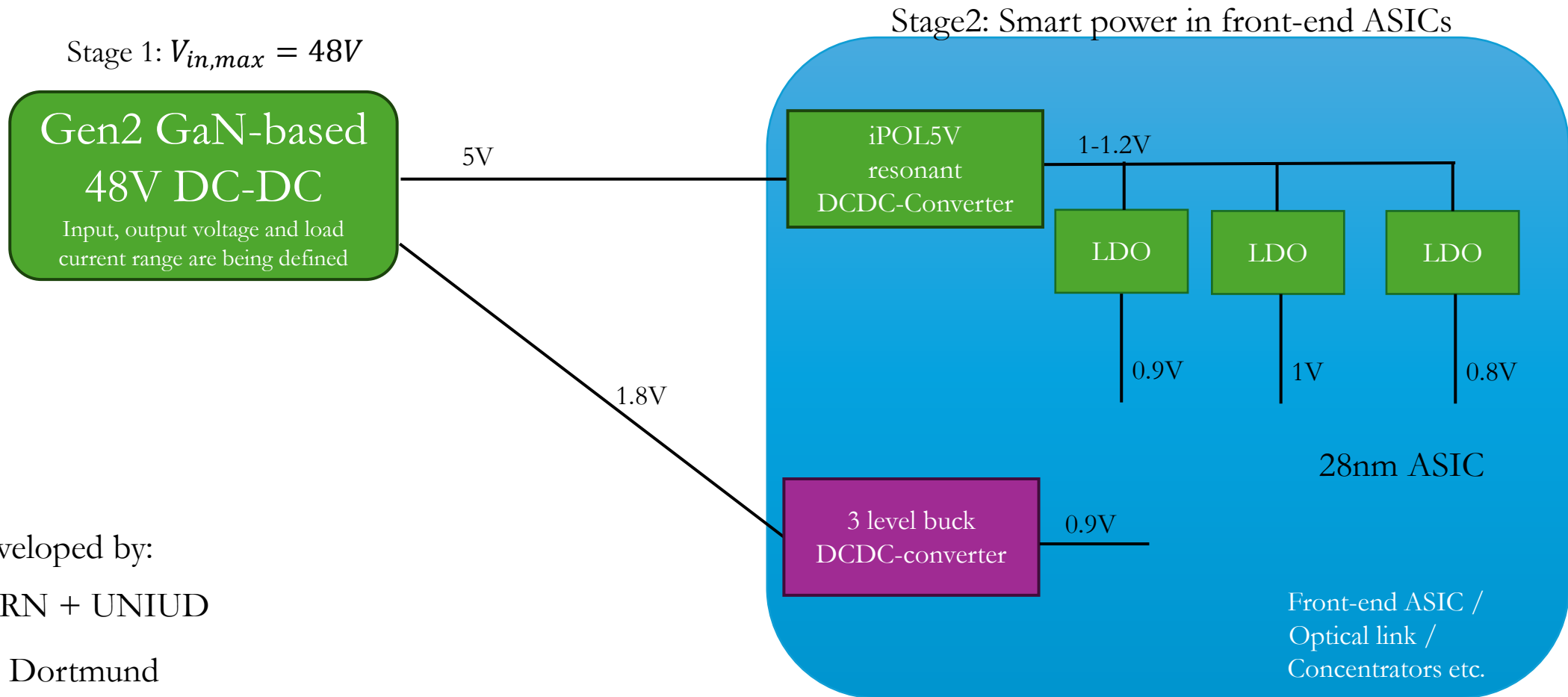
WP 7.1b: parallel power (DCDC)



Stage 1 based on HV CMOS technology and GaN power stage

Stage 2 is a fully integrated solution with all components inside the 28nm ASIC

WP 7.1b: parallel power (DCDC)



Developed by:



CERN + UNIUD



FH Dortmund

48V DCDC module converter development

Using available stock of bPOL48V (~70K dies)

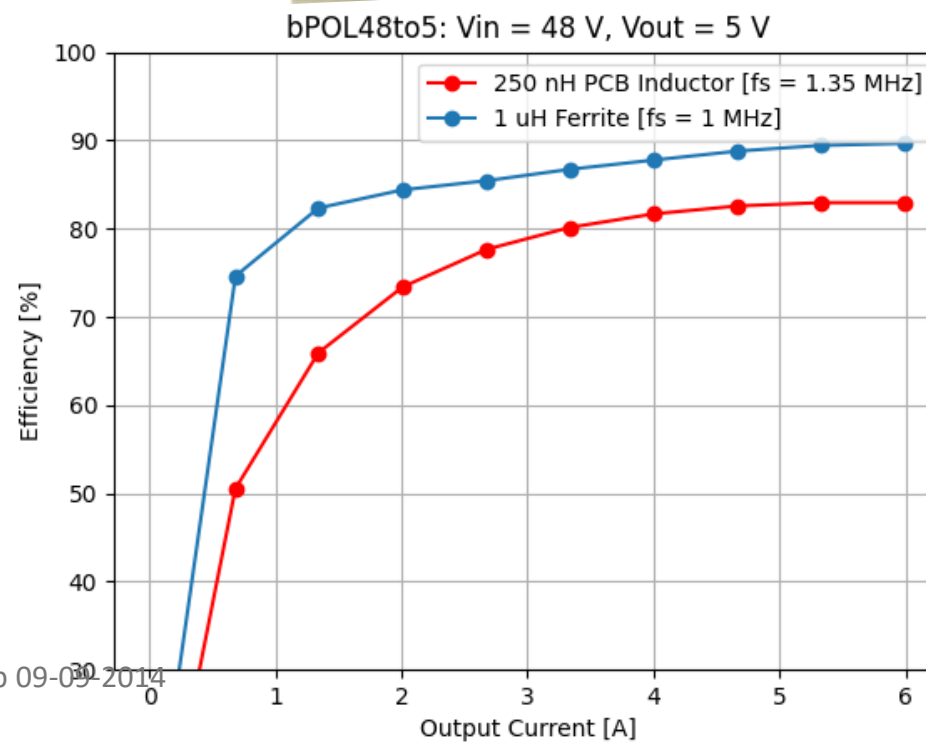
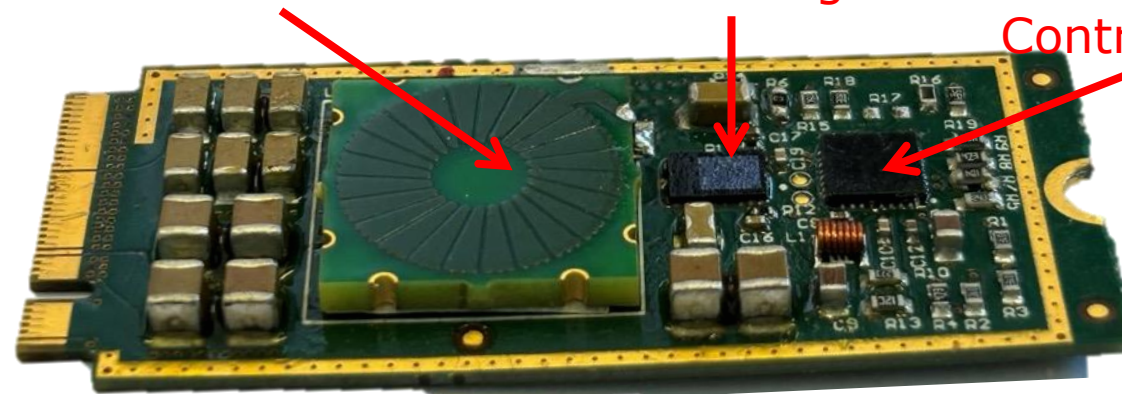
Volume optimized bPOL48 modules:

- bPOL48to12 (EPC2152): 48V to 12V with 6A out
- Dimensions: 24 x 55 x 4 mm

PCB Inductor:

- Inductance: 100-400 nH
- Size: 15 x 15 x 3 mm
- Similar performance to wire wound air-core inductors

PCB Inductor (Copper Filled Vias) GaN Commercial Power Stage CERN Rad-Hard Controller

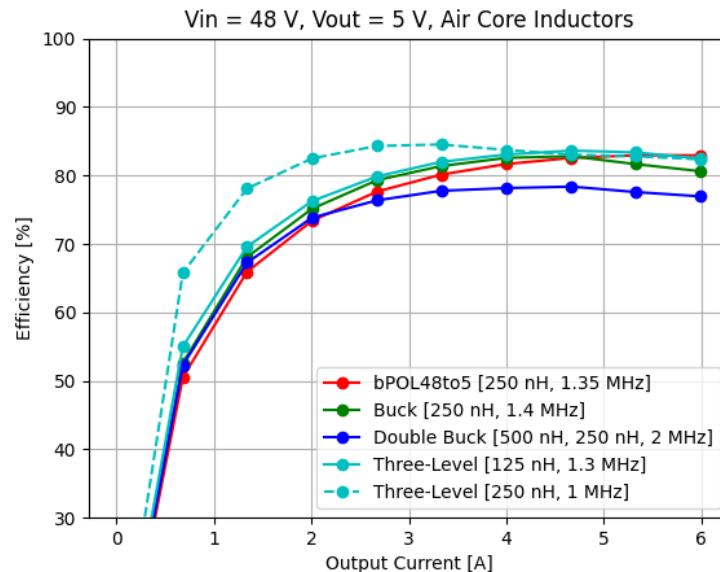


Stage1: 48V new converter R&D

Converter topology

- Optimization algorithms in Python
- Different prototypes with microcontroller

Promising topologies: Buck, 3 and 5 -Level Buck, (Berkeley) Series Capacitor Buck



ASIC design

- New CMOS High Voltage (HV) technology selected
- Design of the new controller started
- We have already all linear regulators designed and a big portion of the control circuit
- A second High voltage technology will be tested in 2025 (testchip currently in design phase)

Stage2: smart power and 28nm On-chip regulation

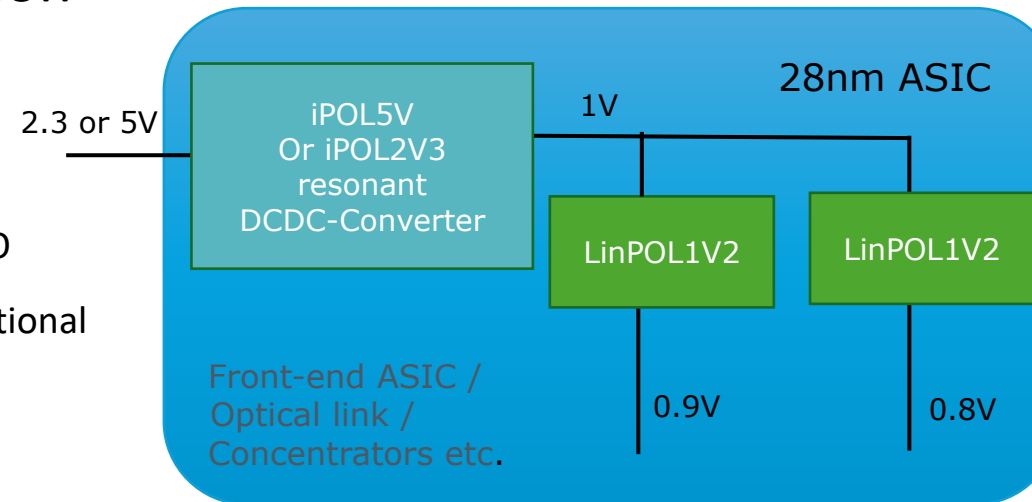
Smart distribution on chip is necessary to limit the power requirements.

A fully integrated DCDC will provide a ~1V on chip from 2.3V or 5V power bus.

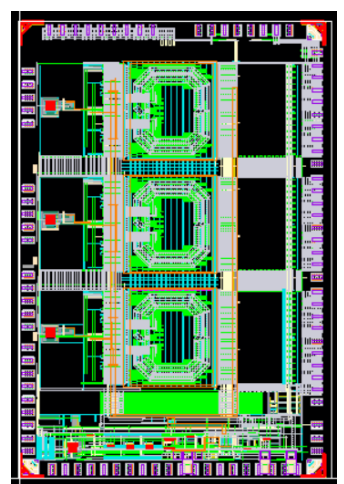
Different part of the circuit can be supplied with different voltages with full integrated LDO

This innovative power distribution scheme (developed with UNIUD) does not require additional external components: input-output capacitors and inductors are fully integrated

3 ASICS have been submitted in Nov2023 and today under testing



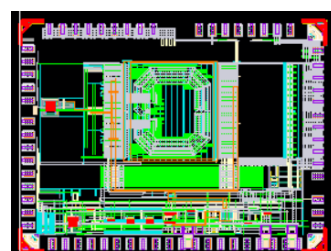
iPOL5V
Resonant
5V to 0.9V-1V



3179.34 um

2139.3 um

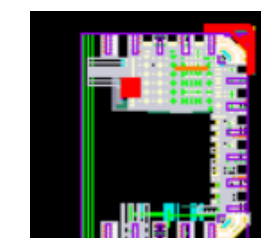
iPOL2V3
Resonant
2.3V to 0.9V-1V



1604.7 um

2139.3 um

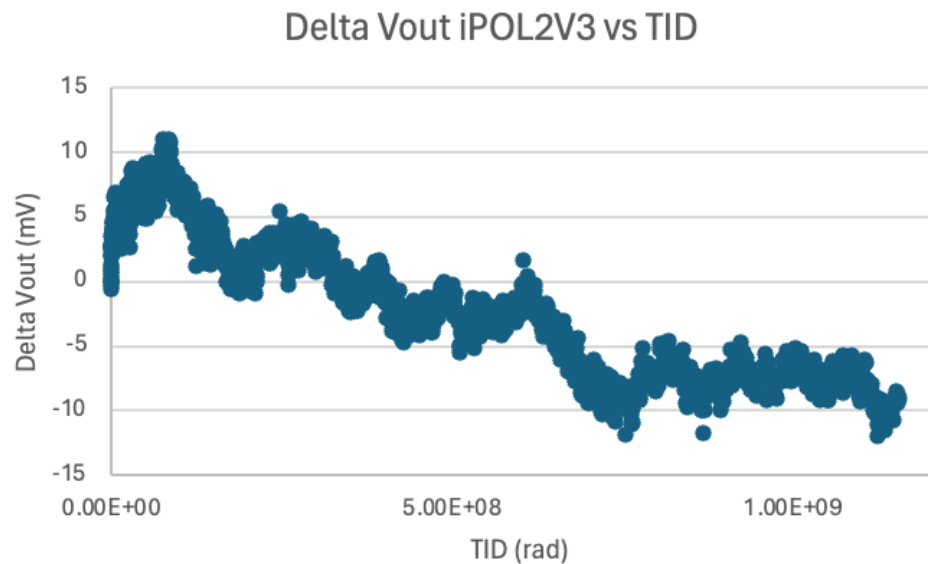
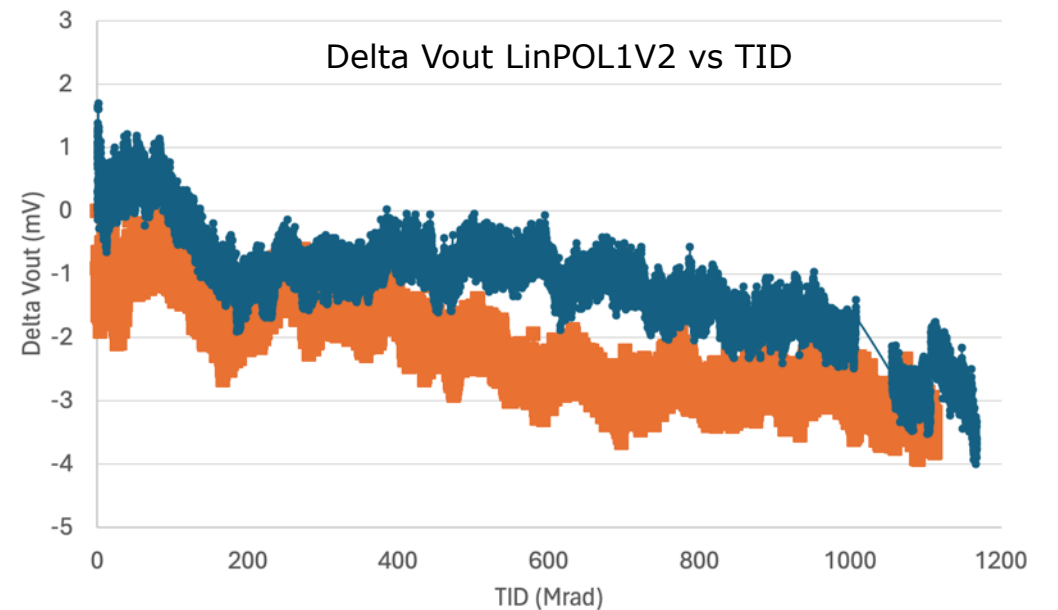
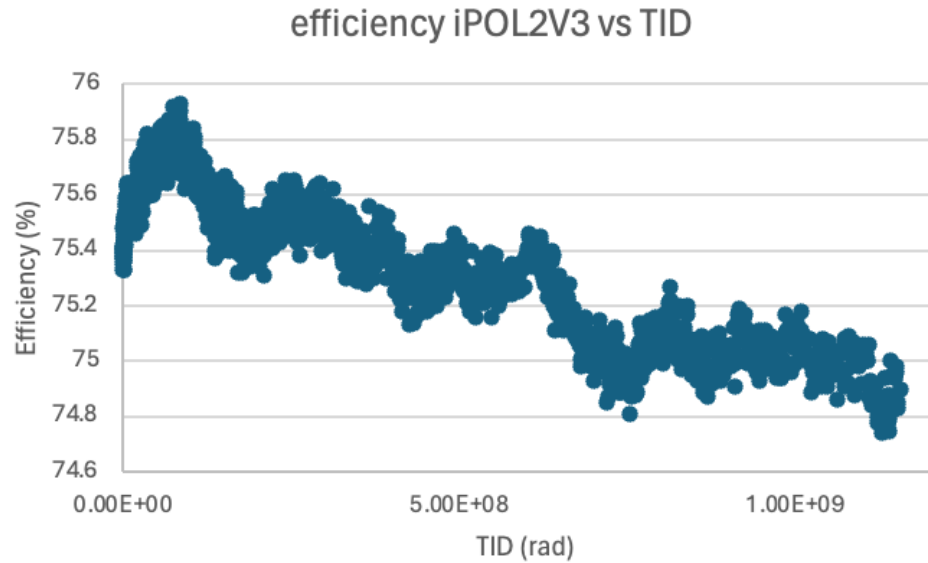
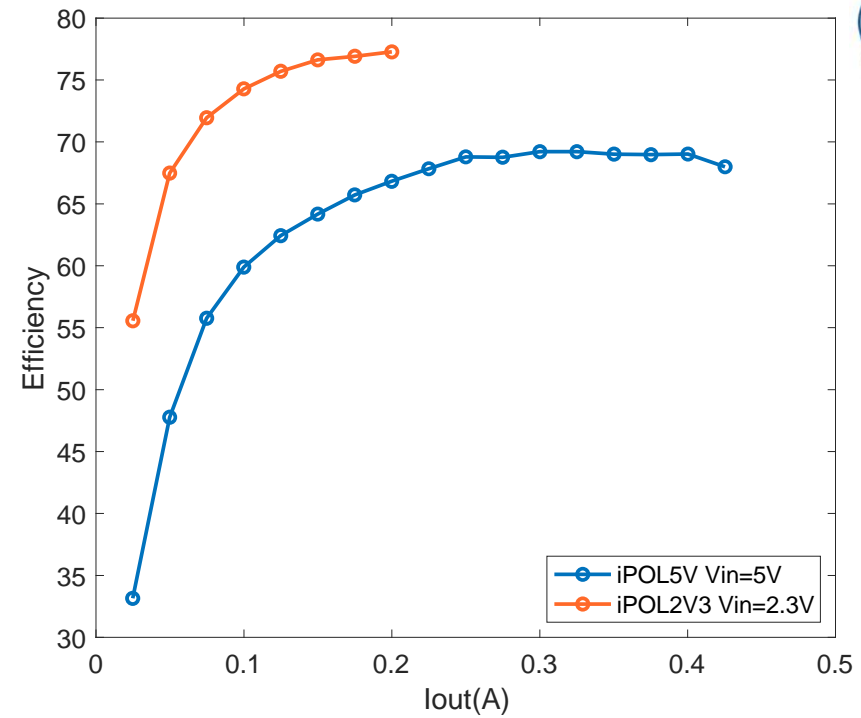
linPOL1V2
Linear regulator
1V to 0.8V-0.9



900 um

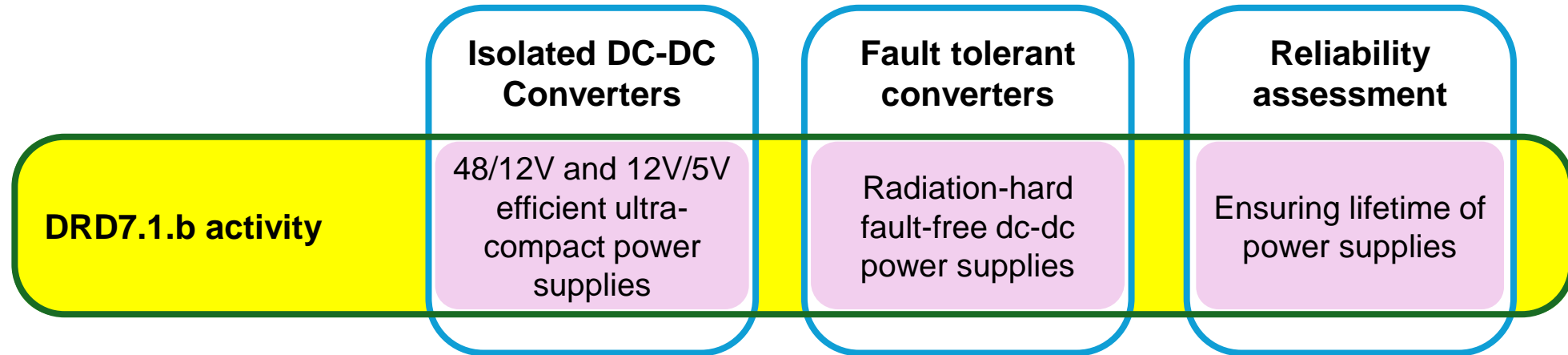
900 um

Stage 2 ASICs results



TOPICS COVERED BY TALTECH IN DRD 7.1.B

Fields of expertise of TalTech Power Electronics Group



LATEST RESULTS

- *Collaboration seminar organized on-site in CERN in December 2023*
- *A Ph.D student will be hired in 2024, position was opened recently (internal funding at first)*
- *Topic supported by national funding from Ministry of Education and Research of Estonia for 2024 (~0.3 FTE for this particular topic)*

TALTECH CONTRIBUTION TO DRD 7.1.B



NEXT STEPS

- *Organization of annual joint seminars in CERN including newly hired PhD student*
- *Apply for funding continuation with extended commitment also covering PhD student involvement starting from 2025 (funding increase from 0.3 FTE to 0.8 FTE) – **NEED OF MoU signed***

TARGETS

- *Synthesize and benchmark promising solutions (2024-2025)*
- *Develop a new low-cost and resilient point-of-load converter in (2025)*
- *Test new technology in selected rad. hard test facilities to verify the technology (2026)*
- *Reliability modeling and lifetime assessment of the technology (2027)*
- *Publish 1-2 common research paper per year*
- *One Ph.D student defended in 2028*

RWTH Aachen contribution updates

A new PhD position has been granted (new student selected, Joelle Savelberg),
2/3rd on DRD7.1.b + 45KEur granted + 10% of senior FTE

A test setup has been designed and realised for testing the bPOL48V. Extensive tests will start in Q4 2024



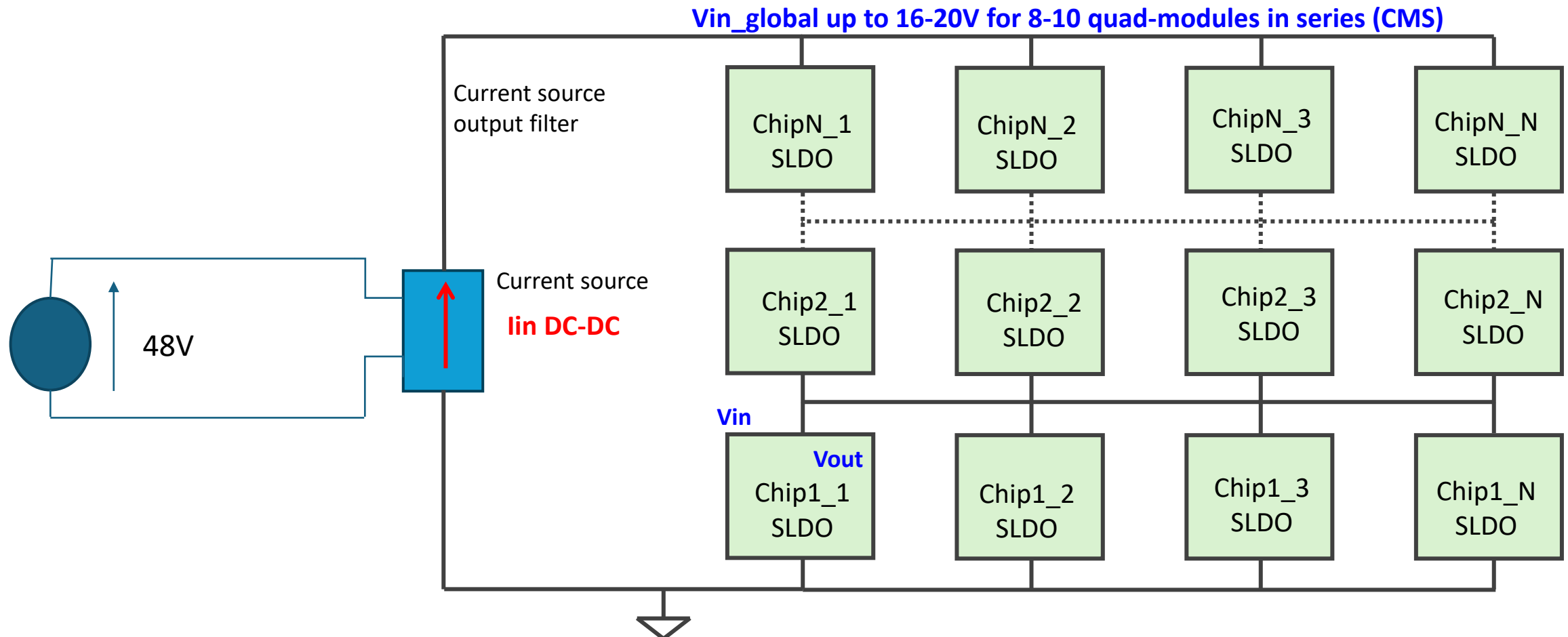
DRD7.1.b Powering, DRD7 workshop 09-09-2014

Serial Powering

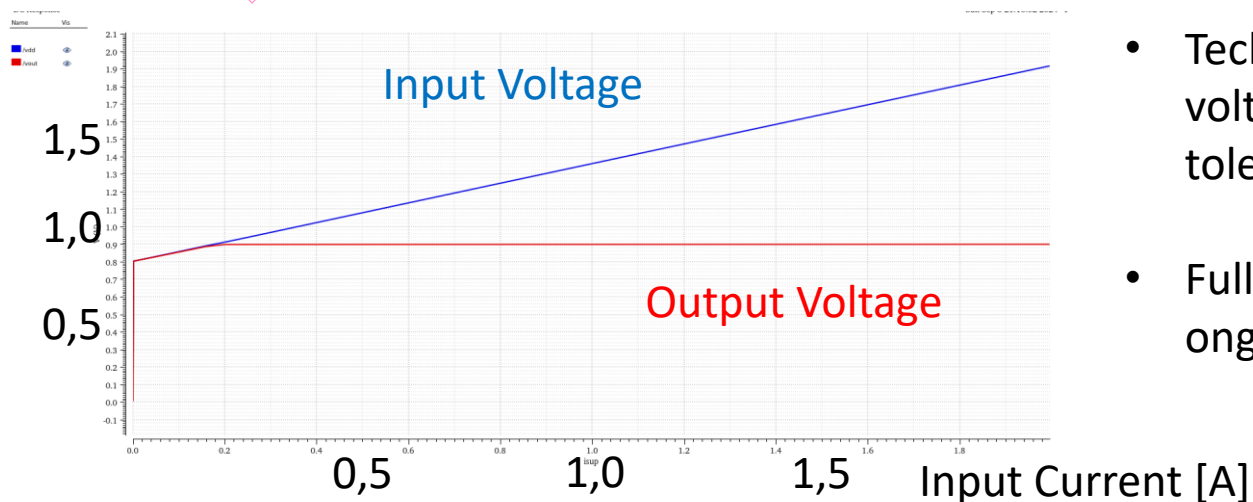
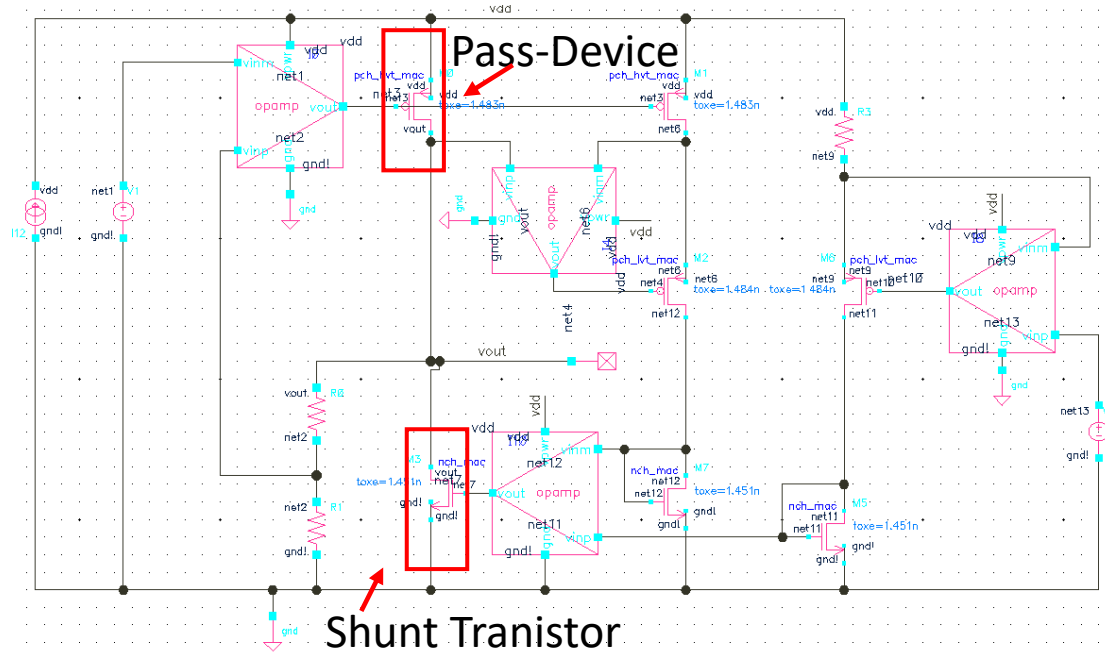
Contribution from:

- FH Dortmund
- ITA
- UNIMI+INFN

WP 7.1b: serial power



Shunt-LDO Design in 28nm



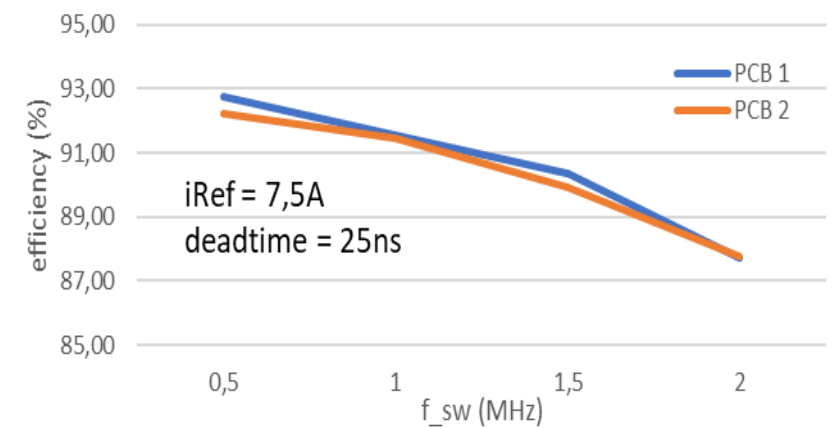
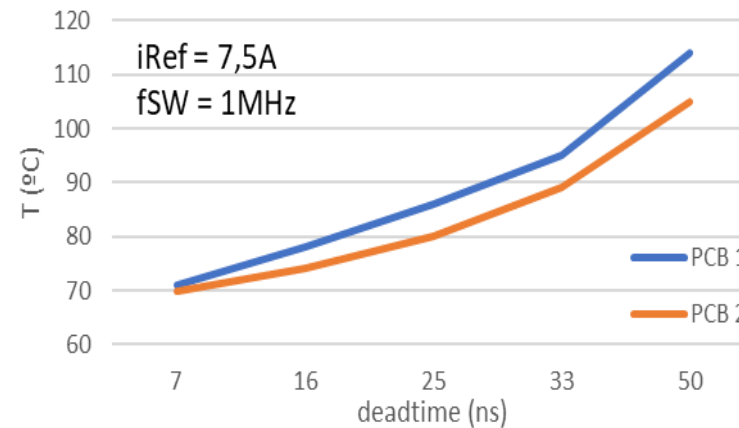
- First simulation studies performed in 28nm based on Verilog-A amplifier models
- Devices types and dimensions studied for shunt and pass-device
- Studies show SLDO thin-gate oxide core transistor implementation feasible in 28nm
- Technology limits maximum input voltage to 1.8V with overvoltage tolerant design (2V @ 65nm)
- Full transistor level implementation ongoing

GaN based power converter for Serial Powering

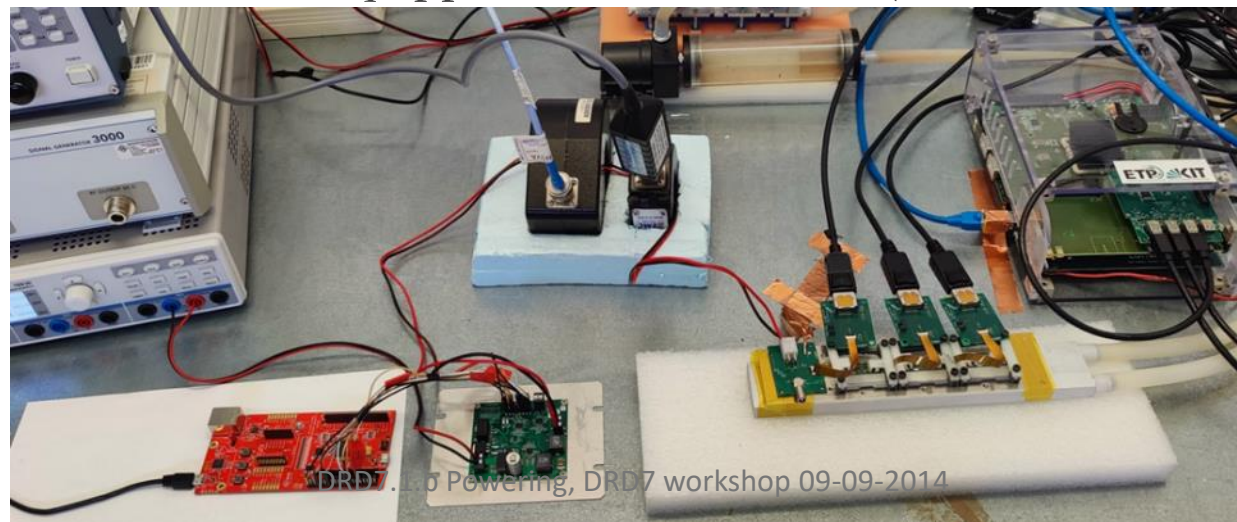
- The main goal of this task is to assess the feasibility of utilizing GaN- based DC-DC converters (current source) for serial powering applications.
- Several critical issues have been identified to optimized the design of these units
 - Design implications associated to GaN switching
 - High frequency (MHz) and short transition times (ns)
 - Precise Duty Control & deadtimes (High Resolution PWM modulator)
 - EMI filter design : Filter embedded in the PCB & magnetic components
 - Radiation hardness
 - Modular /Multiphase concept
- Several activities focused on the development of 200W / 2MHz GaN-based DC-DC have been carried out
 - **Design & Develop a preliminary prototype, which includes (2023)**
 - **Perform a performance evaluation, encompassing efficiency and EMI testing (2024)**
 - This evaluation will also involve combined EMI testing in radiation environments (on going)
 - Design printed circuit boards (PCBs) that incorporate embedded filters and magnetic components.
 - Design & develop a new prototype based on a modular concept, incorporating identified improvements.(2025)

GaN based power converter for Serial Powering

- The performance assessment of the preliminary prototype is almost finalized.

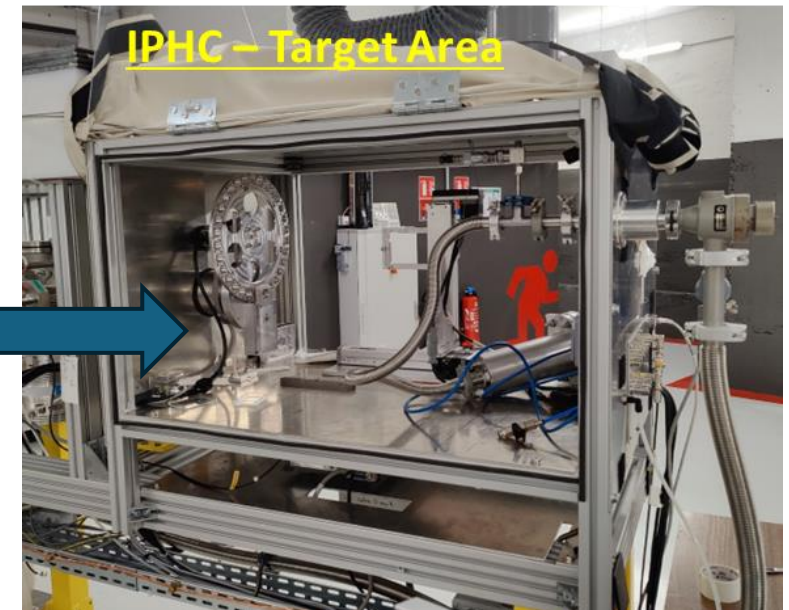
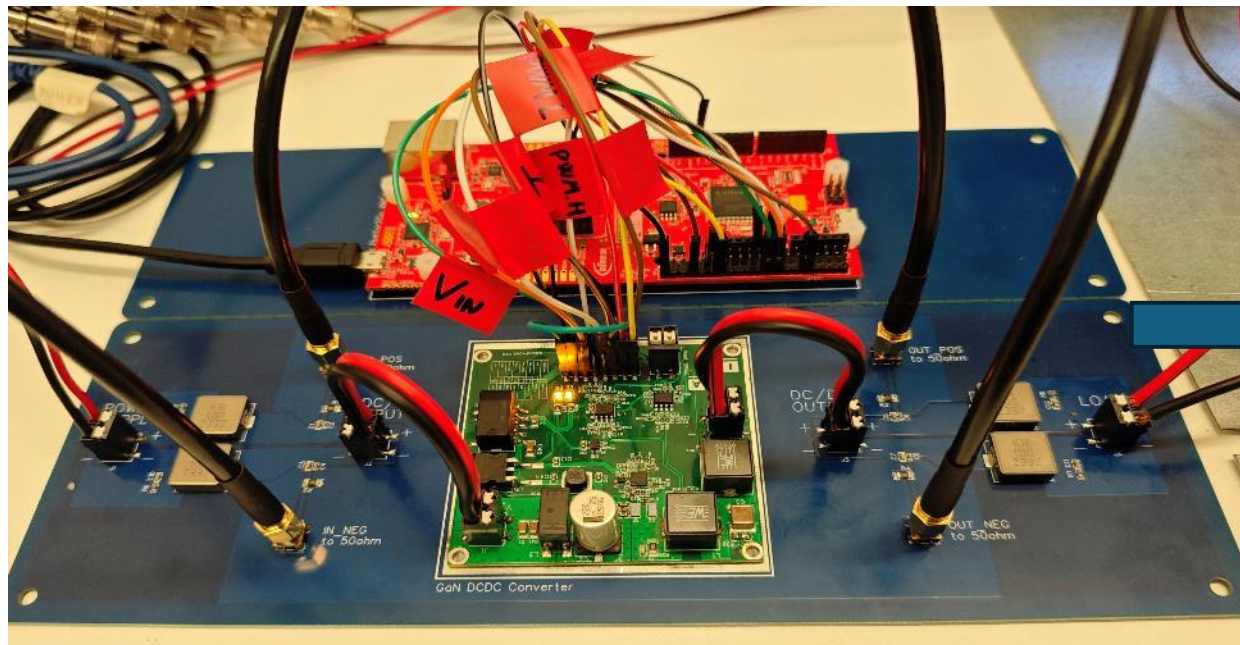


- The preliminary prototype was also tested on a real serial power chain during the noise Transfer Function characterization of 1x2 RD53A modules equipped with 3D sensors (IMB-CNM Barcelona) – CMS IT – Phase II



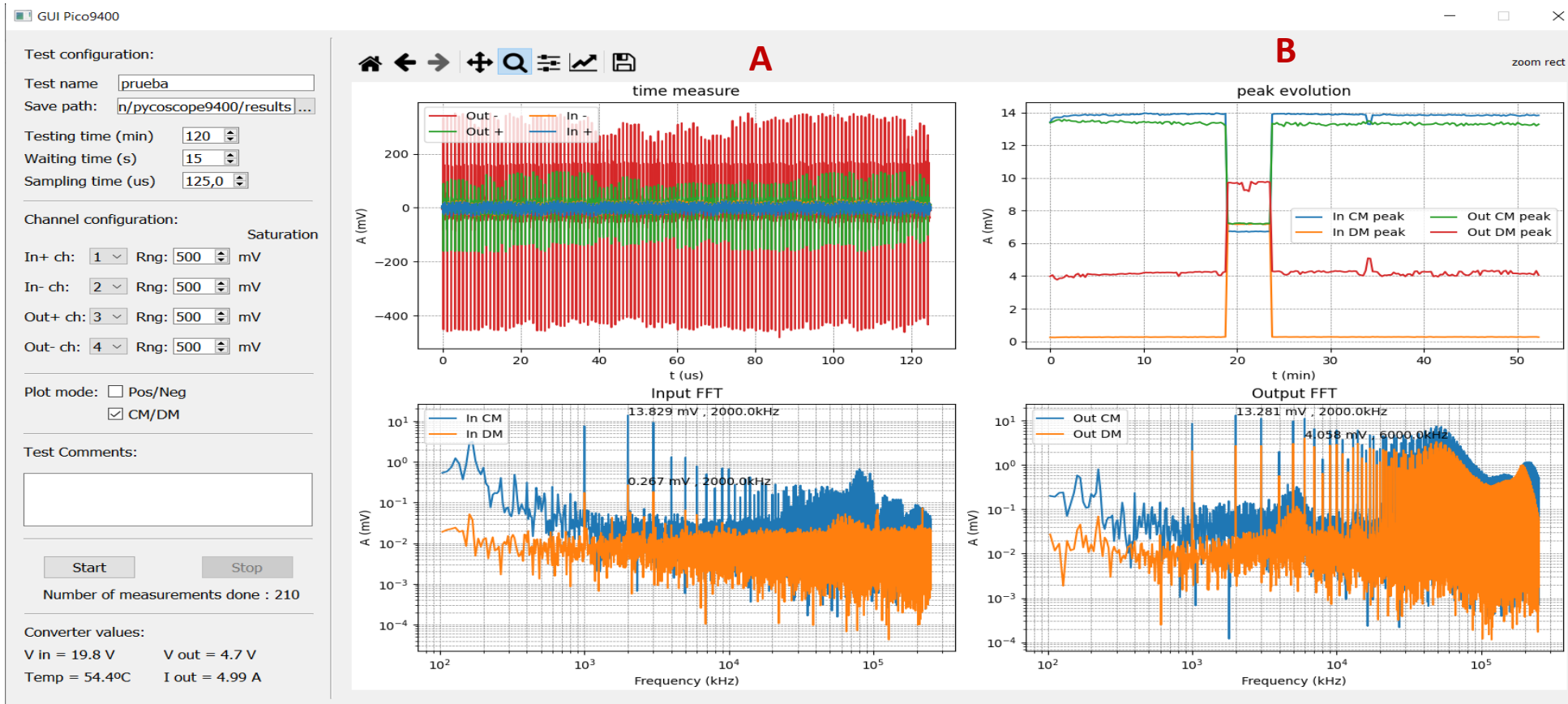
GaN based power converter for Serial Powering

- The EMI evaluation of the prototype was conducted using a specialized setup developed under the AIDAINNOVA project.
 - The setup is portable and fully automated, allowing both time and frequency domain measurements.
 - It is highly effective for measuring transients related to power supplies (PS)
 - The system can also perform noise measurements during radiation campaigns (Measurements are planned at IPHC-Strasbourg).



- Measurements of the noise emission of the DC-DC has been already performed

GaN based power converter for Serial Powering



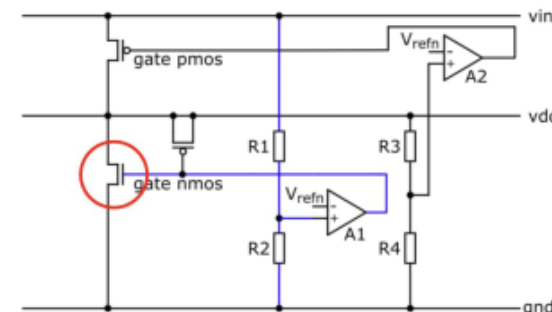
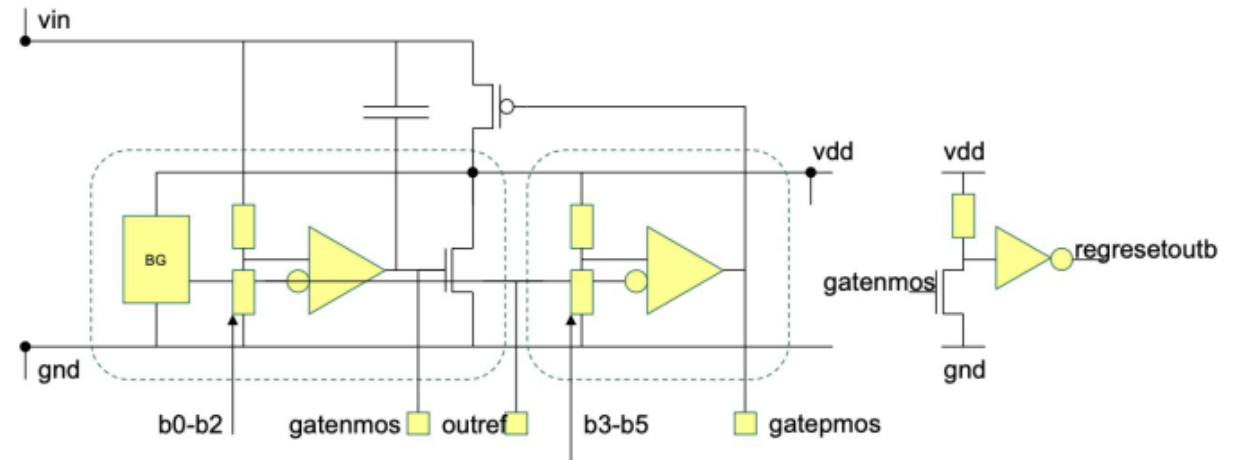
- A. Time domain measurements
- B. Evolution of the maximum peak of all measurements over the test (1hour)
- C. CM & DM at the input (last measurement)
- D. CM & DM at the output (last measurement)

- Next activities:

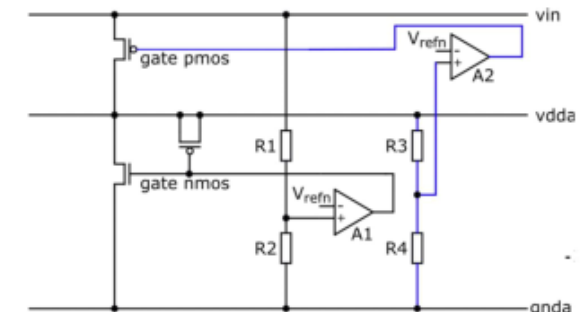
- Radiation camping at IPHC- Strasburg - Including EMI measurements
- Design printed circuit boards (PCBs) that incorporate embedded filters and magnetic components.
- Design & develop a new prototype based on a modular concept, incorporating identified improvements.(2025)

ATLASPIX3.1 Serial Powering

- ATLASPIX3 is a full reticle size monolithic pixel sensor
 - I. Peric (KIT) main designer
- Version ATLASPix3.1 has possibility for serial powering through two shunt/low dropout regulators
 - digital and analog (VDDD/A)
 - 3 bits to tune threshold of shunt regulator
 - 3 bits to tune VDD
 - gatenmos, outref, gatepmos are for monitoring
 - regresetoutb can be used as power on reset
- Possibility to use a single power supply line for all the 6 biases needed to operate the chip



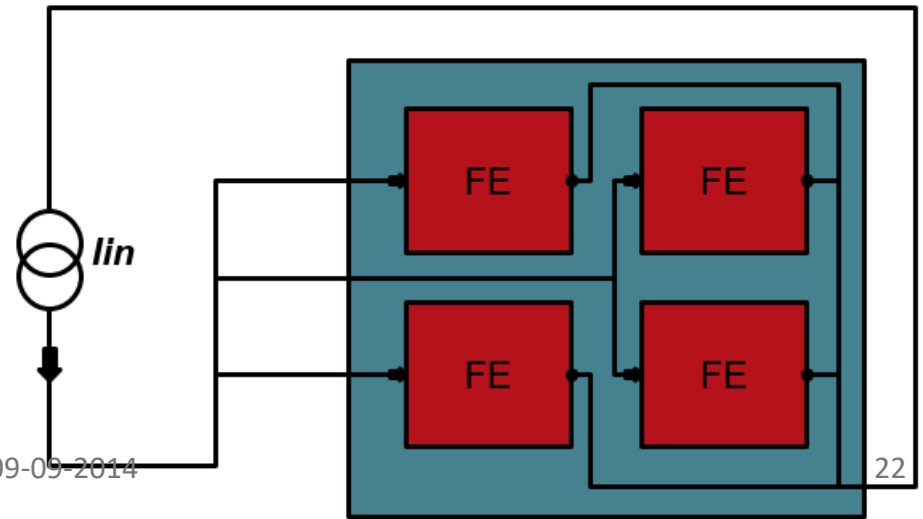
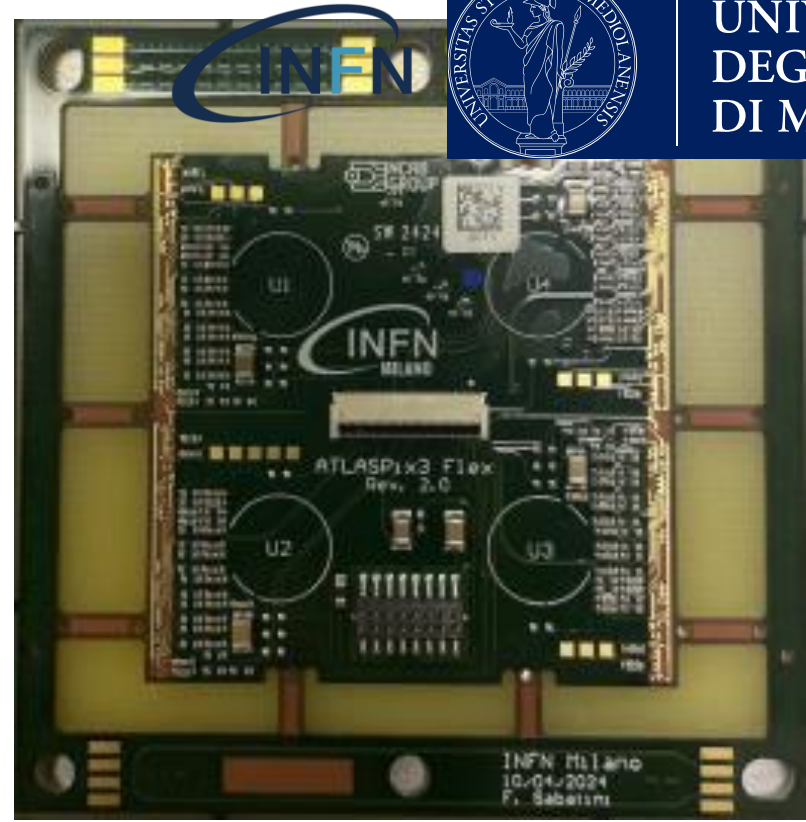
• First loop defines shunt regulators



• Second loop regulates VDDD/As

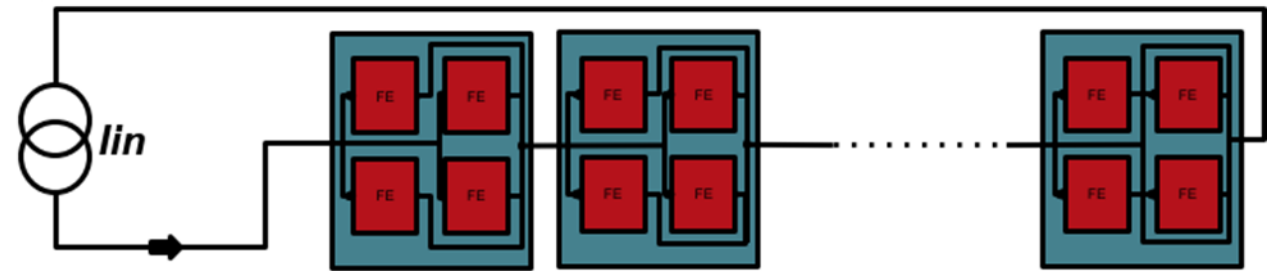
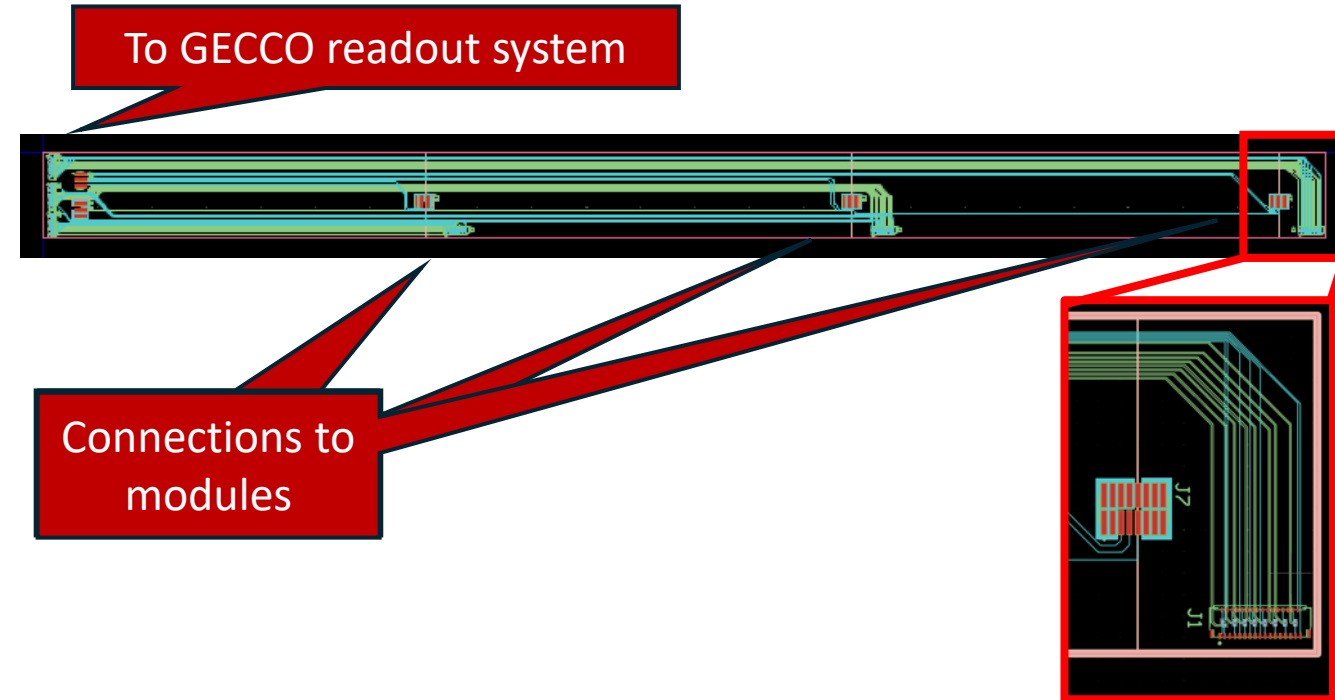
Serial Powered modules

- Developed flex PCB which implement serial powering for multi-chip modules:
 - 4 Front-end regulators are connected in parallel
 - powered with constant current
 - Mechanics compatible with ATLAS ITk pixel modules
- 20 flexes have been produced (Milano) and adapter card for the readout systems are being submitted (Edinburgh)
- Currently testing flex quality and preparing module assembly setup:
 - First modules by end of 2024
 - Verify whether chip-to-chip variation in device performance are not problematic



Serial Power chain

- Next step is to build a chain of modules serially connected
- Preliminary design of a power bus for the chain has been completed
 - Al as conductor to reduce material (target of the work are detector for FCC-ee where radiation length should be minimized)
 - Production to be submitted in Rui de Oliveira's lab after verification of individual module behaviors
- Serial Power chains can be used to test and verify the power distribution system developed within the 7.1b project



Summary

A large community has been built up around powering solutions for HEP applications

Investigate both parallel and serial power distribution solution with low mass, radiation hardness and high efficiency specifications

Main building blocks are:

- GaN DC-DC Converter and GaN DC-DC Current Source, with use of high voltage CMOS and GaN technology up to 48V
- Resonant Converter, 3-level Buck Converter, Capless-LDO and SLDO designed in 28nm technology, aiming 1Grad

There has been a lot of development since last workshop, the collaboration had already a momentum thanks to funds already available. We have functional prototypes for both parallel and serial power.

Funding is granted already for CERN, FH Dortmund, Ita, RWTH Aachen,

Partial funding is already granted for Taltech

Request for funds are pending UNIUD, UNIMI+INFN, TU Graz and Taltech