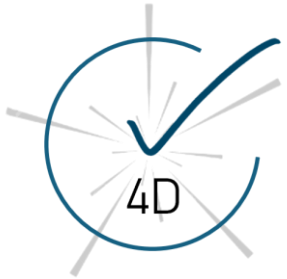
Timing distribution techniques and systems

(Project 7.3b2)



sophie.baron@cern.ch

On behalf of the 7.3.b-2 contributors

Radboud University Nijmegen

Project Target

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Connection with 7.3b1	Support stability tests implementation in HGTD detector slice	NEW! Investigation: online time reconstruction on hardware platform

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Organization

- Members
  - ~25-30 active members* from …
  - 10 Institutes
  - 6 countries

ecfa-drd7-project7_3_b2-contributors@cern.ch
ecfa-drd7-project7_3_b2-observers@cern.ch

*FTE count is much less though ☺

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  - https://indico.cern.ch/category/18005/
  - Kick-off meeting @ CERN in March 2024
  - 2 remote Catch-up meetings in June and September
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- Project Lead
  - Project Lead: Sophie Baron, CERN
    - Sophie.baron@cern.ch
  - Deputy: Javier Galindo, ITAINNOVA
    - fjgalindo@ita.es
  - Rotating every year

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Progress Report

- Assess phase stability and determinism of FPGA transceivers

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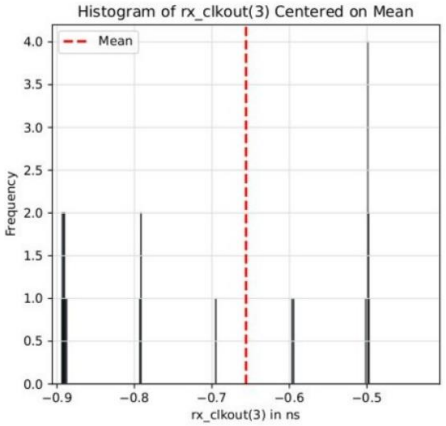
    - Mitigation solutions under development (internal and external)



Court. J.P. Cachemiche

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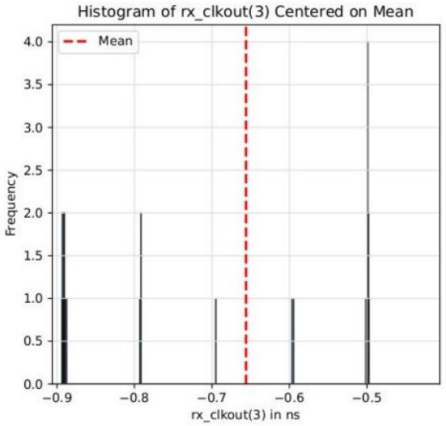
  - Xilinx/AMD (Nikhef)
    - Study correlation between phase and eye opening using Xilinx/AMD internal features
    - Based on FLX-182 with a *Versal Prime* FPGA (VP1802)



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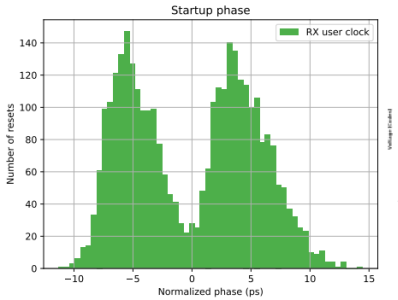

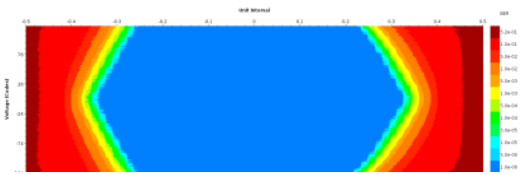

Court. M. Leguijt

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    - WR end node on a uTCA board based on Arria FPGA
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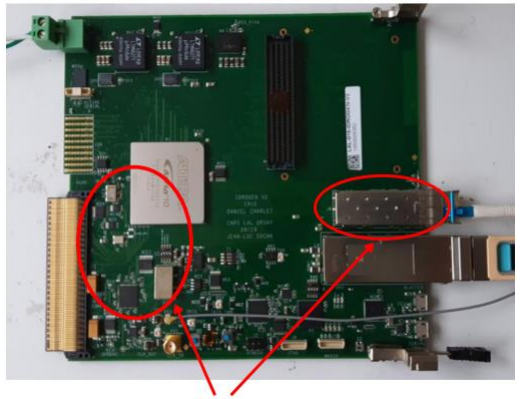
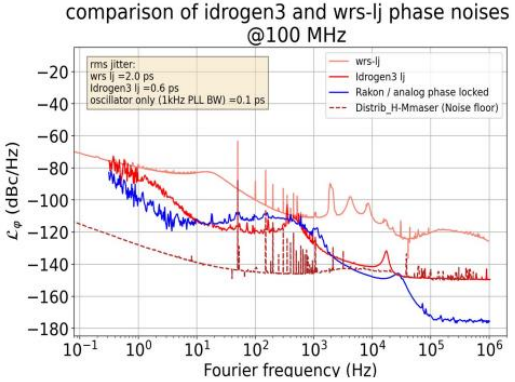
    - Currently at 1Gbps, planning to port to 10Gbps on Agilex





Court. D. Charlet

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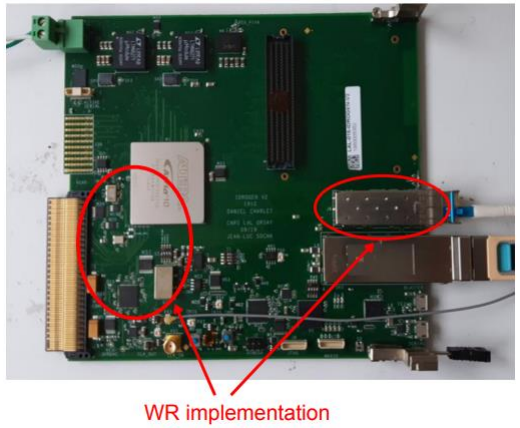

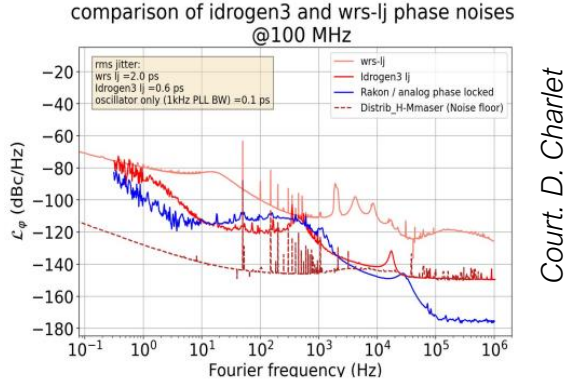

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  - Using White Rabbit for 4D detector (Spanish consortium Itainnova, CNM, IFCA)
    - Detector: multiplane muon tomograph telescope integrating new technologies:
      - LGAD Sensors (IMB-CNM/CSIC)
      - CMS ETROC ASIC (IFCA/CSIC)
    - White Rabbit as reference for clocking in precise ToF measurements (ITA)
      - Implementation on its way in test beam area (WRCLK being recovered at the Front End, now LHC Bunch Clock to be regenerated)

Court. J. Galindo

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- Developing FPGA-agnostic solutions to enforce this stability

Court. E. Orzes

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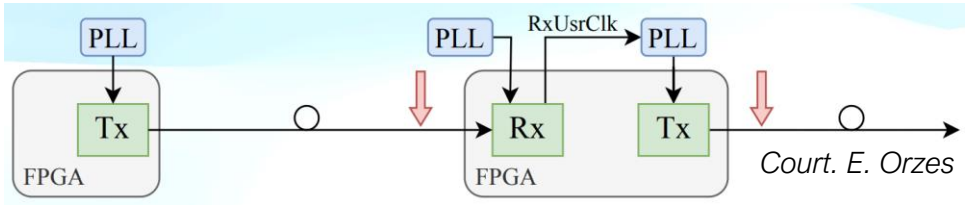
  - Generic hardware and gateware solutions to mitigate FPGA behaviours (CERN, University of Minnesota)
    - Measuring phase shifts and drifts between input and output of FPGA links



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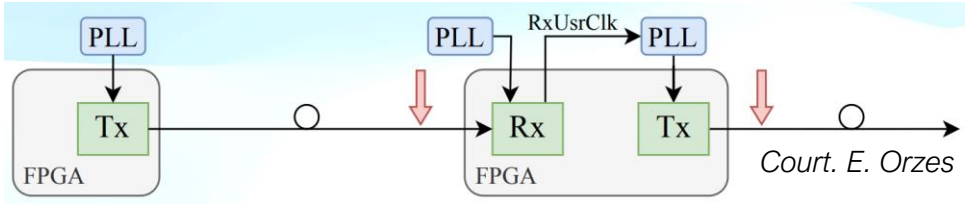
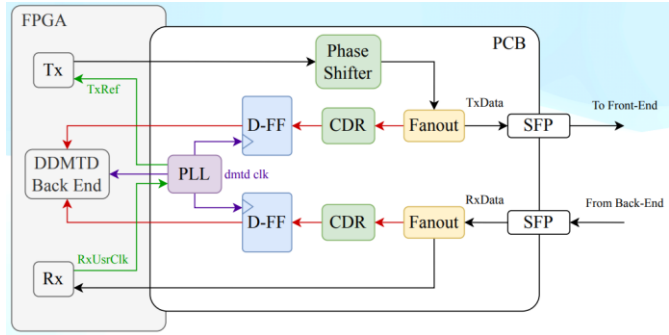


Court. E. Orzes

    - …using FPGA agnostics circuits (COTS or ASICs developed by Minnesota Team)
    - All components have been characterized and Proof-of-Concept validated
    - PCB design is starting
    - New High Precision Phase Shifter ASIC submitted



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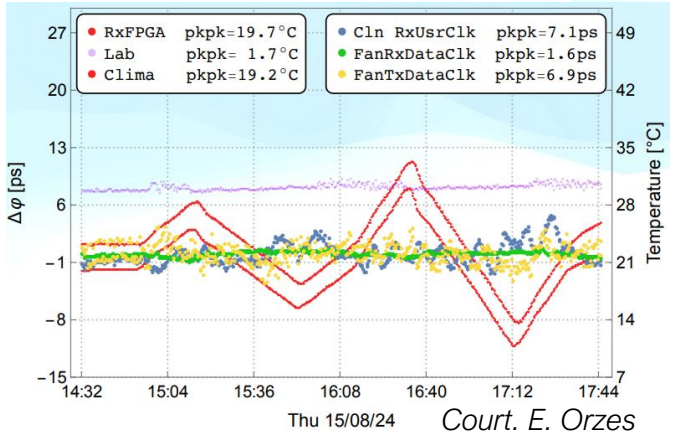

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- Connexion with Project 7.3b1: Strategies for characterizing and calibrating sources impacting time measurements

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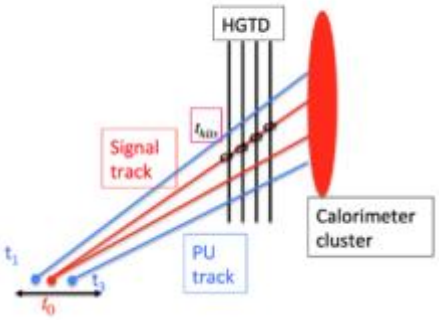
  - Sharing performance obtained with hardware measurements to be injected in simulation
  - Support implement stability tests on a slice of the HGTD detector
  - New proposal from Nikhef & RU Nijmegen on *time data reconstruction*
    - In addition to offline calibration for time compensation…
    - Investigate the possibility of implementing ***online*** time reconstruction on hardware platform

Figure credit: Louis d'Eramo



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- Currently updating contributions wrt results of recent or upcoming funding rounds
  - Almost all Institutes will be able to maintain or even increase effort in the coming year
    - Activity on protocol may be put on hold until next funding round
  - New transversal project activity proposed by Nikhef and RU Nijmegen