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# DRD7 3rd workshop closeout

*A. Rivetti - INFN*

**On behalf of the DRD7 steering committee\***

*\*Jerome Baudot, Marcus French, Ruud Kluit, Angelo Rivetti, Frank Simon, Francois Vasey*

# To start with....

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- This was the first workshop after the **official DRD7 approval** on June 5!
- **From project proposal** to project **implementation**
- Workshop organised along **DRD7 philosophy**: keep the formal part as light as possible and concentrate on **scientific** and **technical** challenges
- More than **100** participants
  
- **Many thanks to all the WP conveners to put together a very stimulating program!**

# DRD7: a project-based R&D on electronics

		DRDT
<b>Data density</b>	High data rate ASICs and systems	7.1
	New link technologies (fibre, wireless, wireline)	7.1
	Power and readout efficiency	7.1
<b>Intelligence on the detector</b>	Front-end programmability, modularity and configurability	7.2
	Intelligent power management	7.2
	Advanced data reduction techniques (ML/AI)	7.2
<b>4D-techniques</b>	High-performance sampling (TDCs, ADCs)	7.3
	High precision timing distribution	7.3
	Novel on-chip architectures	7.3
<b>Extreme environments and longevity</b>	Radiation hardness	7.4
	Cryogenic temperatures	7.4
	Reliability, fault tolerance, detector control	7.4
	Cooling	7.4
<b>Emerging technologies</b>	Novel microelectronic technologies, devices, materials	7.5
	Silicon photonics	7.5
	3D-integration and high-density interconnects	7.5
	Keeping pace with, adapting and interfacing to COTS	7.5

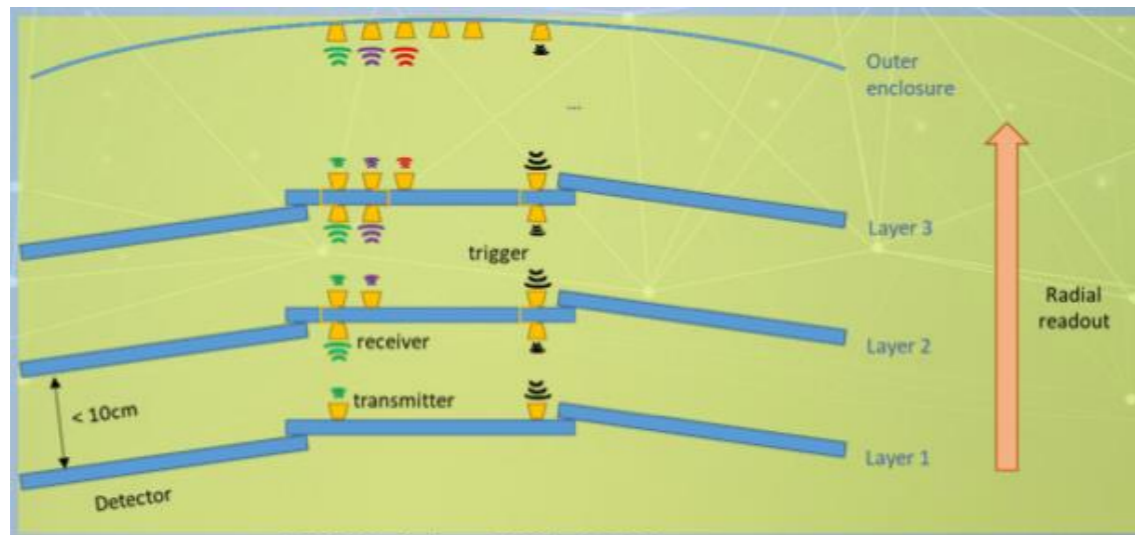
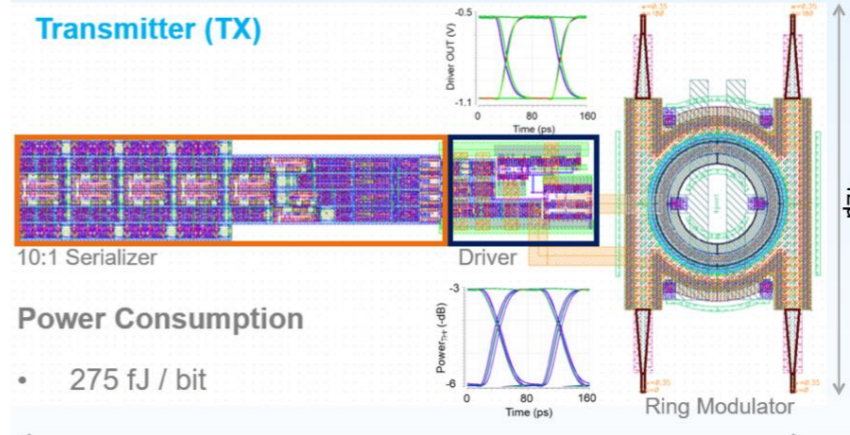
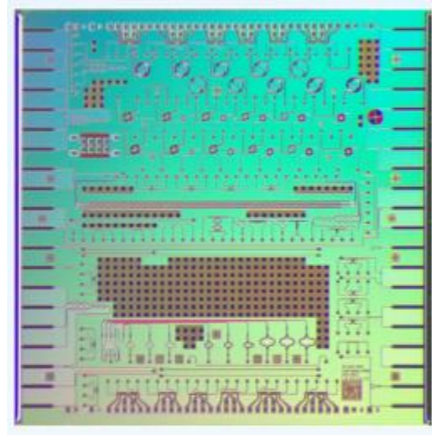
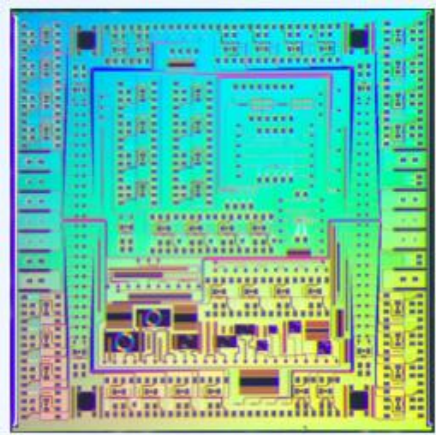
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# Some (very personal) highlights

# Toward 100 Gb/s link...and beyond

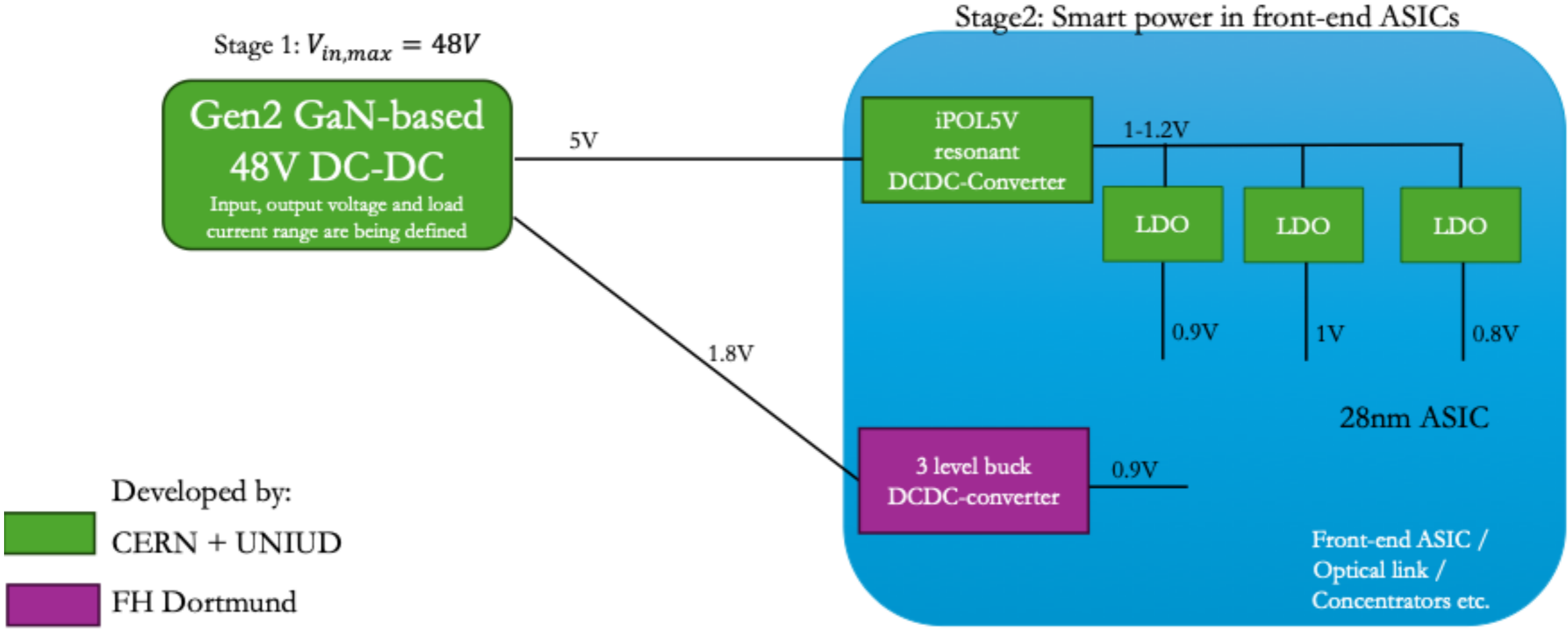
## Performance Target

100 Gb/s per fibre optical readout with 2.5 Gb/s control optical link operating at a BER of  $10^{-12}$ . Radiation tolerance up to  $1 \times 10^{16}$  particles/cm<sup>2</sup> and 10 MGy and power consumption of 250 mW. Cryogenic temperature operation for some lower-speed variants.



# Beyond current mirror bias...

## WP 7.1b: parallel power (DCDC)



# More standardization

Introduction and motivations    The SOCRATES platform    The TriglaV prototype    Final topics and future plans

## Examples of applications in HEP

### Control and monitoring applications

- Stand-alone radiation-tolerant microcontroller – architecture and peripherals customised for application
  - LHC beam monitoring
  - On-detector slow-control operations
  - Others...
  - Power management
  - Detectors monitoring
- Controller embedded in front-end ASICs as pixel read-out chips
  - Dynamic power management
  - Take over and automatise task from the back-end:
  - Possibility to reprogram it in any moment, making it very flexible for new applications

### Data processing application – future target

- Data elaboration and pre-processing
- Replace fixed state machines and data pipelines with programmable logic
- Offload performance critical functions to specialized accelerators

RADIATION TOLERANT RISC-V SOC | DRD7 COLLABORATION ON ELECTRONICS AND ON-DETECTOR PROCESSING | 9 SEPT 2024 | ALESSANDRO.CARATELLI@CERN.CH | 2

- **How much intelligence on the front-end?**

# Physical design on reliable specs

...or avoid excessive safety factors and duplications!

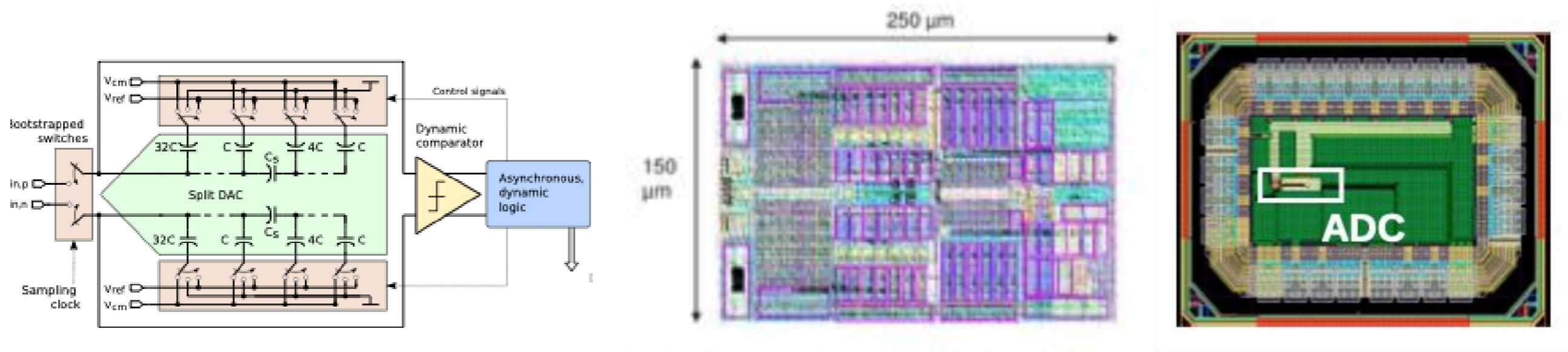
## Virtual Electronic System Prototyping (WP7.2c)

<b>Project Description</b>	<p>Develop frameworks for high-level simulation of particle detectors.</p> <p><b>Topics:</b></p> <ul style="list-style-type: none"> <li>1- Signal generation in detector elements</li> <li>2- Digitization and Signal Processing</li> <li>3- Data readout architecture</li> </ul> <p>Topics 1. and 3. aim to create independent frameworks that can be used as a single toolchain. Topic 2. will be better defined during the project and might converge in one of the two frameworks or represent a third framework of the chain.</p> <p>Duration 3-4 years.</p>	<b>Multi-disciplinary, cross-WP content</b>	<p><b>Detector Technologies:</b> support various detector technologies</p> <p><b>Particle Physics Models:</b> integration of comprehensive particle physics models</p> <p><b>Geometric Configurations:</b> ability to define and customize the geometry</p> <p><b>Data Formats:</b> support for common data formats</p> <p><b>Monte Carlo Techniques:</b> implementation of Monte Carlo methods for simulating particle interactions and energy depositions,</p> <p><b>Electronics Simulation:</b> accurate modeling of the readout electronics</p> <p><b>Readout Architectures:</b> support triggered and data-driven systems</p>
<b>Innovative/strategic vision</b>	<p>Develop a toolchain for virtual prototyping to:</p> <ul style="list-style-type: none"> <li>1- model detector at high-level</li> <li>2- perform architectural studies</li> <li>3- provide a reference model for the verification</li> </ul>	<b>Contributors</b>	<p>CERN</p> <p>FR: IPHC Strasbourg</p> <p>USER: PSI (CH), UK Cons., INFN Cagliari (IT)</p>
<b>Performance Target</b>	<p><b>Topic 1:</b> Cluster multiplicity: 1-10 Position resolution: <math>&lt;10 \mu m</math> Time resolution: 10 ps to 100 ns</p> <p><b>Topic 2:</b> to be defined in M7.2c.2</p> <p><b>Topic 3:</b> Accuracy: Event/Cycle-level Speed: hundred thousand transactions per second Scalability: readout components library Verification: integrate in verification environment User-Friendly: docs &amp; support for user-only roles</p>		



# High performance IPs

- Many interesting developments going on
- How to we manage sharing of IPs
- Encourage even closer collaborations










# Even more precise timing...

## Project Target



- This project aims to study and propose strategies to optimize and assess ultimate precision and determinism of timing distribution systems for future detectors:

Assess phase stability and determinism of COTS and Systems used in HEP	All kinds of FPGAs 	Systems (White Rabbit) 
Develop FPGA-agnostic solutions to enforce clock stability	Generic hardware and gateway solutions to mitigate FPGA behaviours 	Protocols allowing direct clock extraction 
Connection with 7.3b1	Support stability tests implementation in HGTD detector slice 	Investigation: online time reconstruction on hardware platform  

# Going to the extremes: very cold

ECFA

European Committee for Future Accelerators



## DRD7.4.a - summary and outlook



- ❖ Silicon **foundries** are providing (e.g. Skywater 90nm) or planning to **provide access** (e.g. GF 22FDX) to cryo-PDKs.
- ❖ Fermilab, EPFL, FZJ have ongoing funding and a solid track record (instrumentation, facilities, competences) for the development of cryo-PDKs, including test-chip design, characterisation down to 40 mK and **cryo-PDK development** in a collaborative effort **involving industry partners**.
  - To do: Cryogenic noise measurements, study radiation hardness at cold, AI/ML\* based PDK development
- ❖ For DRD7.4a, other partners (UK, INFN, others) are expected to provide support and contribute to die-level and wafer-level device characterisation.
- ❖ Involvement of industry for model library is related to funding availability. Choice of EKV or BSIM models to be done.
- ❖ **Choice of target technology** for the DRD7.4a project needs to happen at the beginning of 2025: TSMC 28nm is baseline
  - A dedicated consortium agreement to define the **distribution and licensing conditions** of the DRD7.4a cryo-PDK will probably be needed.

\* <https://www.infineon.com/dgdl/Infineon-24-0010-010.pdf>

# Going to the extremes: radiation

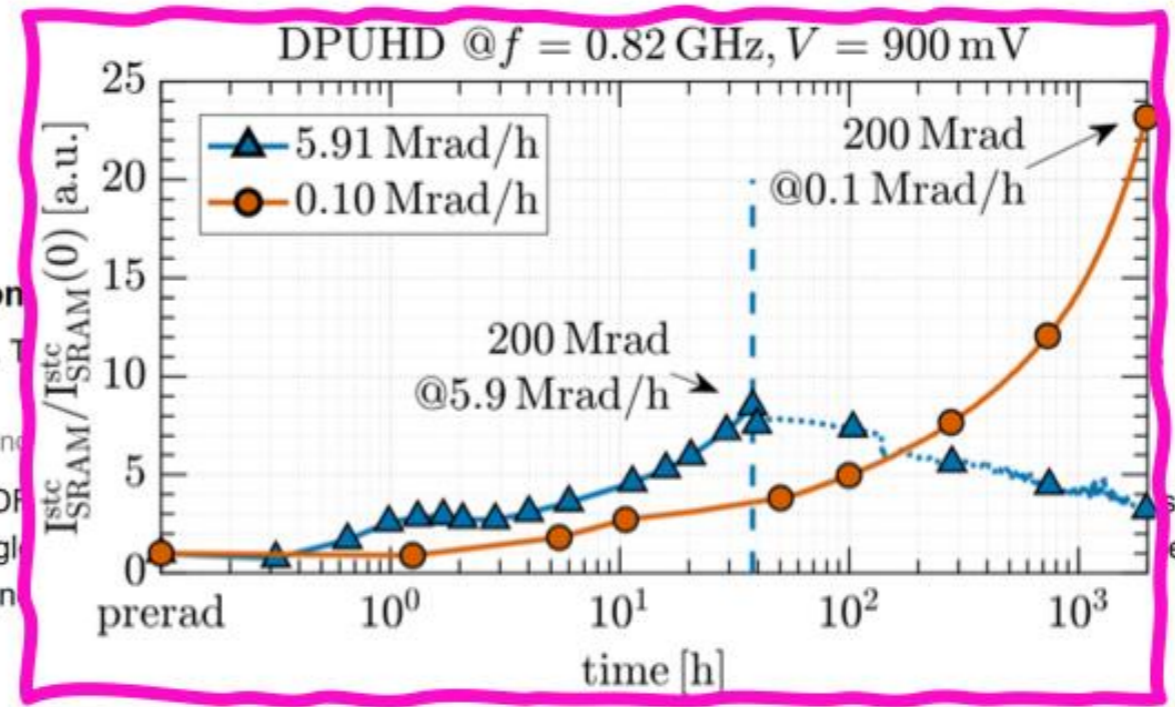
- Irradiation in more realistic conditions
- Radiation-aware PDK



DRD7: AN R&D COLLABORATION ON ELECTRONICS AND ON-DETECTOR PROCESSING

low-dose-rate tests on 28nm CMOS technology

**H4**  
**ELDRS in a con**  
G. Borghello<sup>1</sup>, G. T  
K. Kloukinas<sup>1</sup>  
1. CERN (Switzerland)  
Evidence of ELDRS  
SRAMs, and single  
was evaluated, an



2024/09/10

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# Going to the extremes

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- How we combine both?



# Electronics needs cooling

DRD7: AN R&D COLLABORATION ON ELECTRONICS AND ON-DETECTOR PROCESSING

## Conclusion (1/2)

- Ceramics
  - It has also the potential to include electronic features
  - Fully validated initial prototypes in the coming years to high pressure, leak tightness and cooling performance in the following years
  - LHCb VELO Upgrade 2 as benchmark requirements (High pressure, CO<sub>2</sub> evaporative cooling)
- Metal 3D printing
  - X-ray tomography indicates issue with the fill factor
  - Distortion observed created a choke point
  - New run printed
    - focus on improving distortion and fill factor and investigation of electropolishing (material reduction/easier integration?)
- Microchannel cooling and active interconnection developments (CNM, DESY, IFIC)
  - Aiming to bring more functionalities to the cooling plate
    - Redistribution layer could be an interesting solution for ASICs with through-silicon vias
  - CMOS compatible process to integrate the cooling to the sensor

# Electronics needs cooling

DRD7: AN R&D COLLABORATION ON ELECTRONICS AND ON-DETECTOR PROCESSING

## Conclusion (2/2)

- Microchannel cooling manufacturing via thermocompression (CPPM)
  - Main motivation to reduce the manufacturing cost
    - Very promising results “hyperbar” chamber (resistance to high pressure)
  - Techniques developed can be also explored for integration (chips and connecturization)
- DRD7/8: Cooling and cooling plates
  - “*Mechanics*” in DRD8 and “*Electronics*” in DRD7
  - First version of the draft by end of September in the DRD8
  - Request for descoped DRD7 proposal afterwards

# Trigger and DAQ

## Summary

- 7.5a is aiming for common TDAQ development with COTs.
  - Mainly focus on trigger with various platforms.
  - Also generic development for fundamental purpose.
- Our collaboration will be based on the sharing of technical knowledge of
  - Software/firmware framework
  - Hardware device
  - Using git repository, or even hand-on workshop in the future
- Present activities:
  - PI: Alex Keshavarzi (Manchester), Yun-Tsung lai (KEK IPNS)
  - Monthly meeting on the first Friday of every month
  - Mailing list:  
ECFA-DRD7-WG7\_5-Contributors@cern.ch  
ECFA-DRD7-WG7\_5-Observers@cern.ch
- If you are interested in relevant research works and would like to join us, please do not hesitate to let us know!

**FPGA, GPU, ML, HLS**



# Front-End to Back-End @ 100 Gb/s

## Investigation Themes



Theme 1 : using 100GbE COTS switches to handle data-streams from the Front-End to Network Interface Cards (NICs) or even DAQ processors (CERN LBC and ESE groups).

Theme 2: design of a COTS-based high-density switch bridging the detector environment to the COTS/DAQ world (Imperial College).

Theme 3 : to explore DAQ topologies (based on custom boards for DAQ, concentration and processing) (CPPM CNRS/IN2P3, Nikhef, Brookhaven National Lab)

Theme 4 : study and design of the building blocks IPs necessary for 100Gb Ethernet cores implementation in future FE ASICs. (Rutherford Lab)

- **Evolutionary, visionary...transformative!**

# CMOS technologies for sensors

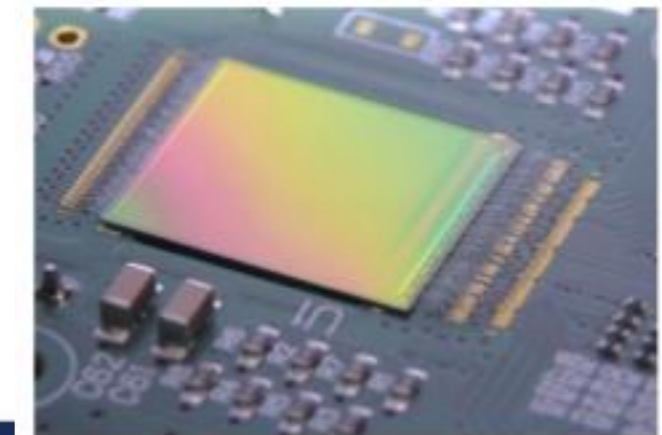
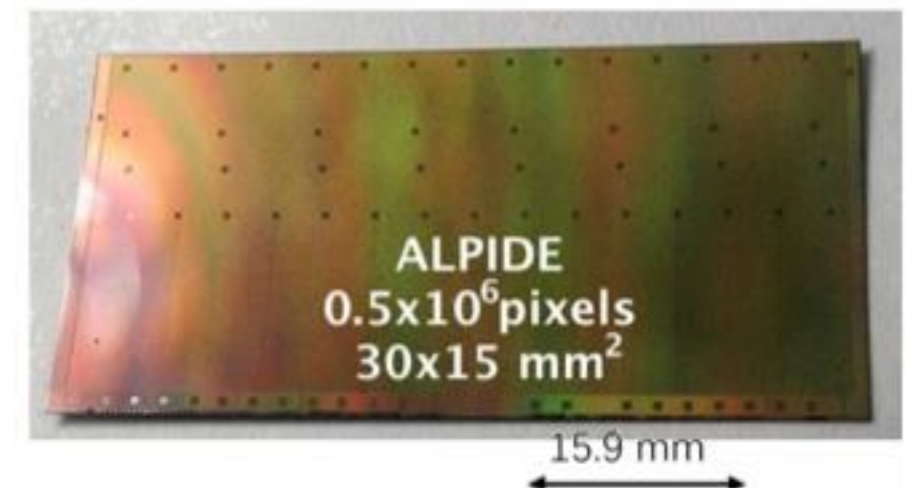
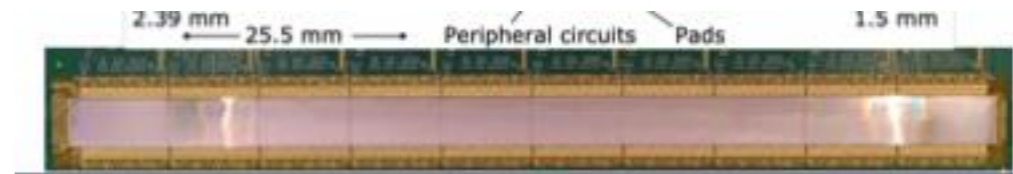
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DRD7.6

<b>Project Name</b>	Common Access to Selected Imaging Technologies (WP7.6a)
<b>Project Description</b>	Provide common access and centralized support for selected CMOS imaging technologies, including specific IP development to accelerate the design effort. Duration 3 years, expected to be extended.
<b>Innovative/strategic vision</b>	Potential of monolithic technologies, confirmed by successful ALICE ITS2 tracker and the widespread community interest. Efficient and affordable technology access requires concentration of the resources in the community.
<b>Performance Target</b>	Organize common runs and efficient and cost-effective access to selected technologies.
<b>Multi-disciplinary, cross-WP content</b>	Concerns several detectors types, calorimeters, tracking, etc. Serves other DRDs like DRD3 and DRD6, experiments and projects in HEP. Strong connection with 7.6b (e.g. 3D integration of chiplets). Requires expertise in analog and digital IC design, device design and technology, and significant testing effort.
<b>Contributors</b>	CH: CERN FR: IN2P3: CPPM, IPHC, IP2I + others IT: INFN(TO, TIFPA, MI, BO, PD, PV, PG, PI) NL: NIKHEF NO: UiB, UiO and USN UK: STFC US: TBC, SLAC already doing effort

**Technologies targeted initially: TPSCo 65nm ISC, TJ 180nm, LF 110nm IS**



DRD7.6 – Complex Imaging ASICs and Technologies

# Shared access to 3D integration

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DRD7.6

Shared Access to 3D  
Integration

## ***Proposed Milestones and Deliverables***

- M7.6b.1 (M18) Establish TSVs process on active/passive interposer, wafer/single die
- M7.6b.2 (M24) Establish RDL process and back-side metallization on real CMOS sensors and custom-designed silicon interposer
- D7.6b.1 (M30) Delivery of report summarising the integration of SiPh on detector by 2.5D interposer/chiplet technologies (→ with DRD 7.1)
- D7.6b.2 (M30) Delivery of a report on W2W bonding by industrial partners
- D7.6b.3 (M36) Deliver documentation of the process for the common use

# Shared access to 3D integration

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DRD7.6

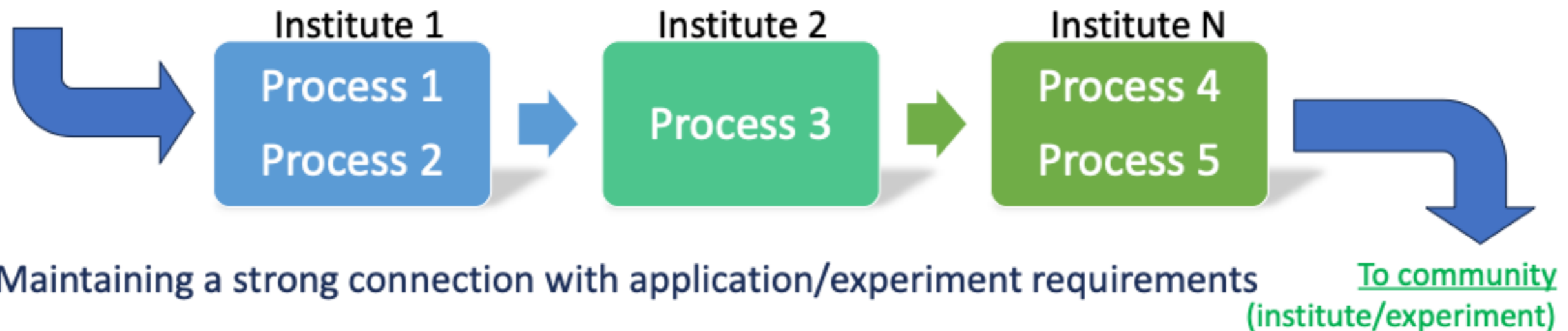
Shared Access to 3D  
Integration

## *International Distributed Detector Laboratory*

- Establish a distributed laboratory that operates as a hub-service for the community
- Each institute highly specialized in one or more technological processes

### From community:

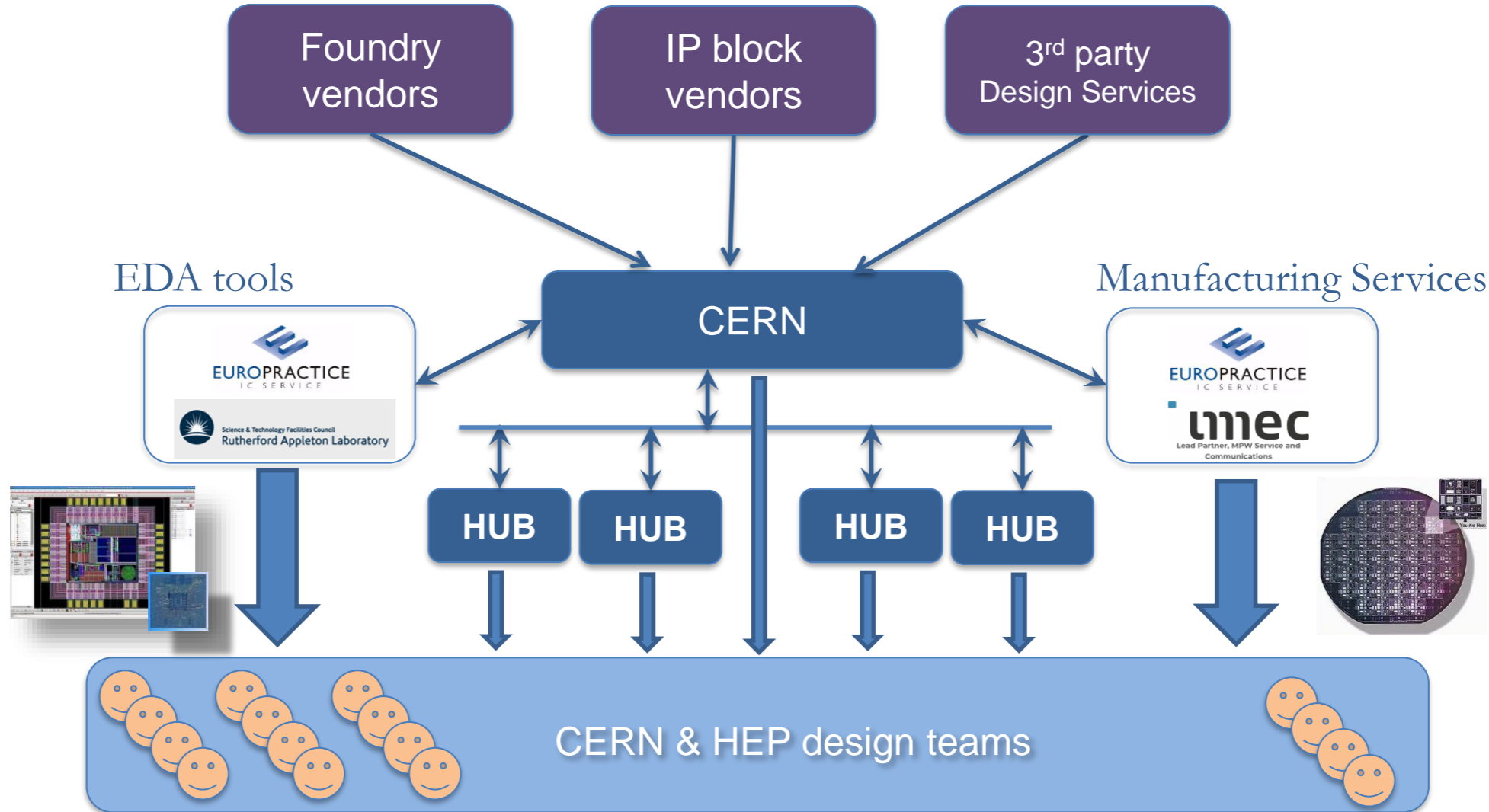
- Request of process/service
- Rapid prototyping of new detector
- Detector production (large scale)



# Maximizing efficiency



## HUB based support service



[asic.support@cern.ch](mailto:asic.support@cern.ch)

# Last, but not least...

- We have a website: do not forget to populate it!



DRD7 COLLABORATION HOME ACTIVITIES EVENTS CONTACT

Q Search

## DRD7: R&D Collaboration on Electronics and On-Detector Processing

The CERN DRD7 collaboration is dedicated to advancing electronic systems and technologies for particle physics detectors. This active collaboration builds on the intention expressed in the Letter of Intent [1] submitted on September 15, 2023, and addresses the critical need for high-performance electronic systems as outlined in the ECFA R&D Roadmap [2]. Given the increasing complexity and cost of these systems, DRD7 focuses on developing and demonstrating new hardware, firmware, and software concepts. The work prioritizes low Technology Readiness Levels (TRLs), targeting disruptive, transformative, and far-reaching goals. This approach sets DRD7 apart from other DRD collaborations, which focus on higher TRL level components needed for immediate detector developments.

The collaboration unites experts from various European and international institutes to tackle projects that are too complex for any single institute to manage alone. By adopting open development practices and facilitating the sharing of intellectual property, DRD7 enhances the efficiency and capability of all participants. The work is organized into several [work packages](#), each targeting specific technical goals and aligning with the strategic recommendations of the Roadmap. Additionally, efforts are underway to establish common standards and approaches for electronics, which will support the broader DRD program.

[1] [DRD7 Steering Committee, Letter of Intent DRD7: R&D Collaboration for Electronic Systems](#), Technical report, Geneva, September 2023.

[2] [ECFA Detector R&D Roadmap Process Group, The 2021 ECFA Detector Research and Development Roadmap](#), Technical report, Geneva, 2020.

<https://drd7-test.web.cern.ch/>

# Last, but not least...

- Do not forget to cast your ballots for the CB chair election!



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## Actions

I would like to organize the next steps if elected

- CB meeting in October
  - discussion of collaboration rules
    - organize offline vote on major items submitted to the board
  - approval of CB Chair Deputy
  - (Resource Coordinator)
- CB meeting in November
  - approval of text of the collaboration rules
    - need enough time for the draft to be circulated and commented
  - start of the process of nomination for Steering Committee/Spokepersons
  - *open a competition for the DRD7 logo* 😊
  - (set up of the Resource Board)
- Elections in December/January, depending on the outcome of the nomination process
- CB meeting late January/beginning of February
  - endorsement of appointments by the governance (WP coordinators, deputies...)

# Here we are...





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**See you at the next workshop!**