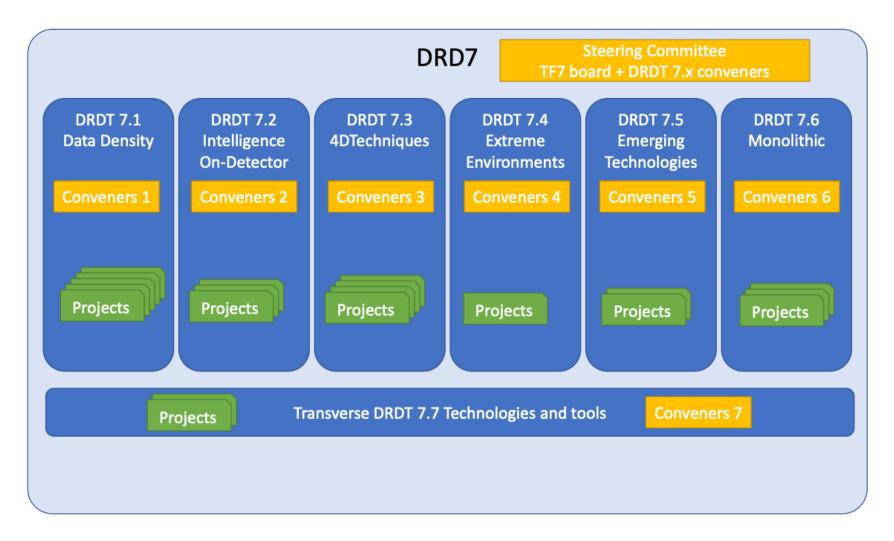
DRD 7.7 Technologies & Tools

CERN

9 Sept. 2024

Xavi Llopart (CERN) Mark Willoughby (STFC, UK) Kostas Kloukinas (CERN)







In response to the DRD7 projects and in order to manage ASIC-related design risks in our distributed community, the Steering Committee invites Conveners of WG7.7 to create and steer a task force that will propose an implementation solution for a hub-based structure for ASICs developments

- WG7.7 Conveners
 - Xavi Llopart (CERN)
 - Mark Willoughby (STFC, UK)
 - Kostas Kloukinas (CERN)



The overall goal of this Hub-based structure is to:

- <u>Establish and maintain access</u>, for the community at large, to state-of-the art <u>microelectronics technologies and EDA software tools</u> through regional collaboration and coordination
- <u>Ensure a professional approach to prototyping and production fabrication cycles</u> by delivering best practice in design, verification and foundry submission,
- <u>Facilitate collaborative work</u> across distributed design teams establishing the necessary infrastructure for <u>IP block sharing</u>, and
- <u>Follow rigorous project review</u> and submission processes to manage risks and control changes in projects



The Hub institutes will collectively:

- Provide access to necessary technical support for projects to ensure rigorous completion of all design validation and foundry design rules checks. Maintain signoff checklists, foundry submission check lists and 'lessons learned' logs to support each other and build best practice
- <u>Coordinate fabrication manufacturing runs and IP library access</u> in partnership with supported foundries, CERN ASIC support and Foundry Services and Europractice
- <u>Maintain a master list of all current projects</u> to enhance global overview and forecast foundry access

Locally, in their region, Hub institutes will also:

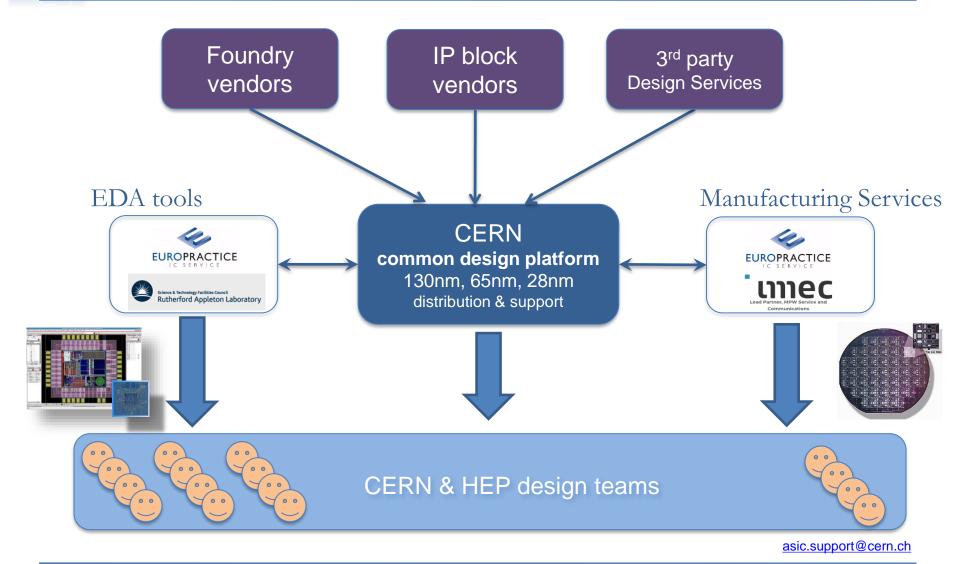
- Lead the preparation and <u>management of IP sharing agreements</u> that meet the needs of their region
- Ensure that the <u>strict end-use rules</u>, export controls and taxation issues in each region are recognized, understood and met by their community, and
- <u>Engage with their local funding agencies</u> to ensure that support and submission management costs are planned for and included in projects.



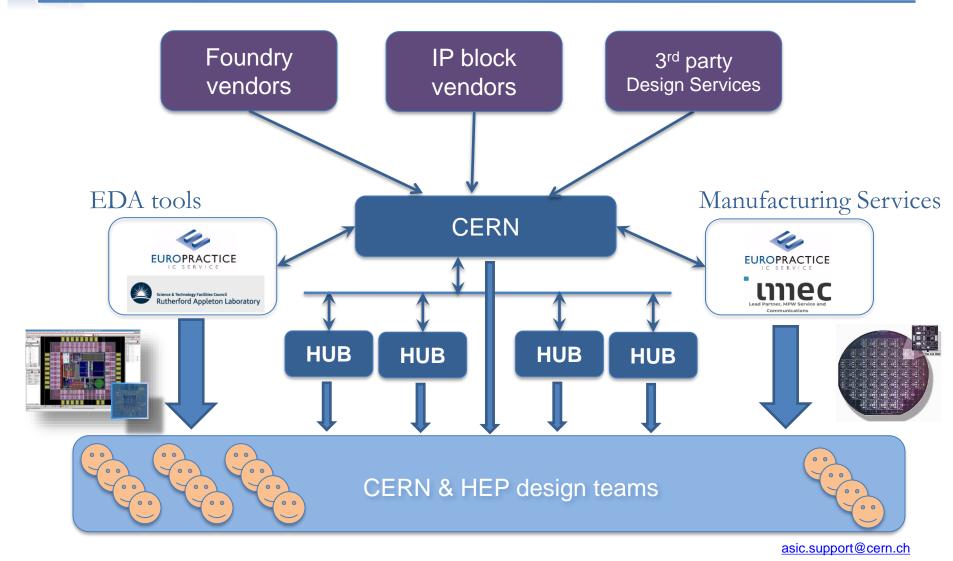
CERN, as lead focus, will coordinate the overall structure and undertake central roles including:

- Negotiating legal and commercial aspects for accessing new technologies on behalf of the community
- Maintaining a list of Institutes eligible to collaborate on NDA protected technologies Providing technical support and training to Hub Institutes
- Working with Hub institutes to develop "common design platforms" and to facilitate maintenance, technical support, training and collaboration, and
- Assisting in supporting the wider community when circumstances prevent a regional Hub from doing so





HUB based support service



15/3/2023



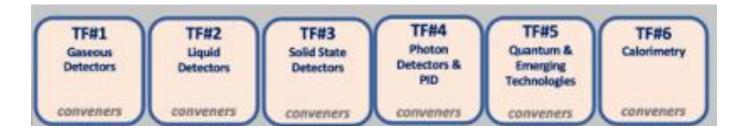
The timeline for the taskforce to propose an implementation solution to the Hubbased model sketched above is <u>12 months</u>.

The proposal will identify the hub institutes and their interactions, the supported technologies and target projects, and will propose a roadmap for presenting, discussing and rolling out the new structure for the DRD community.



DRD7.7 must maintain links with the DRD7.x Workgroups

- Promote cross-collaboration
- Disseminate knowledge across Workgroups
- Link-persons to other DRD7.x
 - DRD7.1: Marco Bregant and Sorin Martoiu
 - DRD7.2: Elena Gramellini
 - DRD7.3: Jerome Baudot, Eva Vilella
 - DRD7.4: David Gascon
 - DRD7.6: Christophe de la Taille





- Call for Institutes to present their interest to participate in the HUB structure
- Create and steer a task force that will propose an implementation solution for a hub-based structure for ASICs developments
 - Workgroup Link Persons will be contacted
- Please contact WG7.7 conveners
 - TWEPP2024 presents a nice opportunity for discussions







- Technology Challenges
 - Augment EDA Tools -> EUROPRACTICE
 - Access to Advanced technologies -> EUROPRACTICE
 - Integrate support for "More than Moore" technologies
 - 3D Interconnect & Advanced Packaging
 - SiPh
 - CMOS Imaging (monolithic sensors)
 - Specialty embedded devices

Design Challenges

- System Architect role
- System Level Modeling and Simulations
- Design Verification at System Level and component level
- Establish & Conform to a Rad-Tol SoC infrastructure

Productivity Requirements

Establish a Collaborative Work structure

Enablers for Collaborative Work

Technical Framework

- Comprehensive "common design platforms"
 - Foundry PDKs & Foundry IP blocks
 - Rad-Tol IP blocks and IP block repository
 - Rad-Tol SoC infrastructure
 - Design & Verification methodologies
- Access to common EDA tools
- Maintenance, Training & Support services

Legal Framework

- 3-way NDAs with Foundries permitting technology data exchange
- Commercial Contracts with Foundries
- EULAs of EDA tool providers permitting IP block sharing
- IP block sharing agreements among design teams
- Export Control regulations

Technology Challenges

Complex deep-submicron silicon manufacturing processes Powerful, Flexible but highly Complex EDA Tools Design Challenges **EDA** software Tools Designs of increasing complexity and size Design **Methodologies** Novel designs for scientific instrumentation **Radiation Tolerance** 90 nm 45 nm 14 nm **Productivity Requirements** 130 nm 65 nm 28 nm Large, fragmented, multinational design teams Technology Designers with different levels of expertise scaling Work on common design projects 130 nm 90 nm 65 nm 45 nm 32 nm <u>22 nm</u> 2003 2005 2007 2009 2011 Costly technologies Importance of 'first-time-right' designs ! 15

Challenges in ASIC design @ HEP