H2M: Characterization of a MAPS in a 65 nm CMOS Imaging Process

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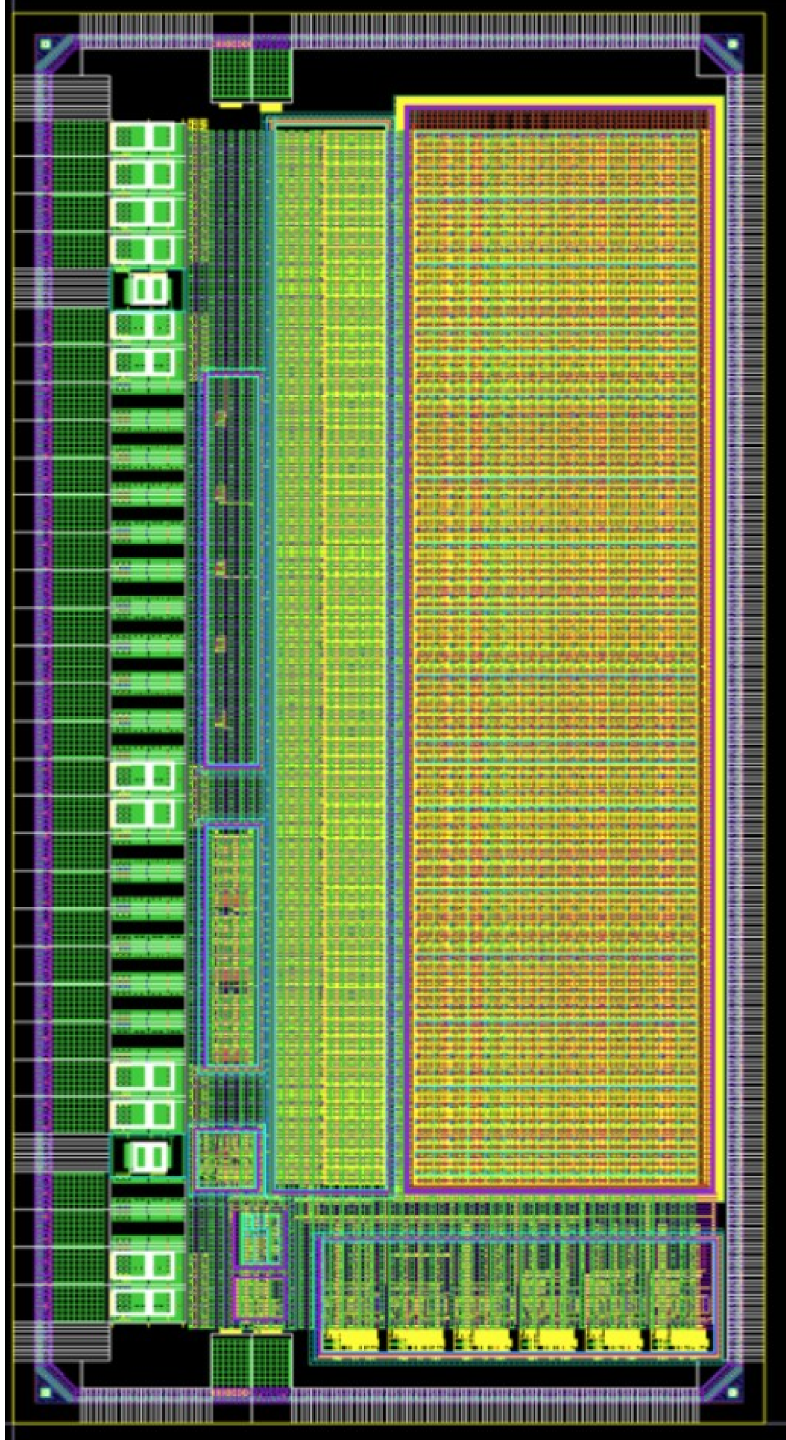
2nd DRD3 Week
CERN 05.12.24

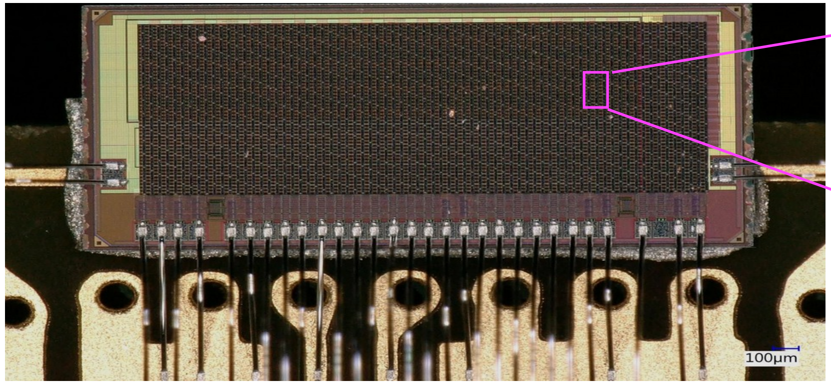


H2M (Hybrid-to-Monolithic)

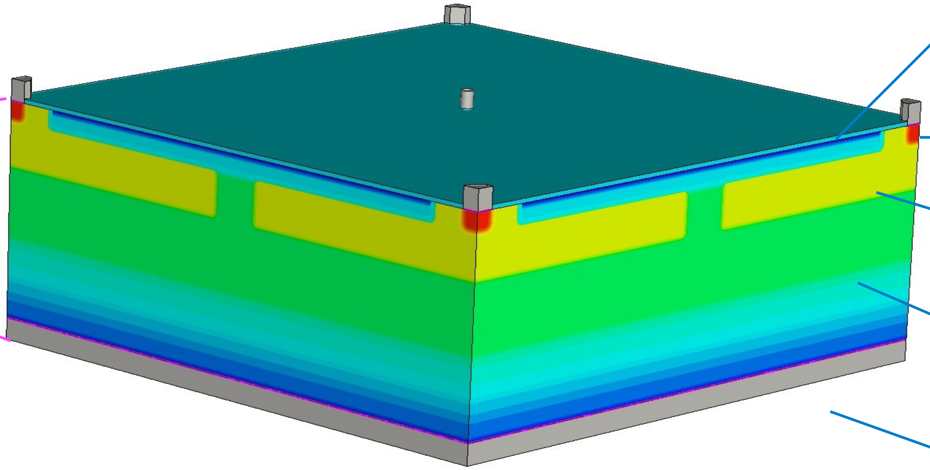
Vertex detector requirements:

- Sensor thickness: ⩽ 50 µm
- Spatial resolution: ⩽ 3 µm
- Time resolution: ~ ns

- **R&D chip for a vertex detector at a future lepton colliders or as an upgrade to beam telescopes**
- Ports a **hybrid pixel detector architecture into a monolithic chip**
- **Digital-on-top** design workflow
- Manufactured in a modified TPSCo **65 nm CMOS imaging process**

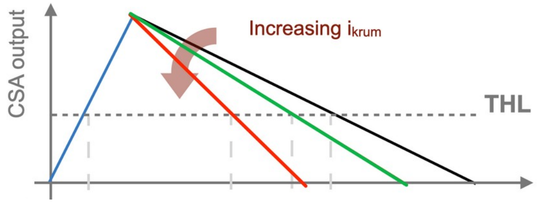


Active area outside of the chipboard to reduce material budget

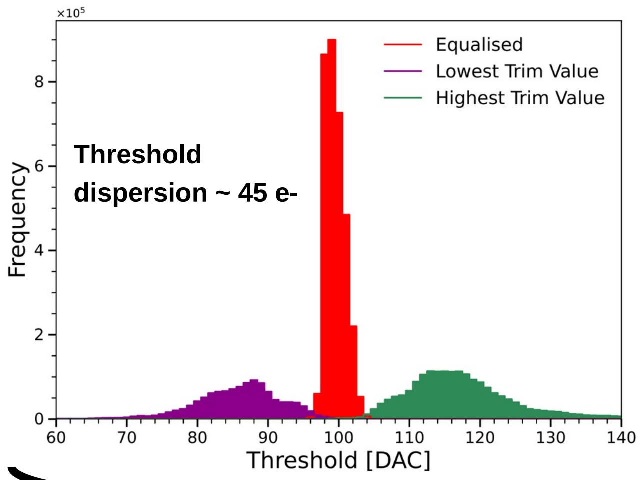


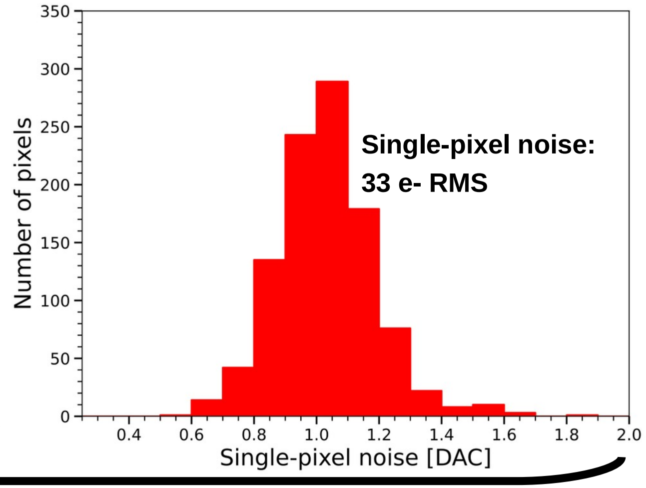
- **35 µm pixel pitch in 64x16 pixel matrix** (sensitive area: 2.24 × 0.56 mm^2). Thickness ~ 50 µm (p-epi ~ 10 µm)
- **Analog and digital front-end per pixel**

Analog front-end design



Constant slope of falling edge tuned with Krummenacher feedback current (ikrum)



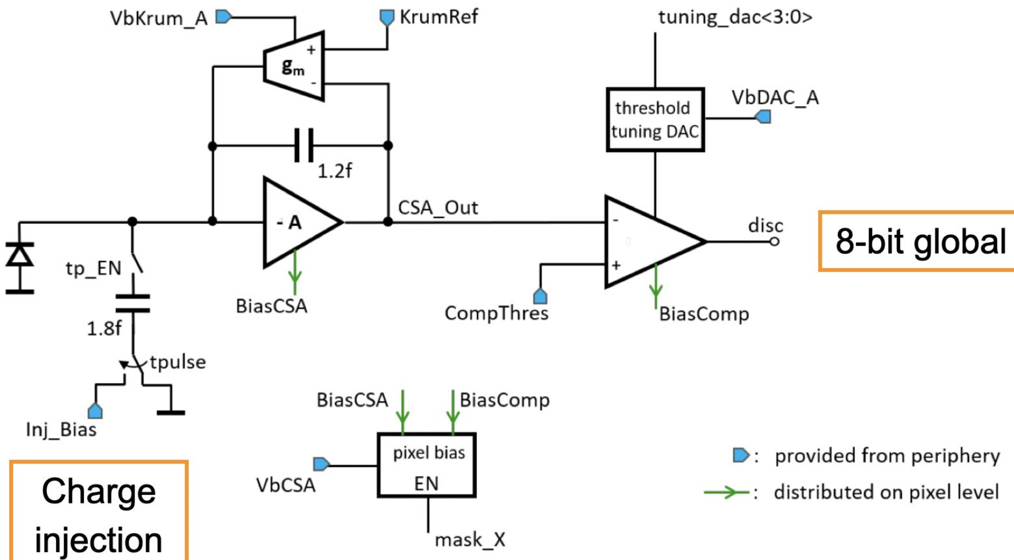


Charge sensitive amplifier with Krummenacher feedback

4-bit in-pixel trimming DAC → threshold mismatch compensation

Sensor diode

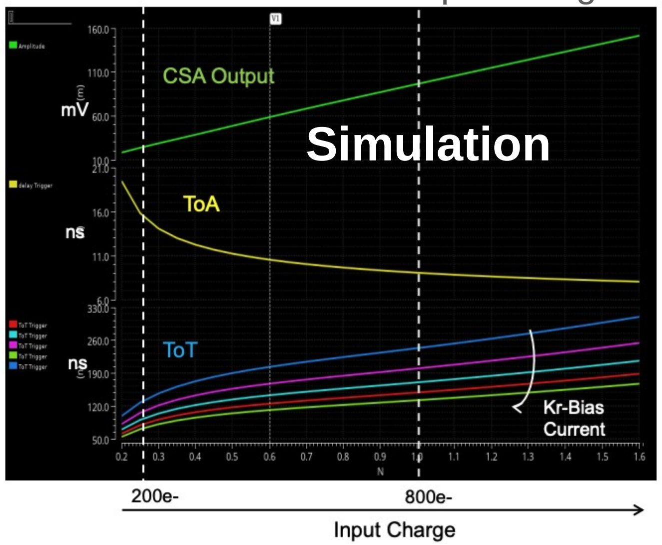
8-bit global threshold DAC



Charge injection

Pixel enable/ disable

ToA/ToT as function of input charge

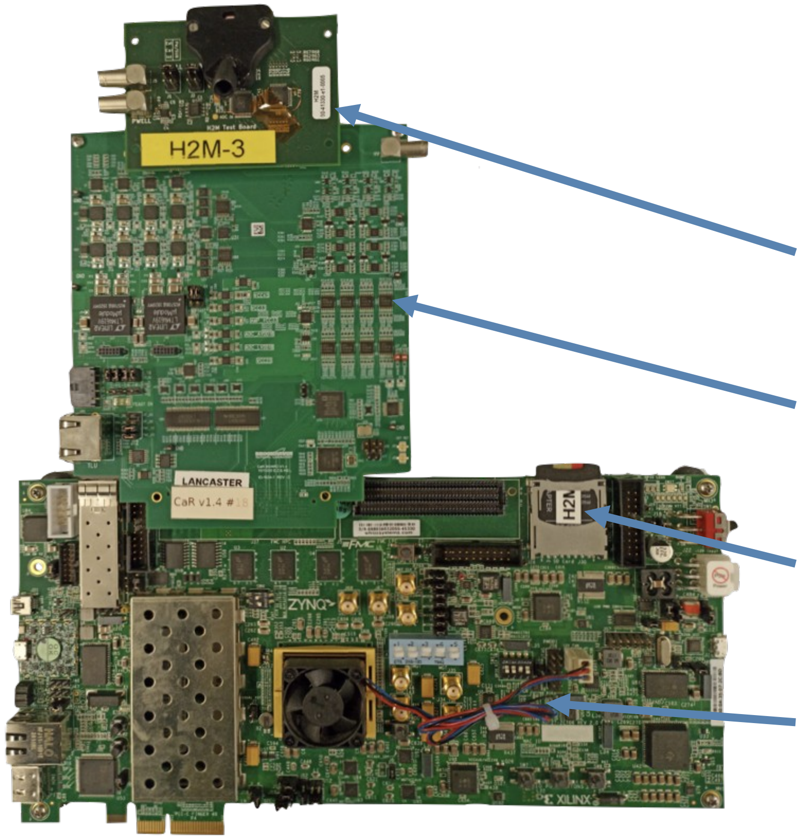


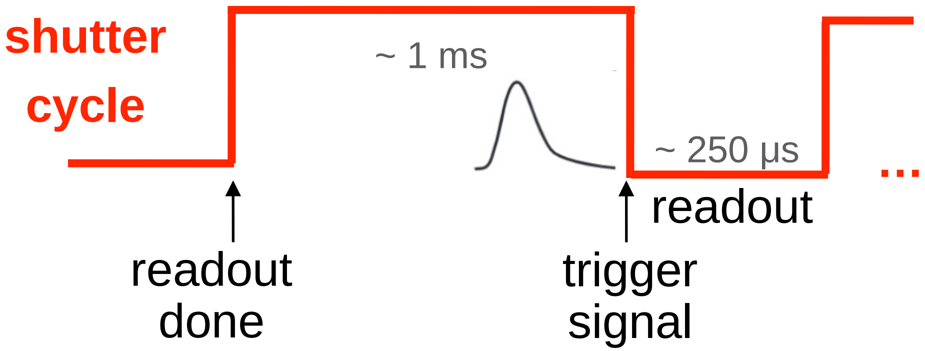
https://h2m-chip.docs.cern.ch/

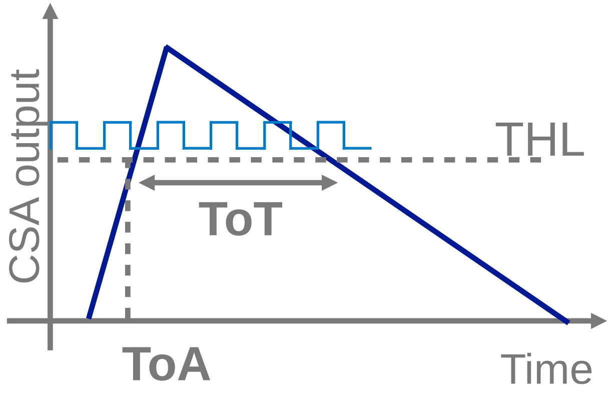
- **Time walk below 10 ns** for input charges larger than 400 electrons expected from **analog FE simulations**

Data acquisition

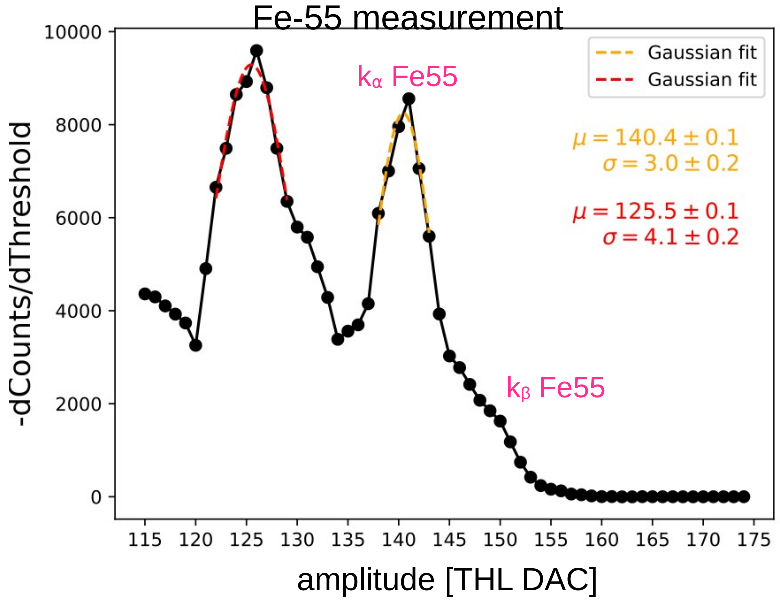
- The chip can operate in **4 acquisition modes**:
  - Shutter signal enables acquisition
    - Time over Threshold (ToT, 8 bit)
    - Time of Arrival (ToA, 8 bit, 10 ns binning)
    - Hit counting (number of hits above threshold)
  - Shutter signal validates hit
    - Triggered (8 bit counter accounts for delay)
- **Readout**: 40 MHz clock, frame based, no zero suppression
- Integrated into the Caribou DAQ system
  https://doi.org/10.22323/1.370.0100

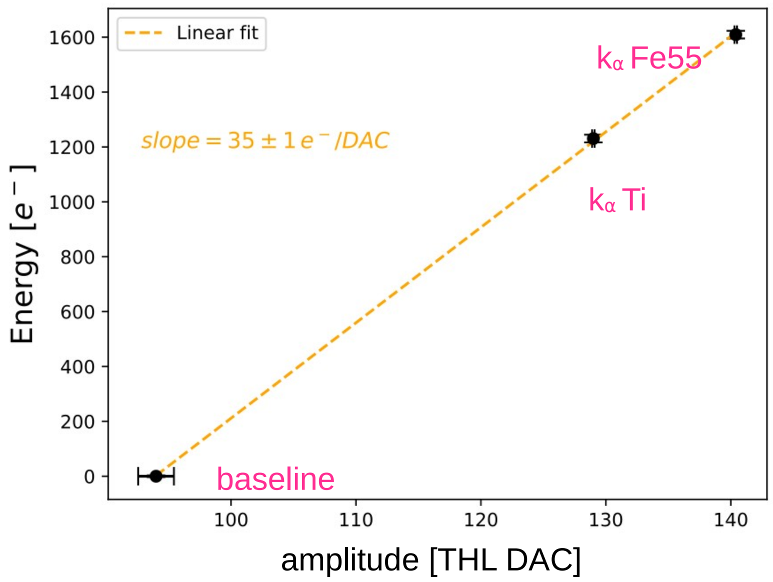


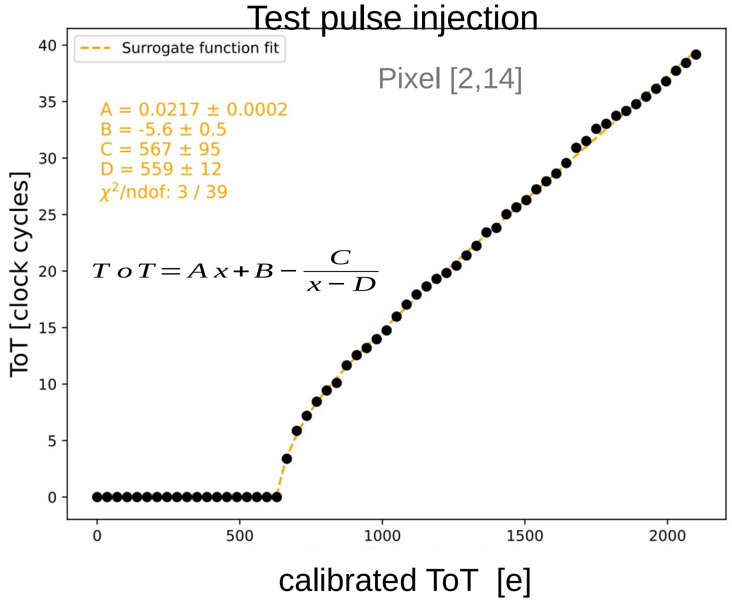




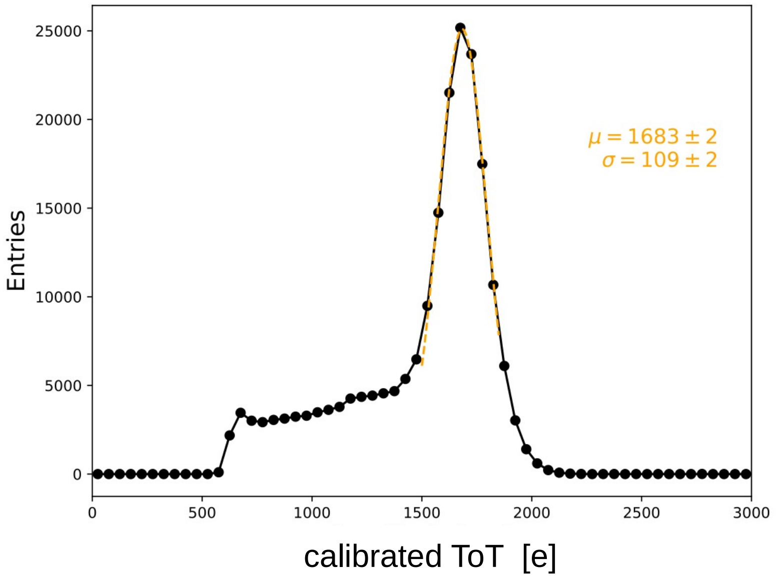
Threshold and ToT calibration



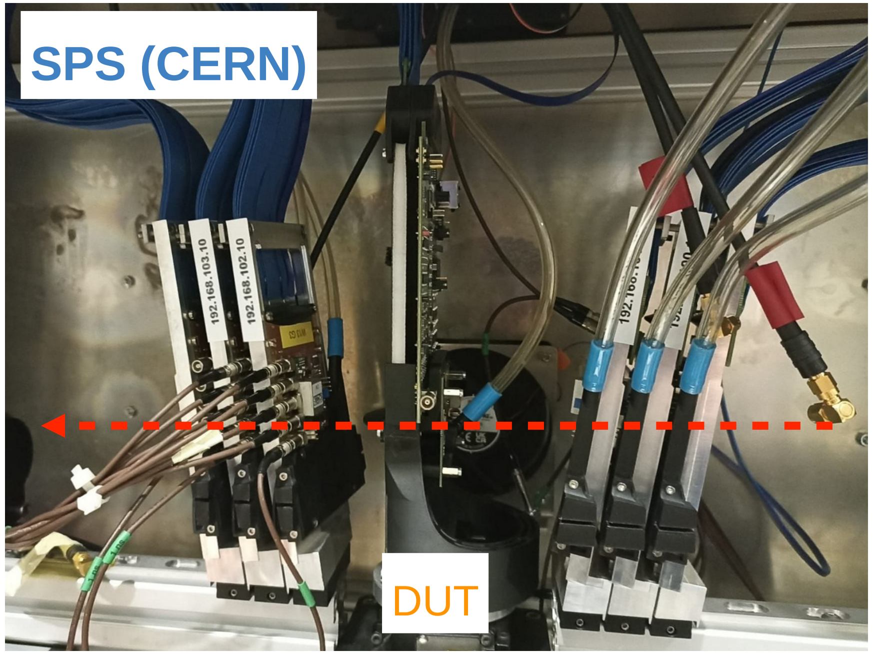




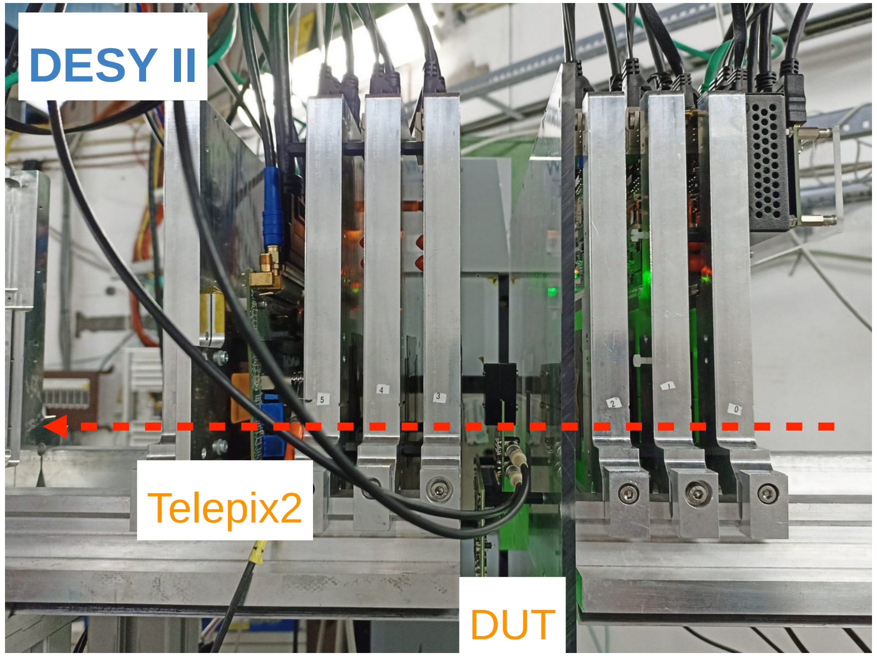
- **Threshold calibration** to find the relation between threshold-DAC and electrons for comparison with simulations using k_α of Fe-55 and Ti
- **Test pulse calibration** to find the relation between ToT and signal height per pixel
- Do Fe-55 measurement in ToT mode as Cross-check
  peak position agrees within 5%
- **Double peak in amplitude spectrum**:
  similar behavior observed in test chip; indicates ballistic deficit



Test-beam measurements at SPS and DESY II



- H6 beam line, 120 GeV charged pions.
- **Timepix3 reference telescope.**
  - Pointing resolution ~ 1.5 µm
- Continuous DUT readout with 150 us (2.56 us) shutter duration for ToT (ToA) mode.

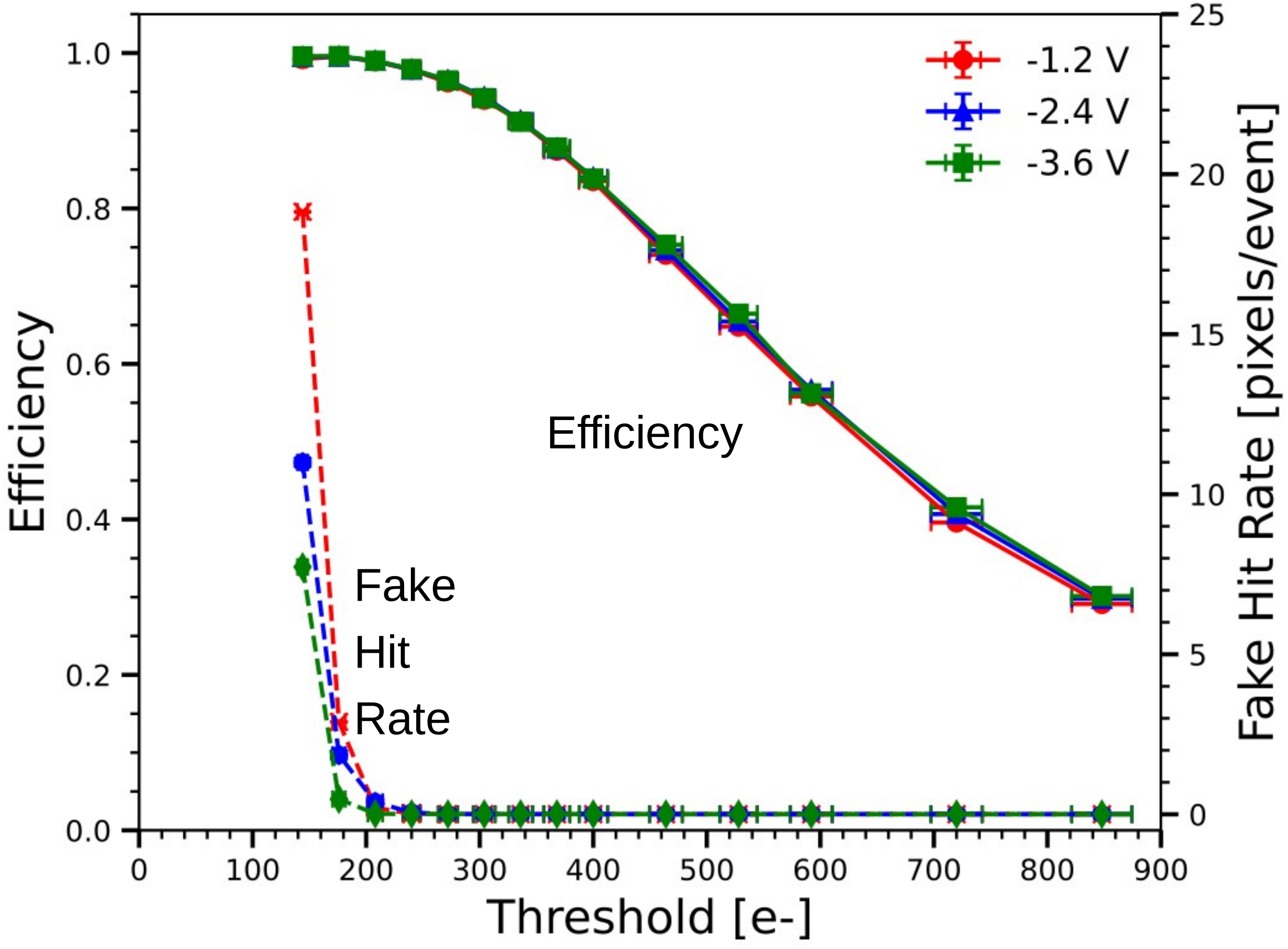


- Beamline 22, electron beam ~4.8 GeV.
- **ALPIDE reference telescope.**
  - Pointing resolution ~ 4 µm
- External rigger closes shutter; open for O(1 ms)
  - Using Telepix2* with configurable ROI
  - Time resolution < 4 ns

*presentation at PIXEL 2024

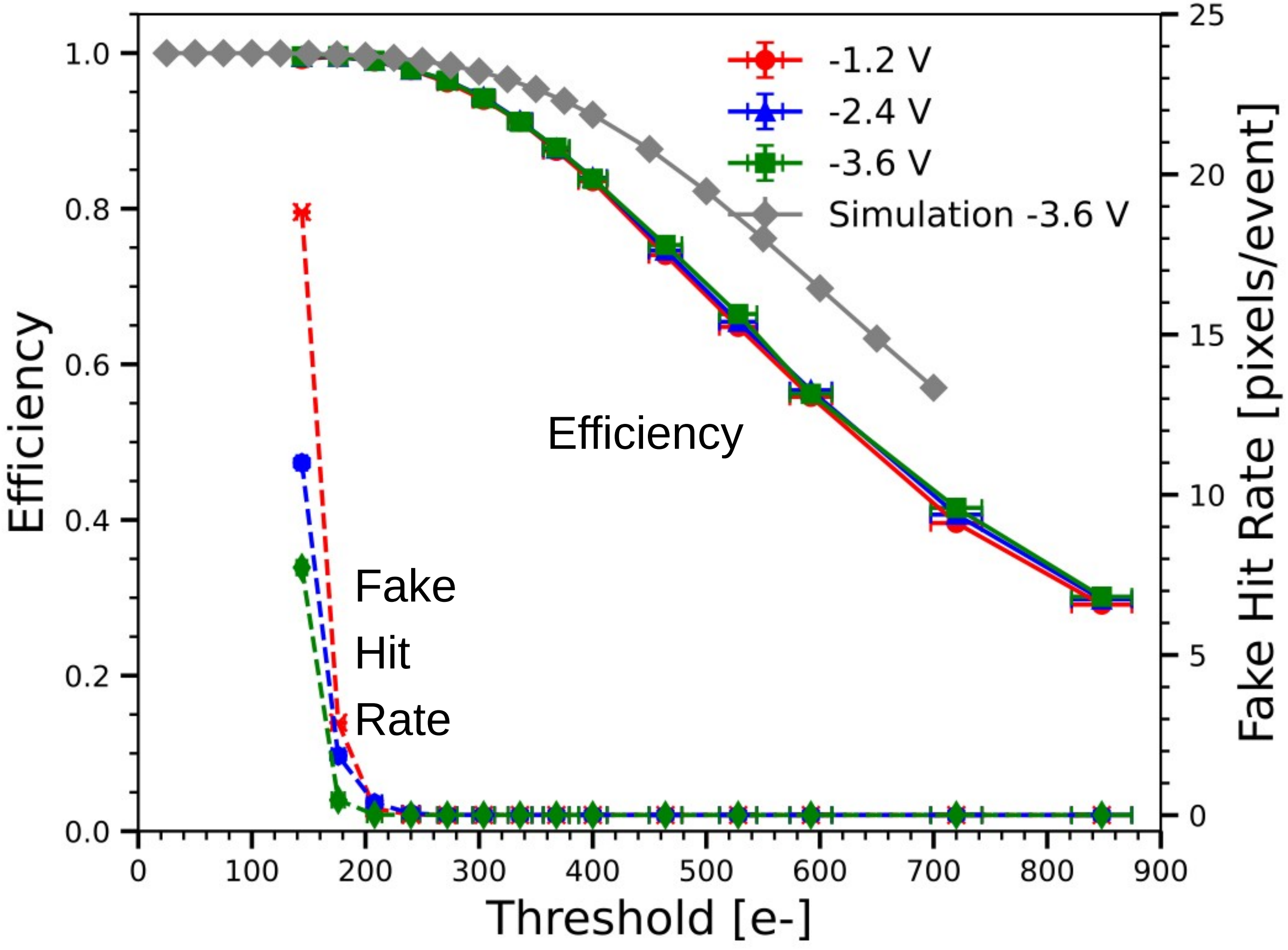
Use similar corryvreckan analysis configuration

Efficiency and fake hit rate (triggered mode)



- No significant differences between bias voltages
- For a fake hit rate < 10 pixels/event, **efficiency of 99.6%** at a threshold of 144 e- (~5σ_{noise}) and -3.6 V

Efficiency and fake hit rate (triggered mode)

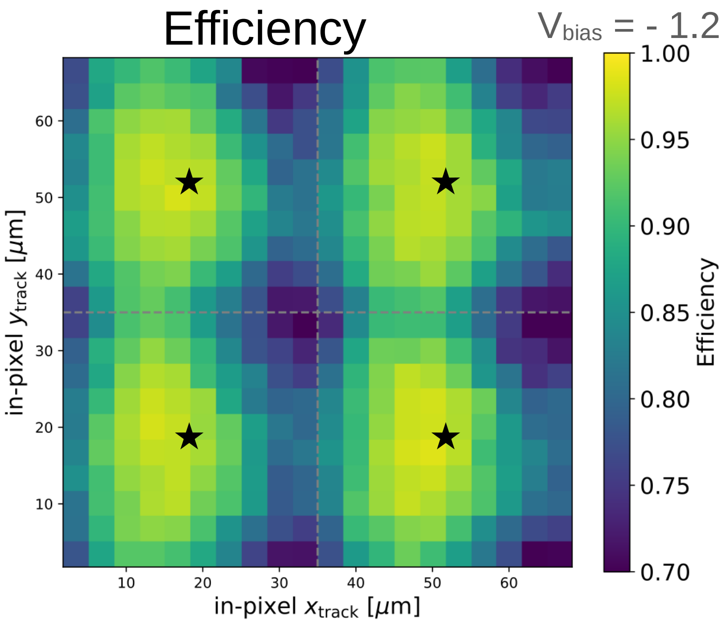


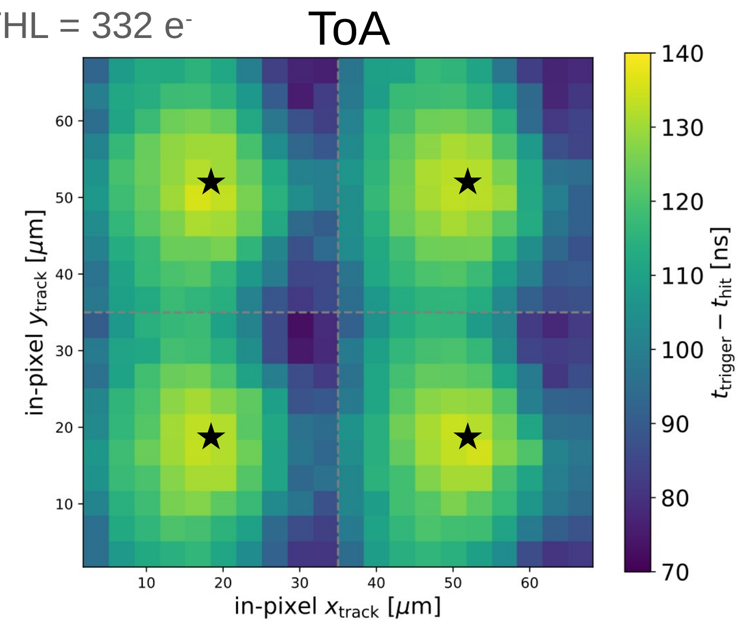
- No significant differences between bias voltages
- For a fake hit rate < 10 pixels/event, **efficiency of 99.6%** at a threshold of 144 e- (~5σ_{noise}) and -3.6 V
- However, **lower efficiency was measured than expected from simulations** (using generic methods without proprietary information, and simulating the deep p-wells as flat profiles/nothing within the deep p-wells https://arxiv.org/abs/2408.00027)

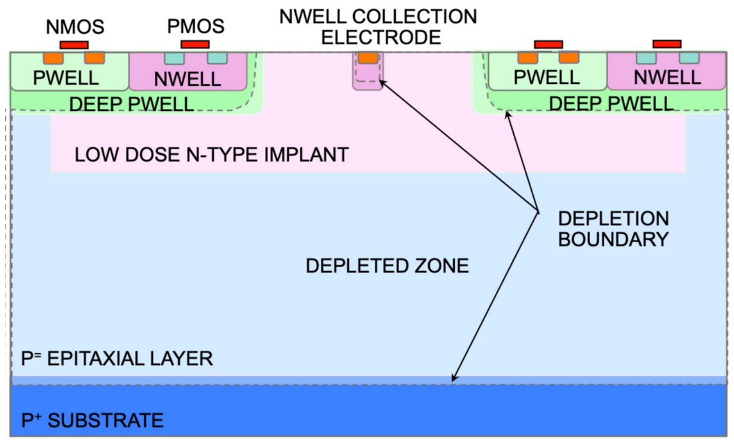
Non-uniformity in-pixel response

★ Collection electrode

V_{bias} = - 1.2 V, ikrum = 21, THL = 332 e^-







W. Snoeys, DOI:10.1016/j.nima.2017.07.046

Non-uniformity in-pixel response

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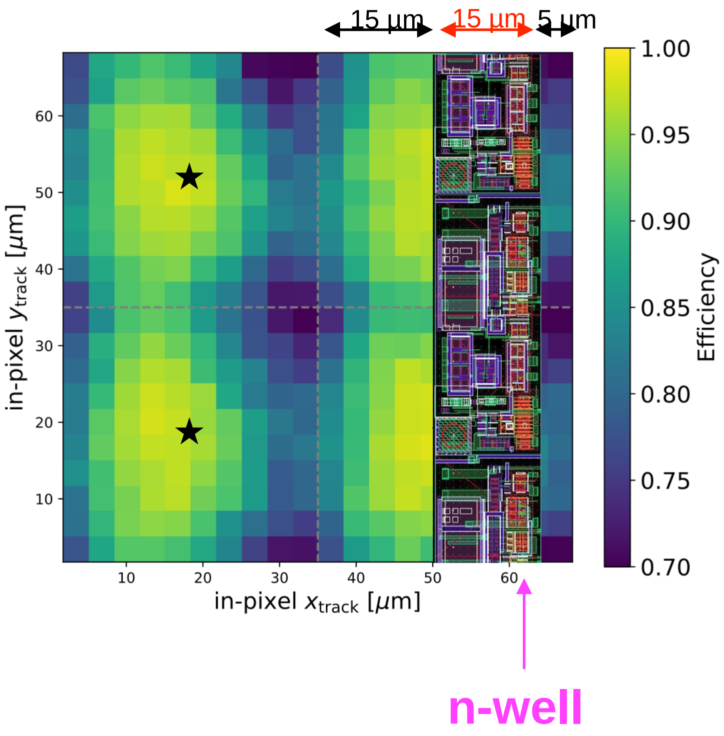
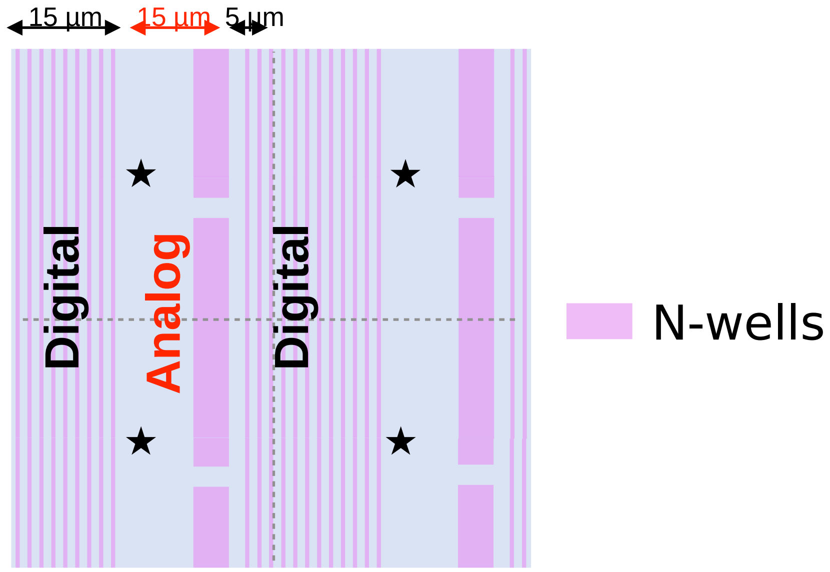
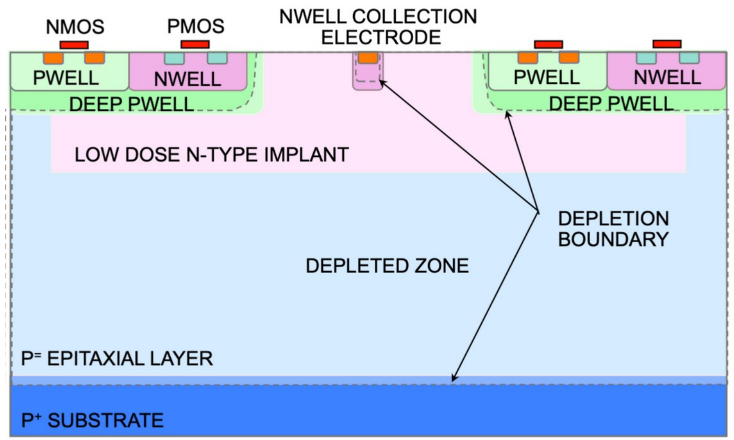




- Related to the **size and location of the n-wells** of the analog circuitry.



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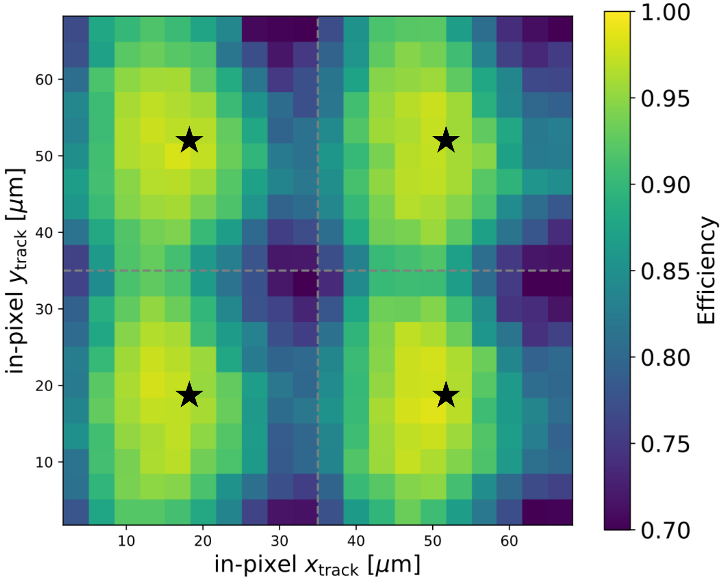
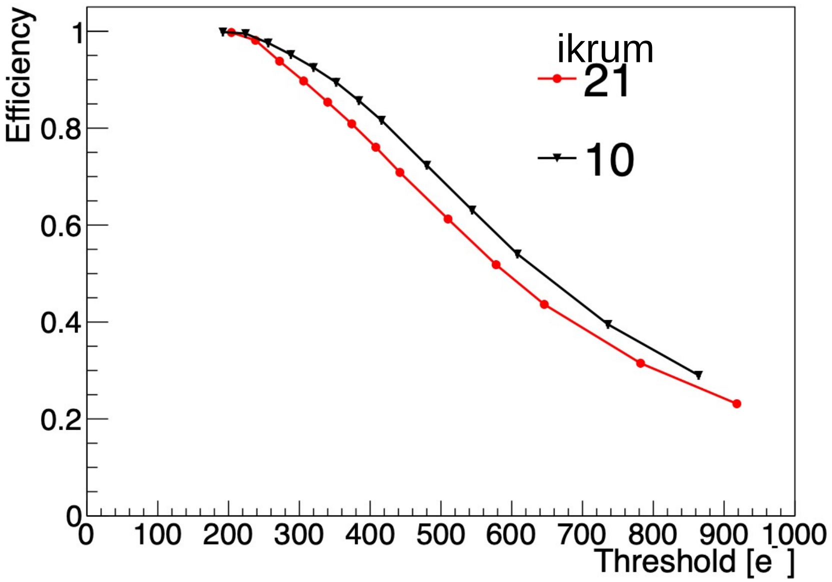
Non-uniformity in-pixel response – Mitigation

★ Collection electrode

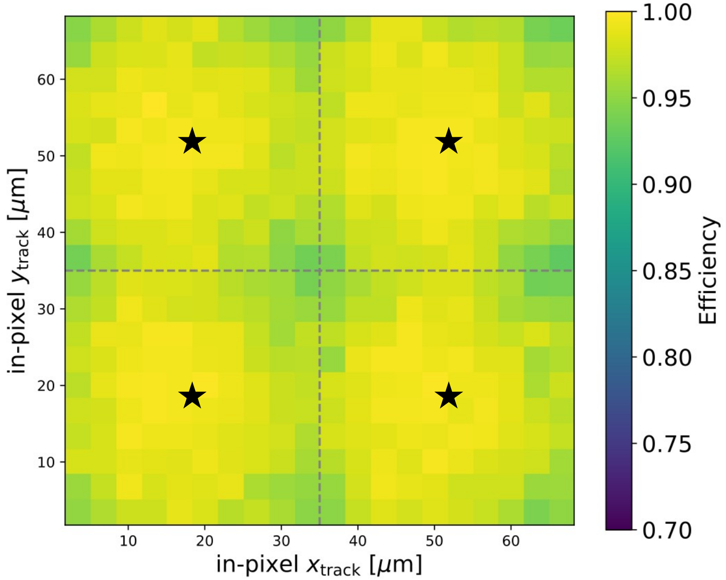
V_{bias} = - 1.2 V, ikrum = 21, THL = 332 e$^-$



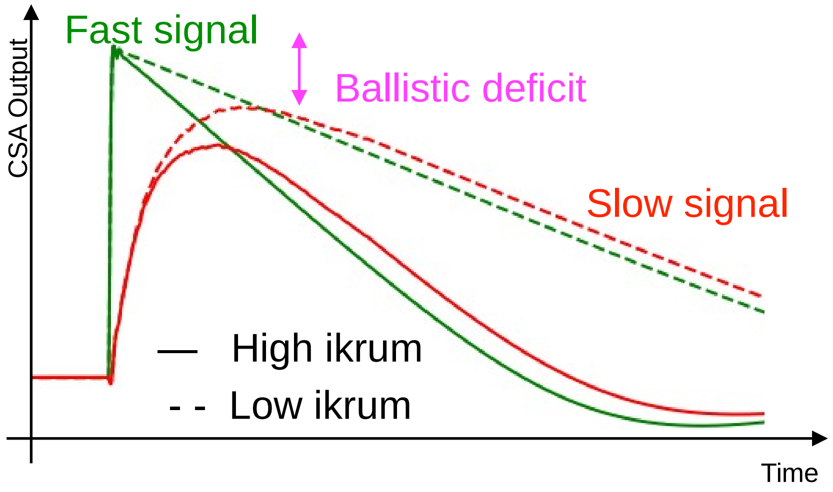
V_{bias} = - 1.2 V



V_{bias} = - 3.6 V, ikrum = 10, THL = 240 e$^-$



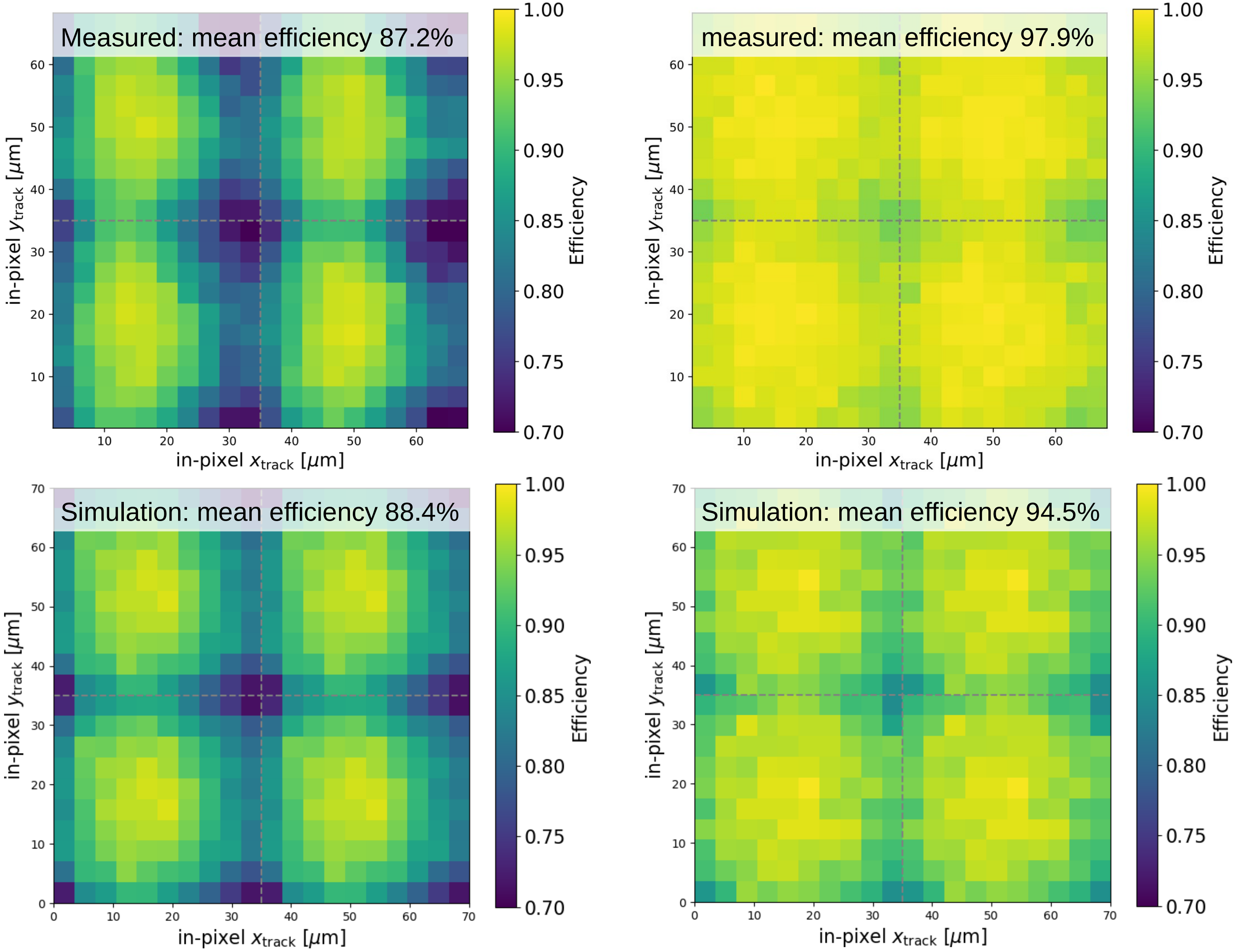
- Related to the size and location of the n-wells of the analog circuitry
- Mitigated at **lower ikrum**, **higher bias voltages**, and **lower threshold**
  - Collection speed influences the amplitude due to ballistic deficit
- Additionally, effects of fast front-end and large pixel size
- Qualitatively confirmed by **simulations with real profiles**



Non-uniformity in-pixel response – Simulation

V_{bias} = - 1.2 V, ikrum = 21, THL = 332 e^-

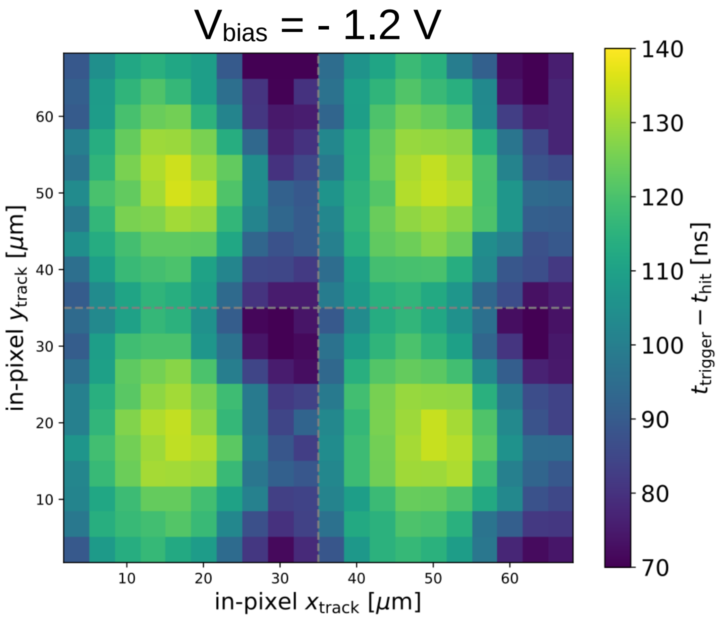
V_{bias} = - 3.6 V, ikrum = 10, THL = 240 e^-

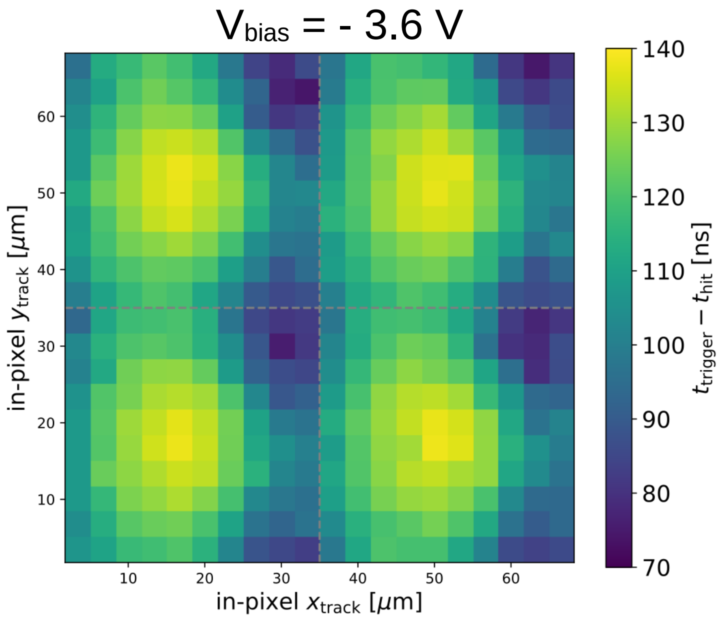


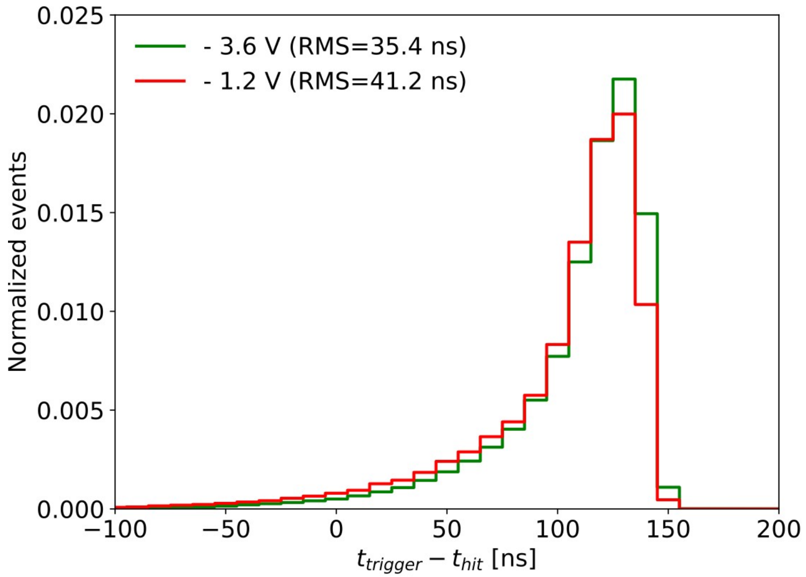
- Simulation procedure:
  - Electric fields: TCAD (Sentaurus) simulation with realistic doping profiles
  - Transients: Allpix-Squared Charge deposition and transport
  - Front-end response: Spectre
  - All of these steps are crucial
- Adding electronics noise and track resolution effects
- Good agreement
  - Only few percent difference
  - Similar shape (simulation tends to be more symmetric)

Time resolution (ToA)

ikrum = 10, THL = 304 e^-

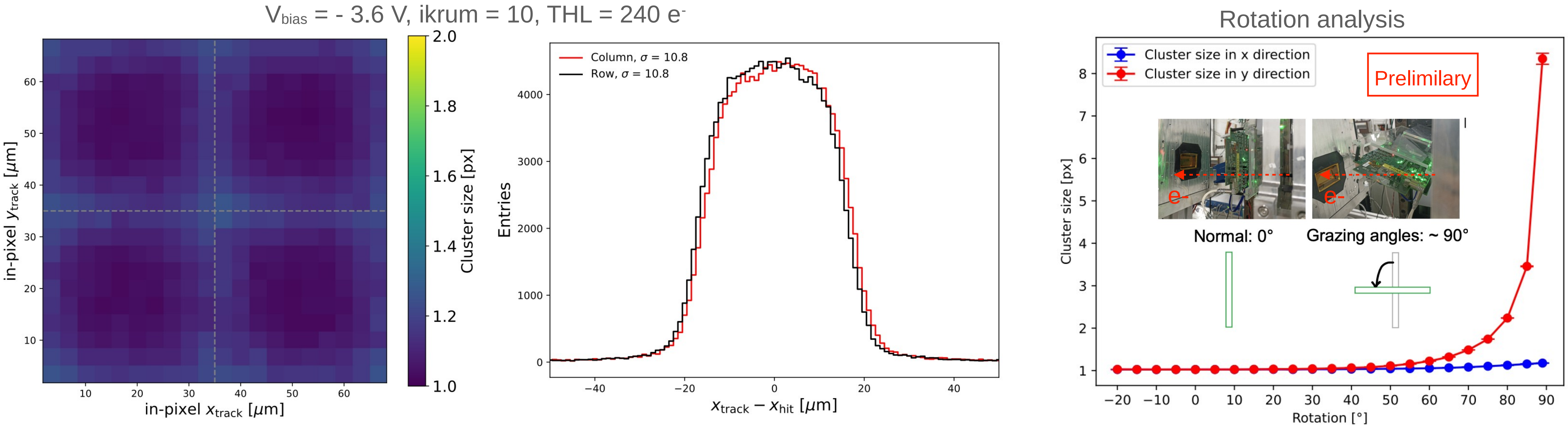






- Arrival time depends on track impact position→**timing limited by non-uniformity of charge collection**
- **Better timing resolution for -3.6 V than -1.2 V** due to more uniform charge-collection time across the pixel
- **No possibility of time-walk correction** since charge information is not available simultaneously

Cluster size and spatial resolution (ToT)



Spatial resolution in X (same in Y) $\sqrt{(10.8^2 - 3.8^2)}$ = 10.1 μm (~35/√12 μm) and **cluster size** ~ 1

- Dominated by the large pitch of 35 μm, even at low threshold
- Asymmetric residuals in the row direction due to the low-efficiency part

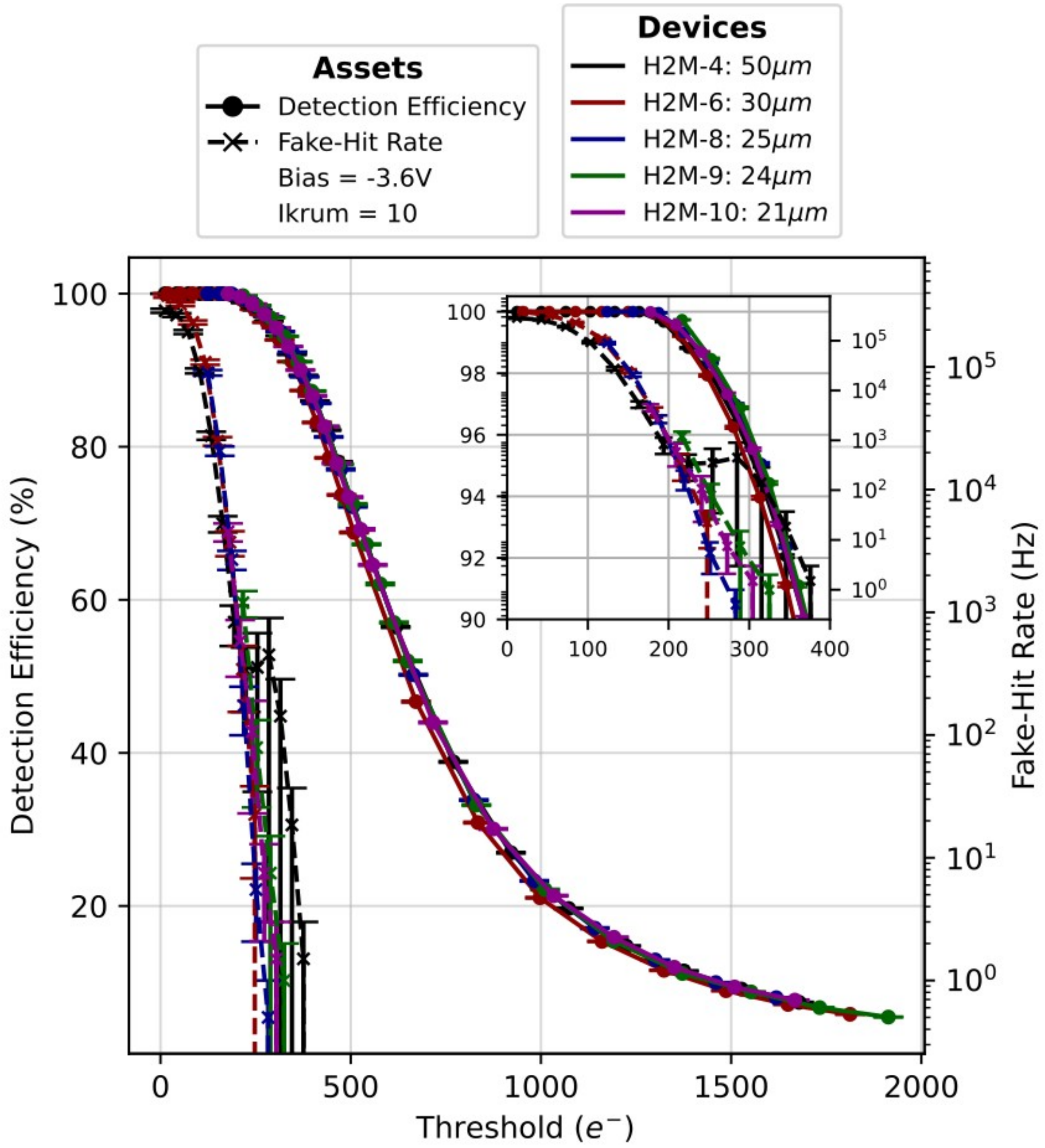
- Analysis of rotation data ongoing (grazing-angle study) → **extract active thickness**

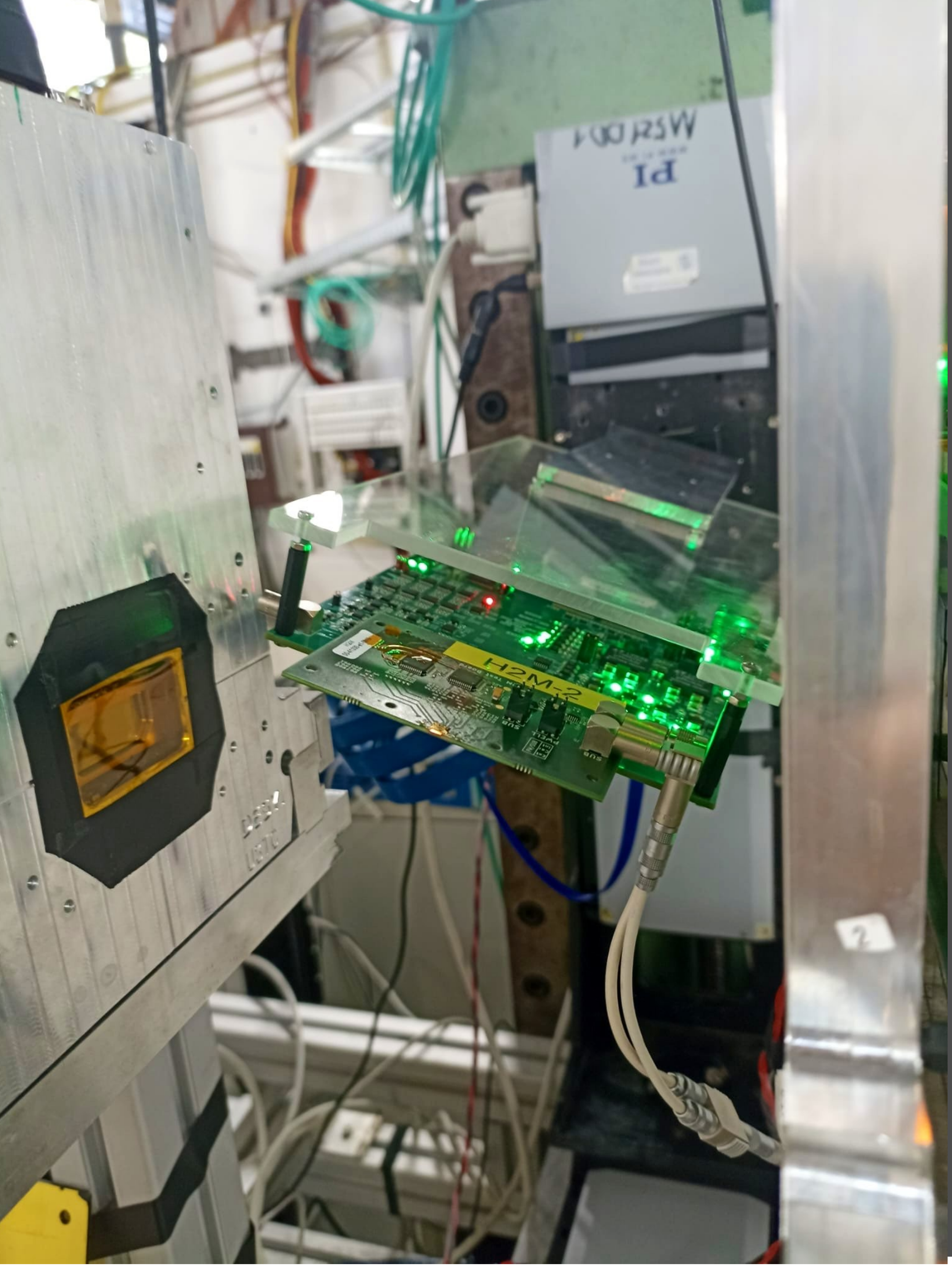
Thin samples (ToT mode)

- **Single-die backside thinning** of H2M samples, performed by [OPTIM WS]
  - 30, 25, 24, 21 µm physical thickness

- **No performance degradation from thinning**
  - Efficiency >99% for ~200 e- threshold

- Studying thinning down to below 20 microns
  - Includes ~5 µm circuitry + ~10 µm epitaxial layer





Summary

- **Fully functional monolithic sensor in a 65 nm CIS designed in digital-on-top workflow**
- **Calibration and characterization** of performance with **laboratory** and **test beam** measurements
  - Efficiency 99.6% at a threshold of 144 e- (~$5\sigma_{noise}$)
  - Spatial resolution 10.1 µm (expected from pitch)
  - Thinning down to 21 µm without performance loss
- **Impact of n-wells on charge-collection**
  - Non-uniform in-pixel response affects timing
  - And efficiency for high thresholds and ikrum
  - Reproduced in simulations

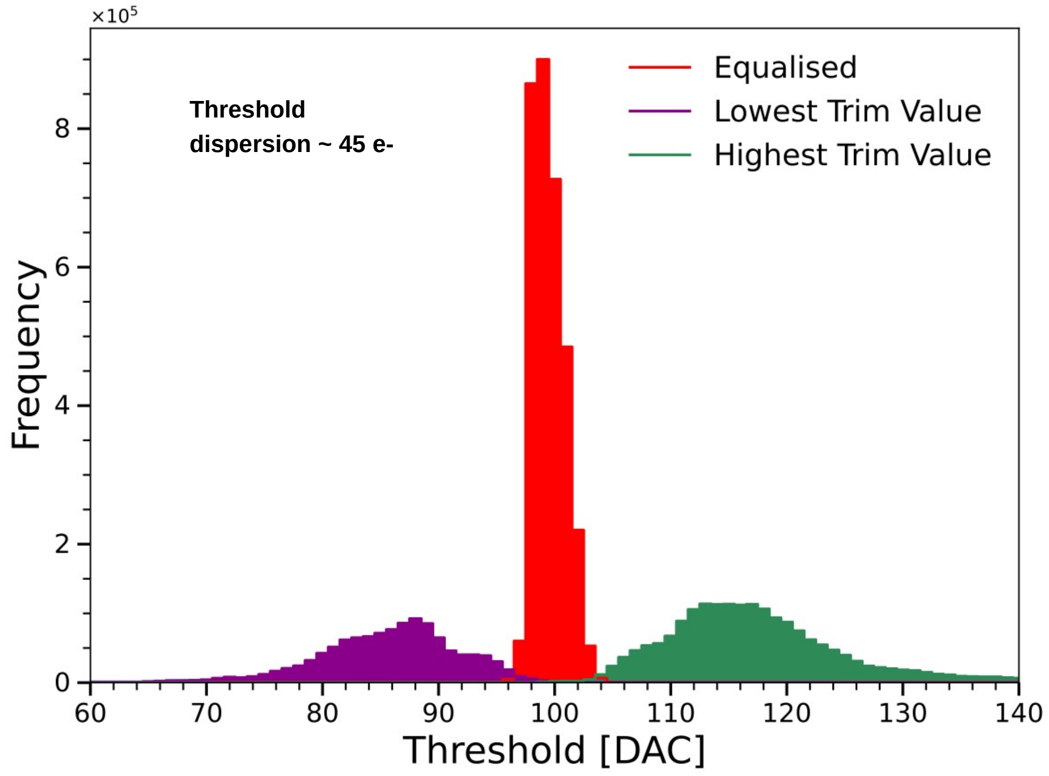
Outlook

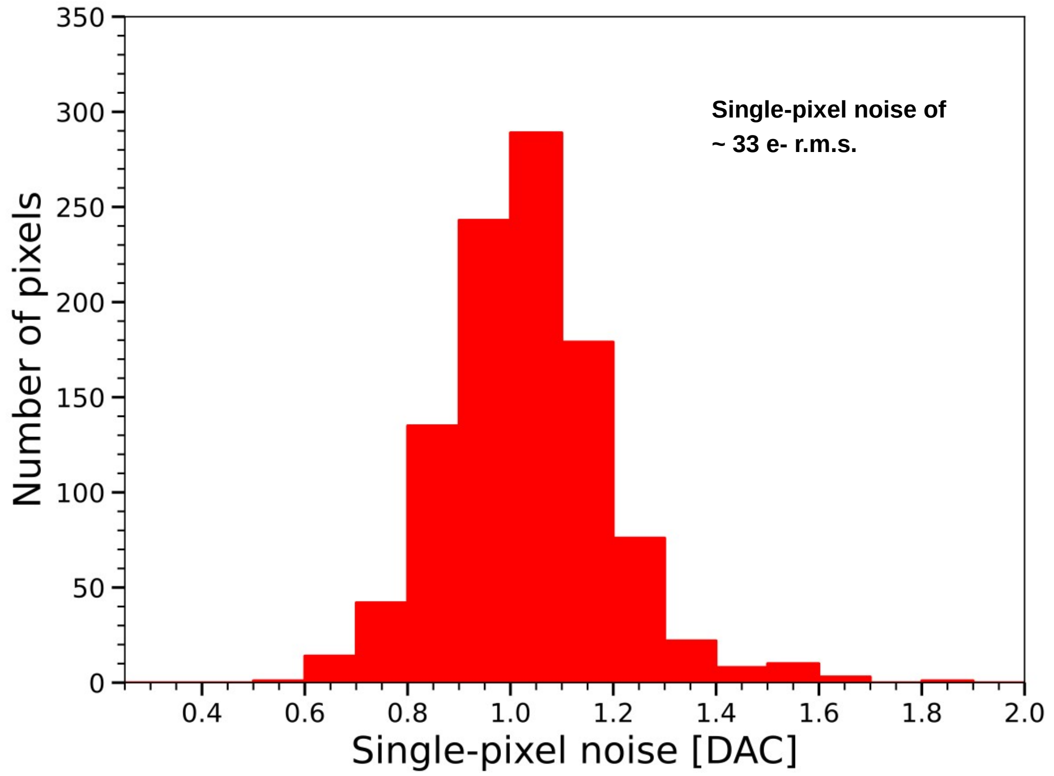
- Analysis of rotation data (**grazing-angle study**)
- Investigating **thinning** the chips to a total thickness **< 20 µm**
- PIXEL proceedings [Sara Ruiz Daza] and [Corentin Lemoine]

Thank you!

"The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)".

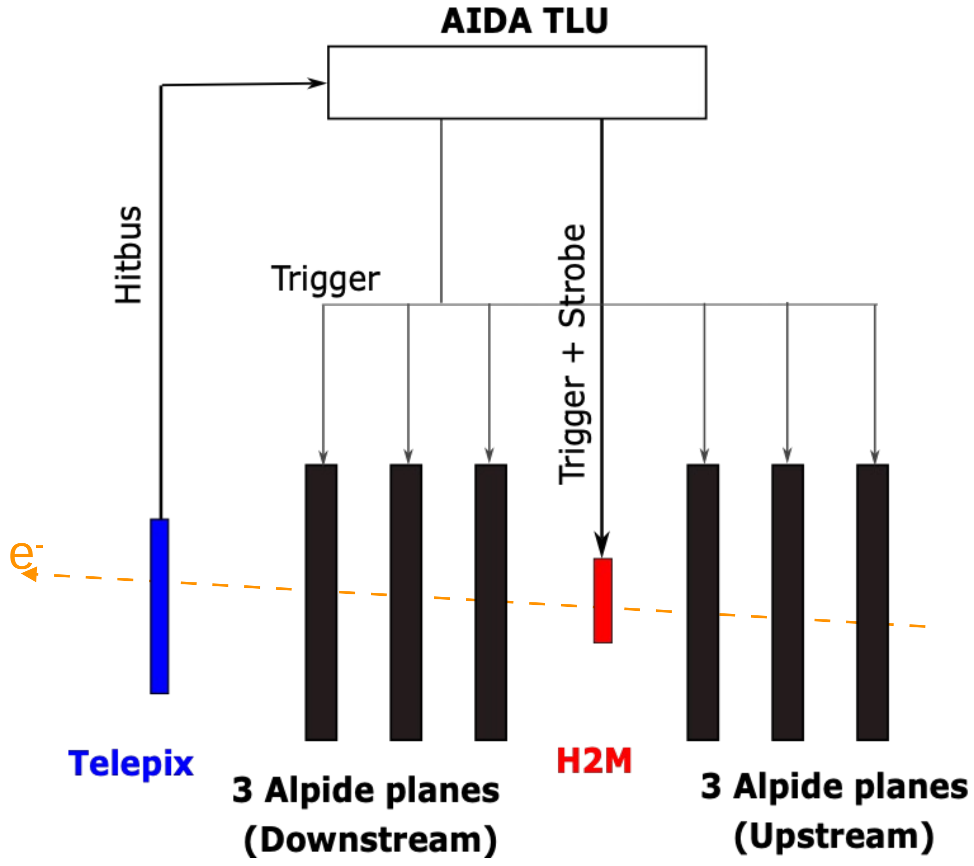
Threshold equalization and single-pixel noise

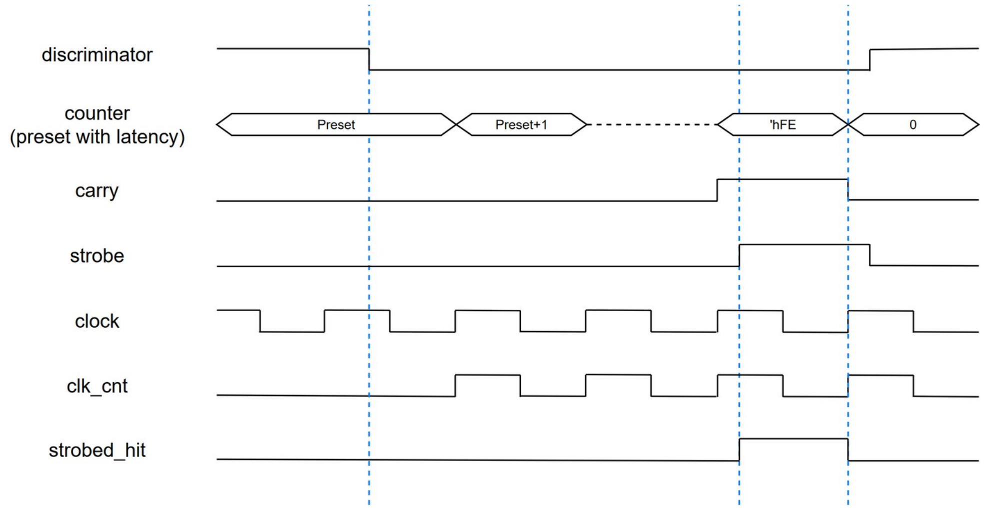




- Equalization of the hit detection threshold:
  1) Threshold scan in counting mode for the 16 trimming values
  2) Determine the baseline for each pixel for each trimming value
  3) For each pixel, the trimming DAC is adjusted to the one that makes the closest to a fixed trimming target.
- **Single pixel-noise** obtained from width of threshold turn-on curves.

Triggered mode





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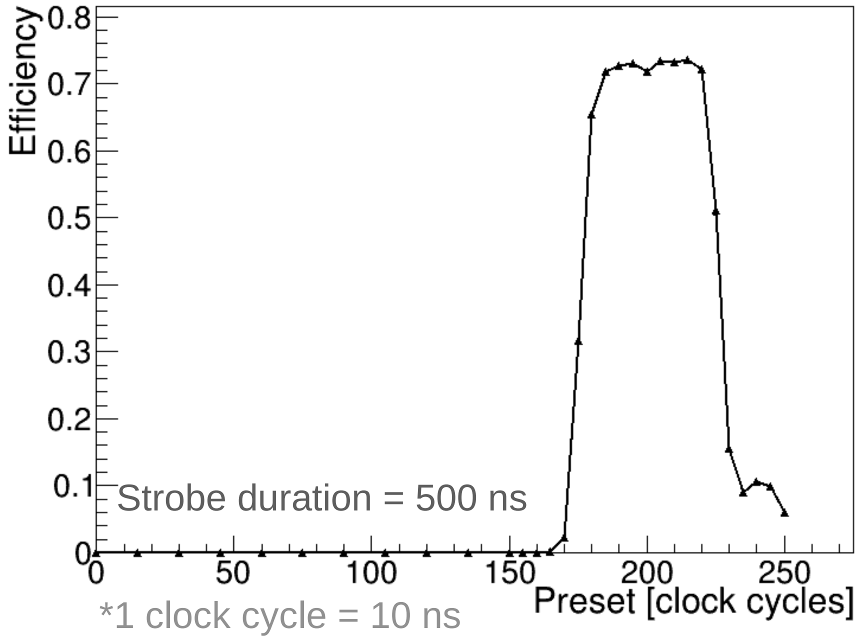
- **Strobe window duration** accounts for time walk (~ 100 ns).
- **Preset** value accounts for the trigger latency.

Shutter (strobe signal) open for 500 ns vs O(ms) in ToT/ToA

➔ Efficiency compatible with the other acquisition modes

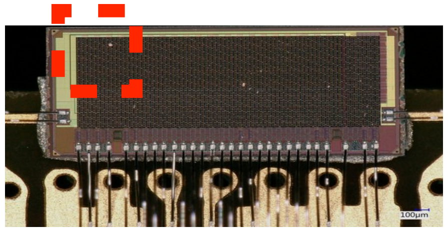
➔ Fake rate reduced by a factor of about 100

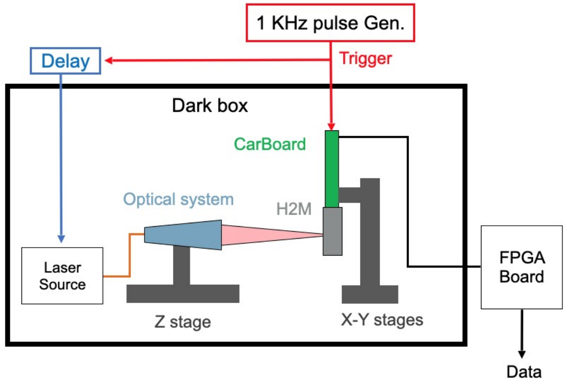
➔ Minimum threshold achievable ~ 144 electrons



*1 clock cycle = 10 ns

Measurements with a laser setup

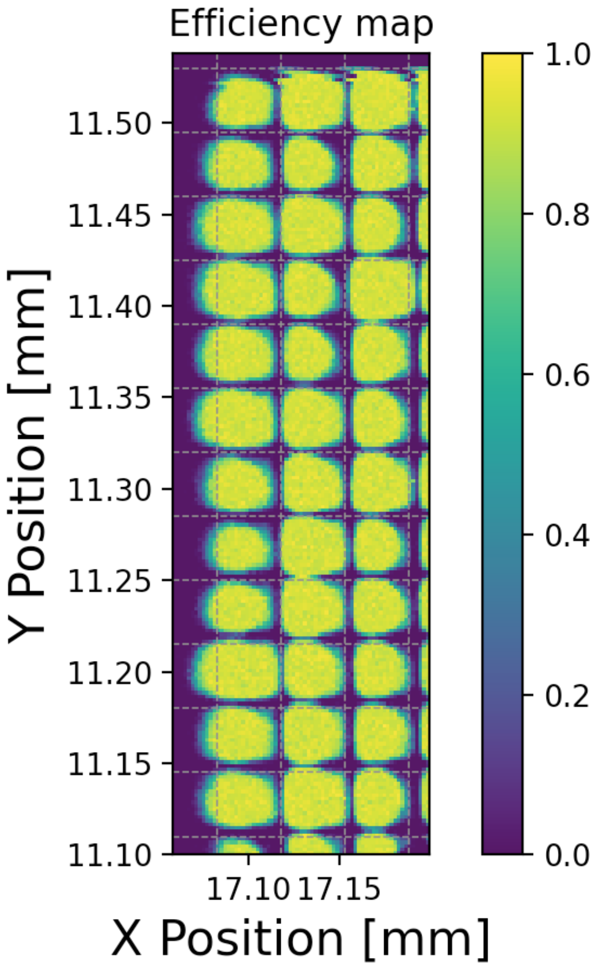


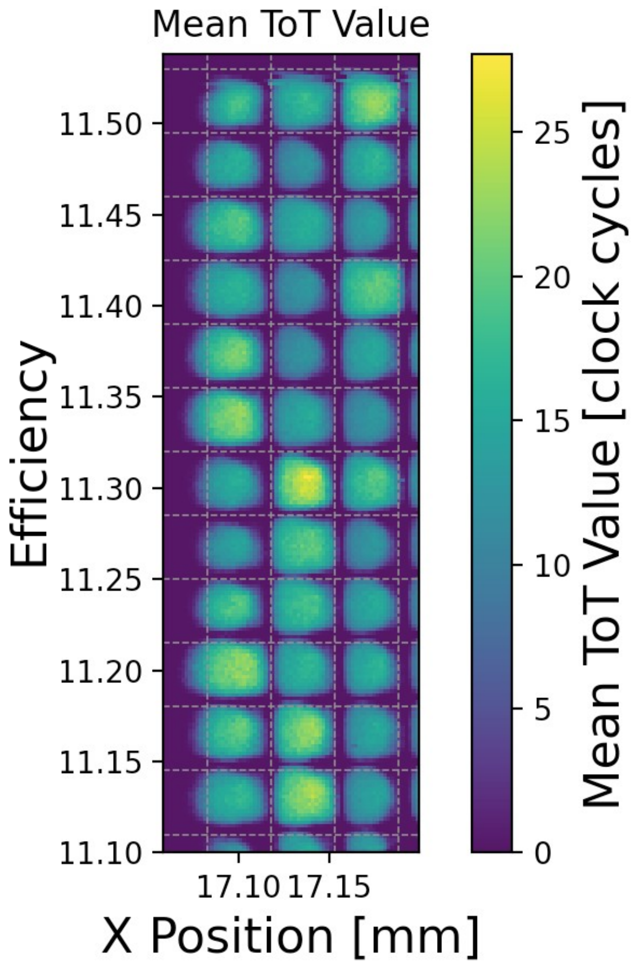


- Backside incidence with an **infrared pulsed laser**. Light intensity tuned to correspond to the ToT MPV signal of 1 MIP.

- Confirmation of the **in-pixel efficiency pattern** observed in the test beam measurements and its orientation.

- **Pixel-to-pixel differences** attributed to different returns to baseline due to differences in the circuit's Krummenacher current and feedback capacitance.



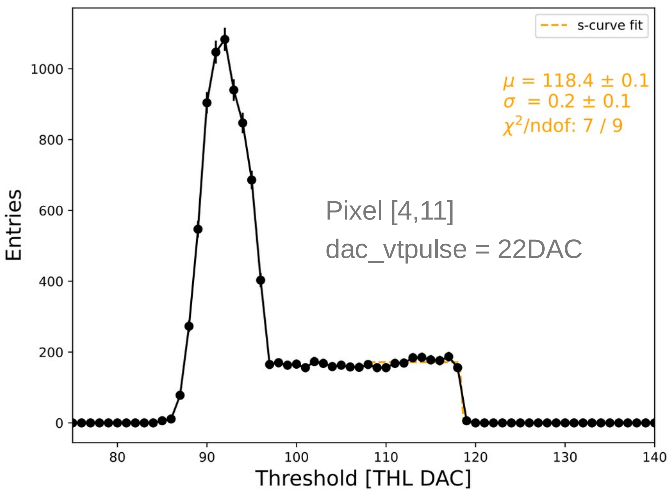


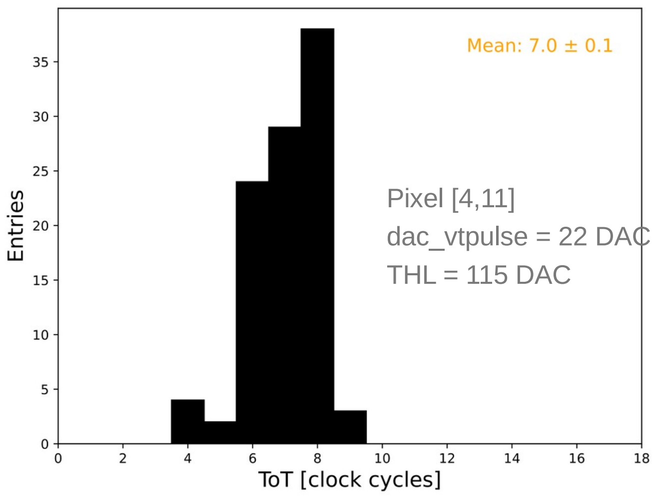
*1 clock cycle = 10 ns

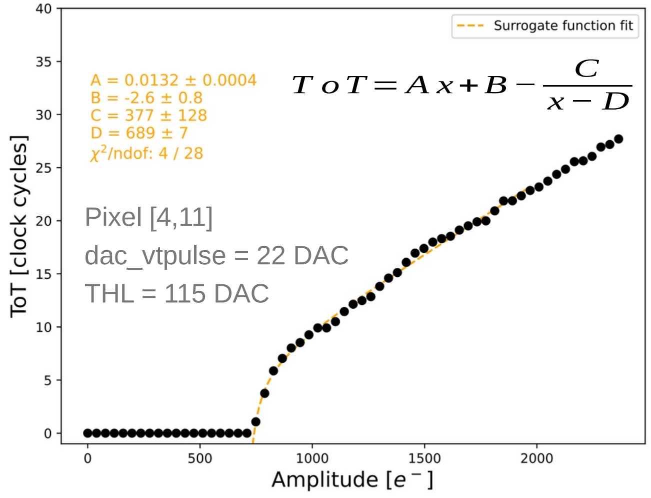
ToT calibration

1.Amplitude vs dac_vtpulse + 2.ToT vs dac_vtpulse => 3.ToT vs amplitude

One pixel







All pixels