Development of MAPS using 55nm HVCMOS process for future tracking detectors

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On behalf of COFFEE team

2nd DRD3 week on Solid State Detectors R&D

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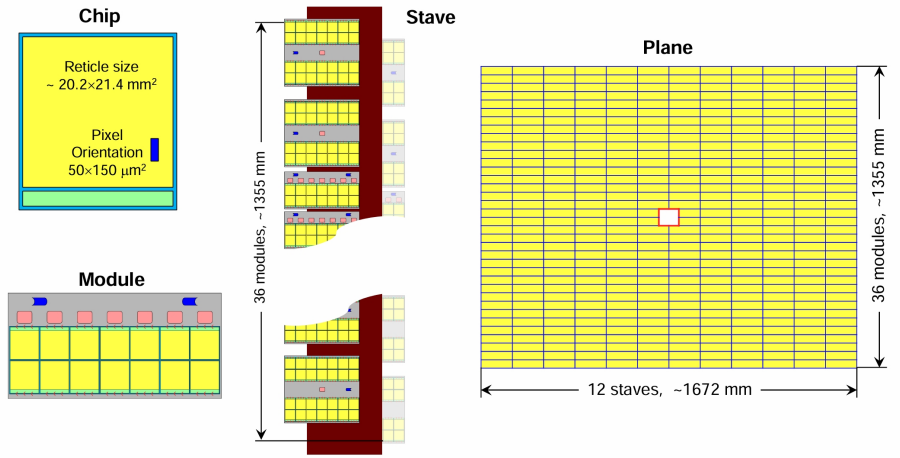
Motivation

- LHCb Upgrade2 requires tracker with finer granularity and better radiation-hardness
- Future Higgs factory, CEPC, plans to utilize large-area silicon-based tracker

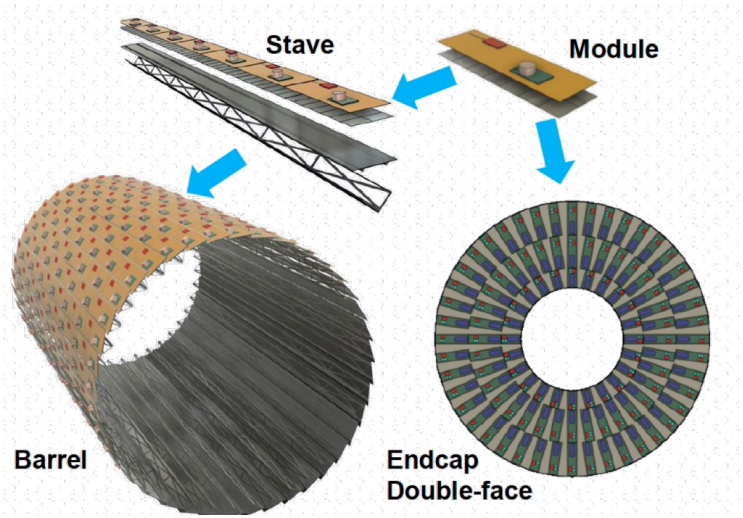


Upstream Tracker@ LHCb U2 FTDR

area $\sim 8\mathrm{m}^2$

radiation hardness $\sim 3 \times 10^{15}\mathrm{n_{eq}/cm^2}$

timing $\sim$ ns to tag 25 ns bunches



CEPC Inner Tracker

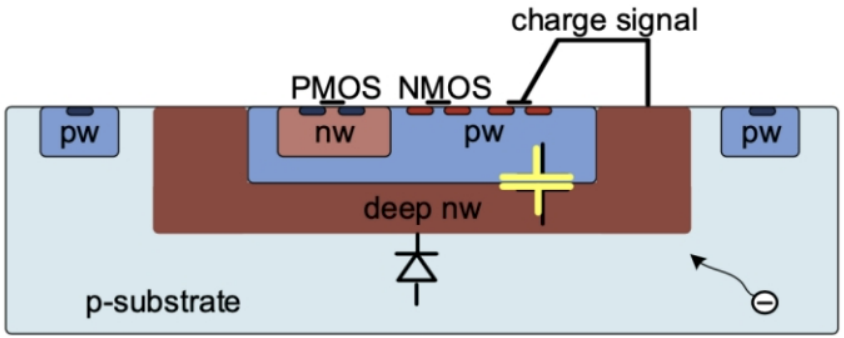
area $\sim 15\mathrm{m}^2$

spatial resolution$< 10\mu\mathrm{m}$

timing $\sim$ ns to tag 23 ns bunches

HVCMOS as Possible Solution

Needs	Radiation hardness	Resolution	Timing	Power consumption
	$3 \times 10^{15} \mathrm{n_{eq}/cm^2}$	$10 \mu\mathrm{m}$	3-5ns	$200\ \mathrm{mW/cm^2}$



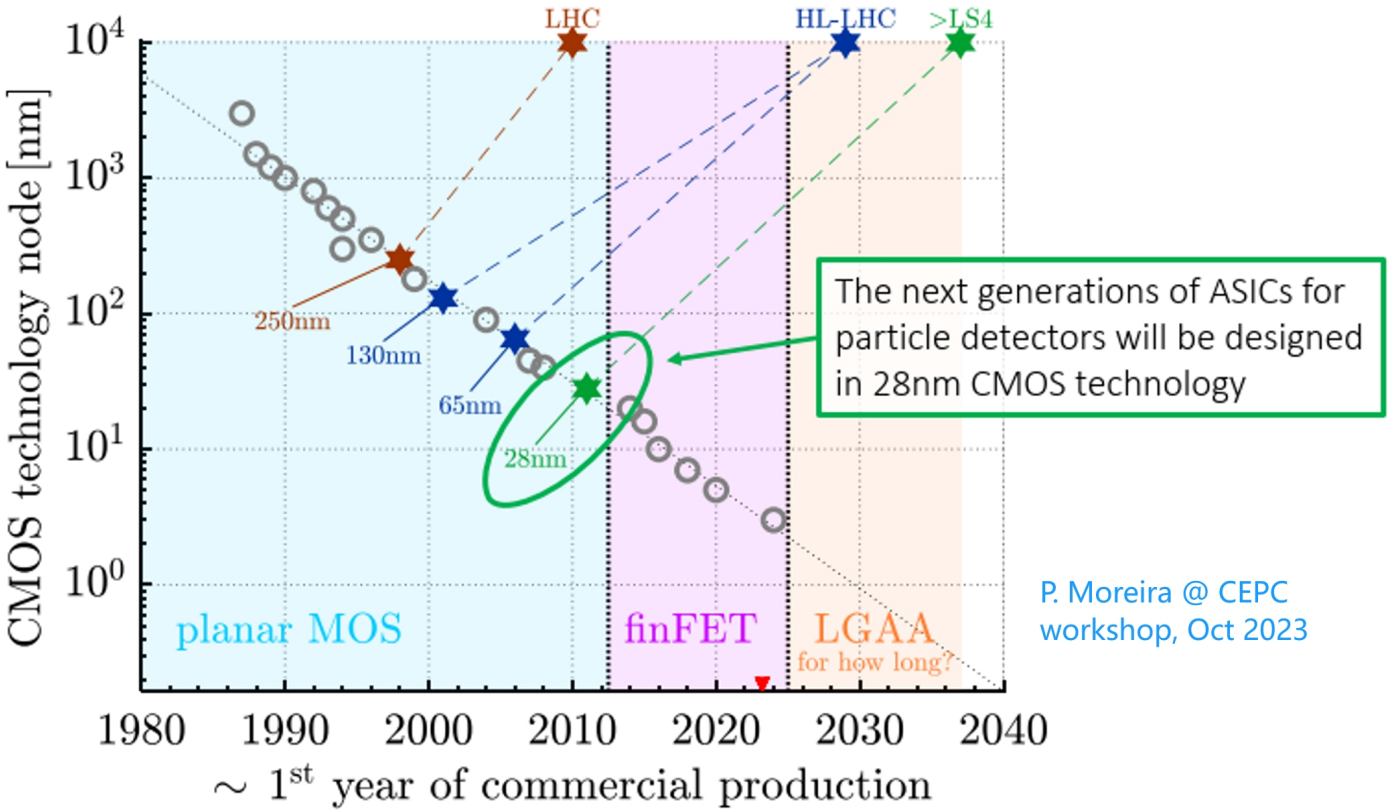
Large collection electrode

HVCMOS characteristics:

- Front-end circuit inside the charge collection well
- Large depletion depth and electric field
- On average shorter drift path: faster charge collection, radiation hard

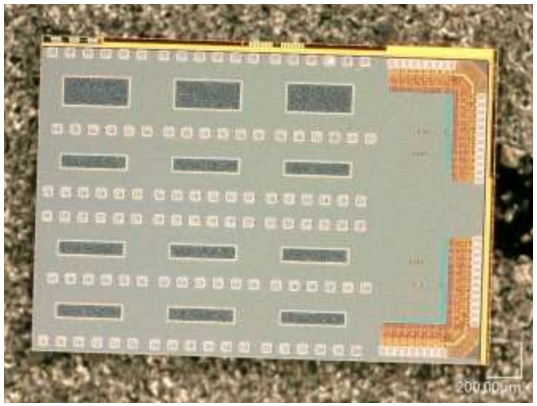
Choice of HVCMOS with 55nm Process

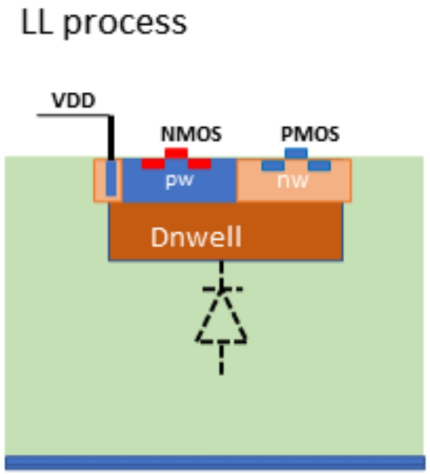
- The international mainstream technology is 180/150 nm process. HVCMOS pixel sensor will be applied to Mu3e experiment
- Motivation of chip R&D in 55nm process:
  - Smaller feature of process should provide stable support for mass production in next decades
  - Technological benefits: lower power, higher circuit density...



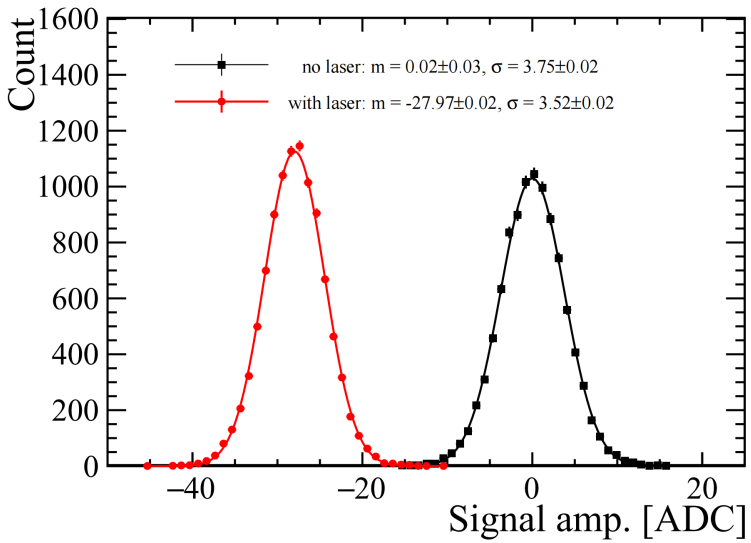
CMOS sensOr in Fifty-FivE nm procEss (COFFEE)

- COFFEE1 chip, $3 \times 2\mathrm{mm}^2$, verify the feasibility of 55nm process





- Sensor can responds to red laser, test with IDE1140 read-out chip

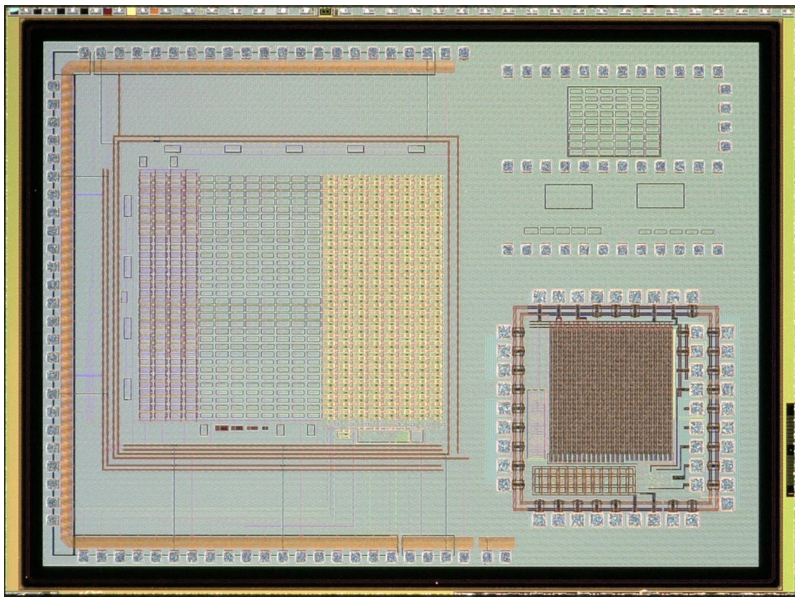


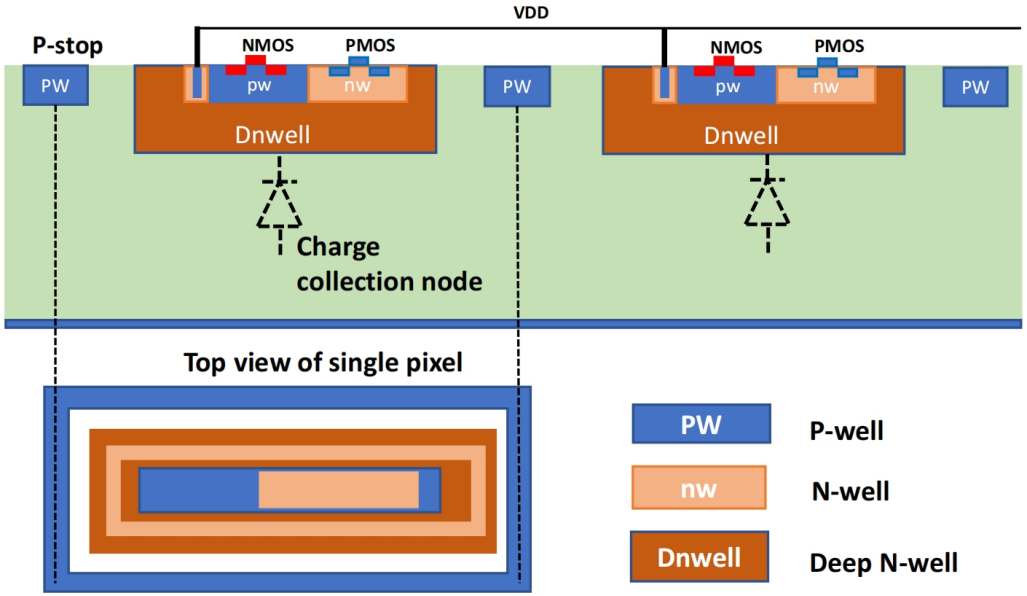
NIMA Volume 1069 P169905 (2024)

CMOS sensOr in Fifty-FivE nm procEss (COFFEE)

The first HVCMOS chip in 55nm process

COFFEE2 chip ($4 \times 3\mathrm{mm}^2$), real validation of the sensor



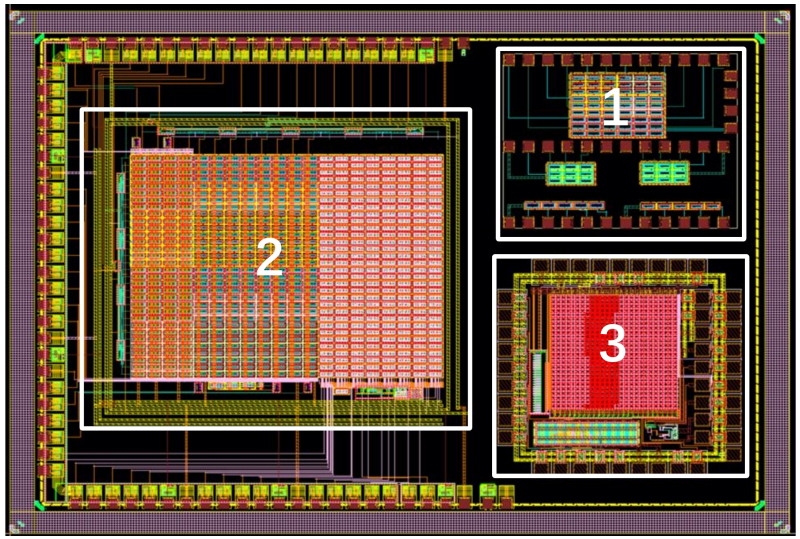


NIMA Volume 1069 P169905 (2024)

CMOS sensOr in Fifty-FivE nm procEss (COFFEE)

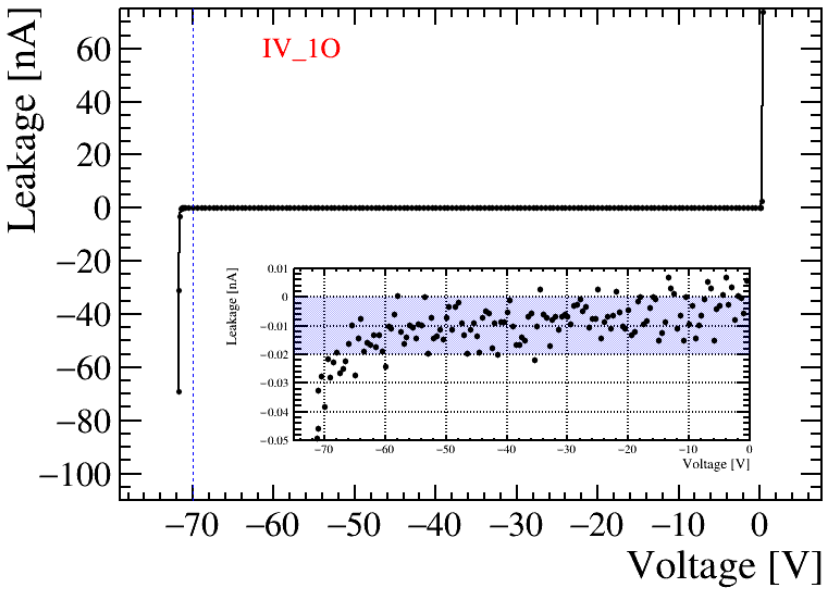
COFFEE2 chip contains 3 sectors

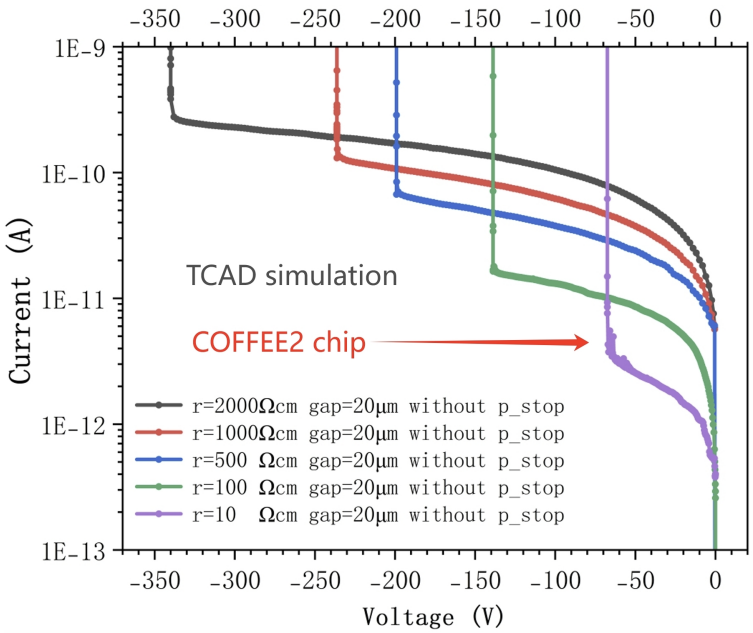
- Sector1: passive diode arrays with pixels of size $34 \times 68 \mu\mathrm{m}^2$ for study on sensing diode and charge sharing
- Sector2: 32 rows×20 columns pixel matrix, various diodes and in-pixel amplifier or discriminator designs for process validation
- Sector3: 26×26 pixel matrix of $21 \times 21 \mu\mathrm{m}^2$ pixels with digital readout periphery for novel electronics structure study (Hui Zhang's poster at TWEPP 2024)



Typical IV Test

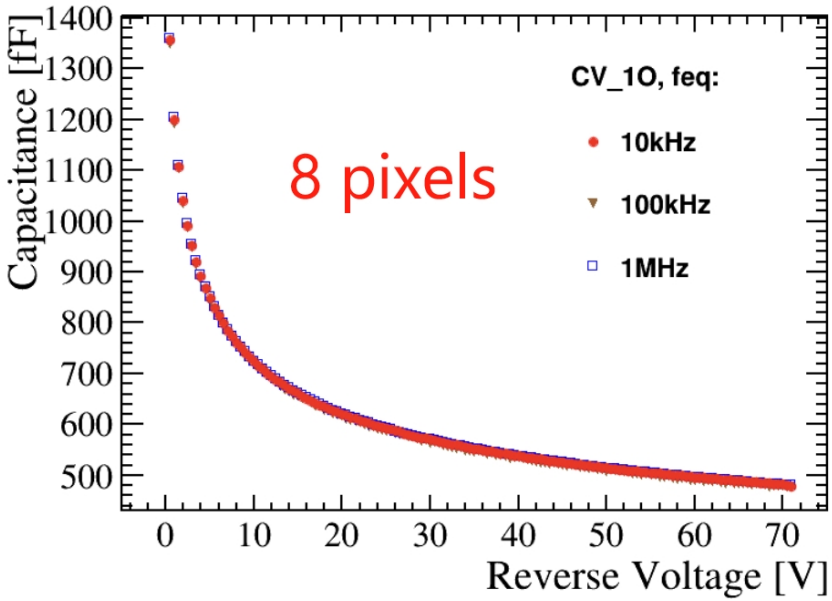
- Breakdown voltage $\sim$ 70V, leakage $\sim$ 10pA. Consistent with TCAD simulation with $10\Omega \cdot \mathrm{cm}$ resistivity substrate
- Breakdown voltage can be further improved with high resistivity substrate

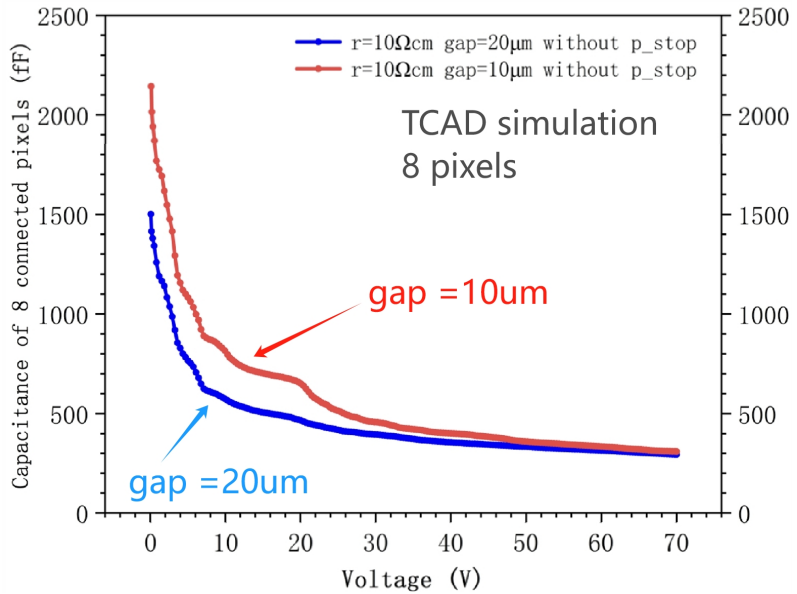


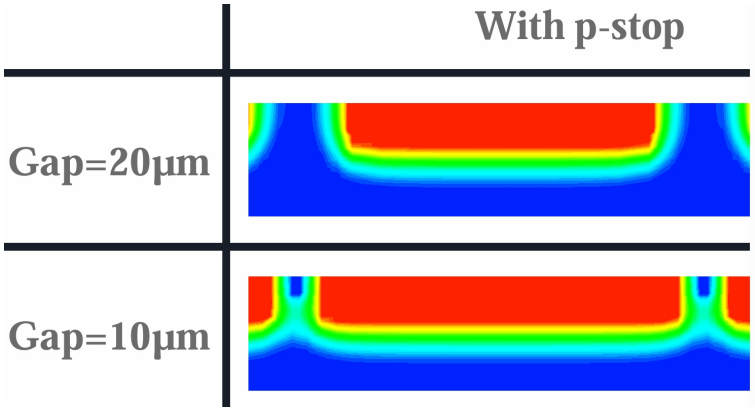


Typical CV Test

- At 70V, the capacitance of single pixel due to depletion $\sim 50\mathrm{fF}$
- Not fully depleted. The capacitance also takes into account parasitic effect (i.e. metal electrode/routing wire)

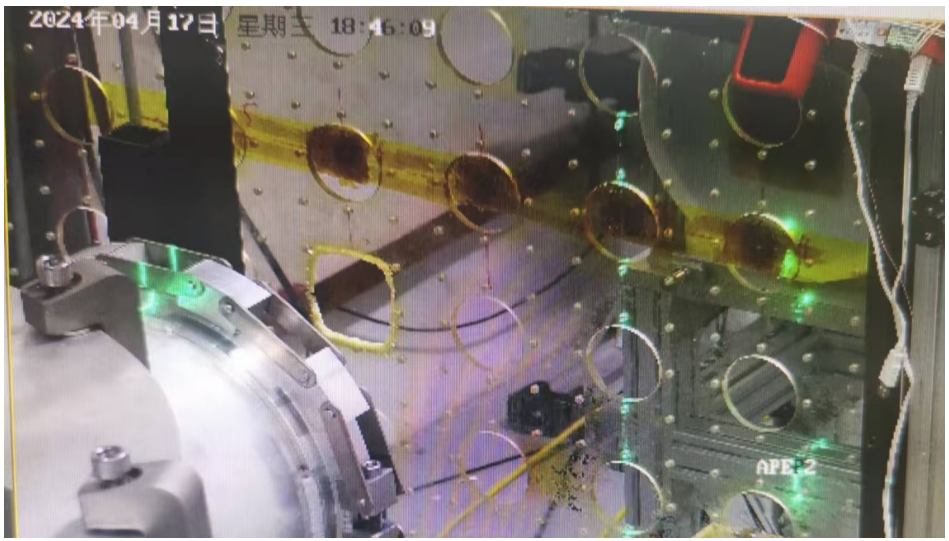


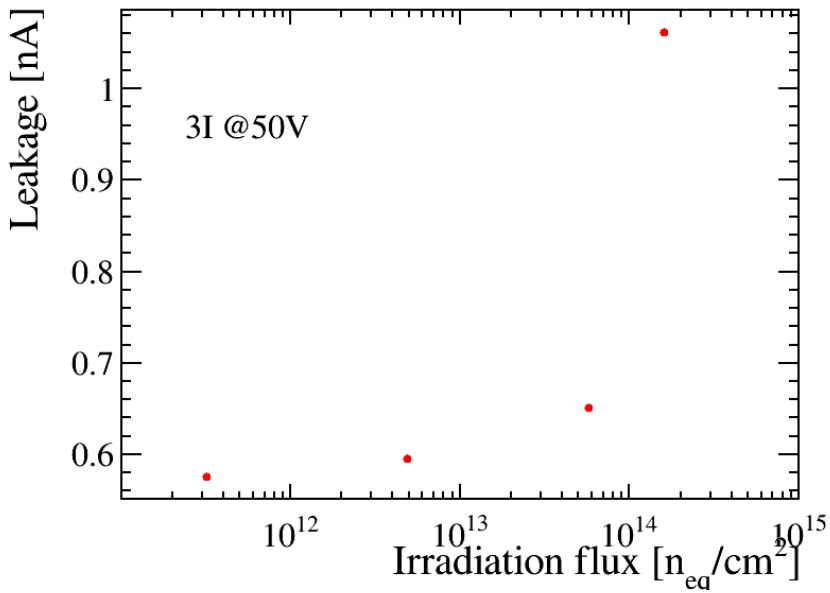




Glance at Irradiation Effect

- Proton beam @80MeV of CSNS
- Irradiation up to 1.6×10^{14} $\mathrm{n_{eq}/cm^2}$ at room temperature
- Leakage current increased to 1nA after irradiation

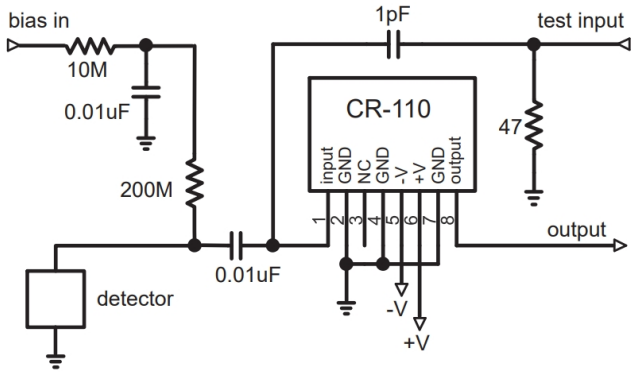


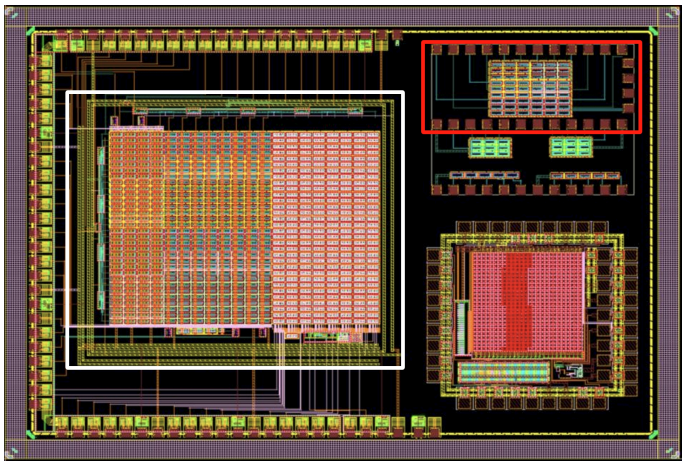


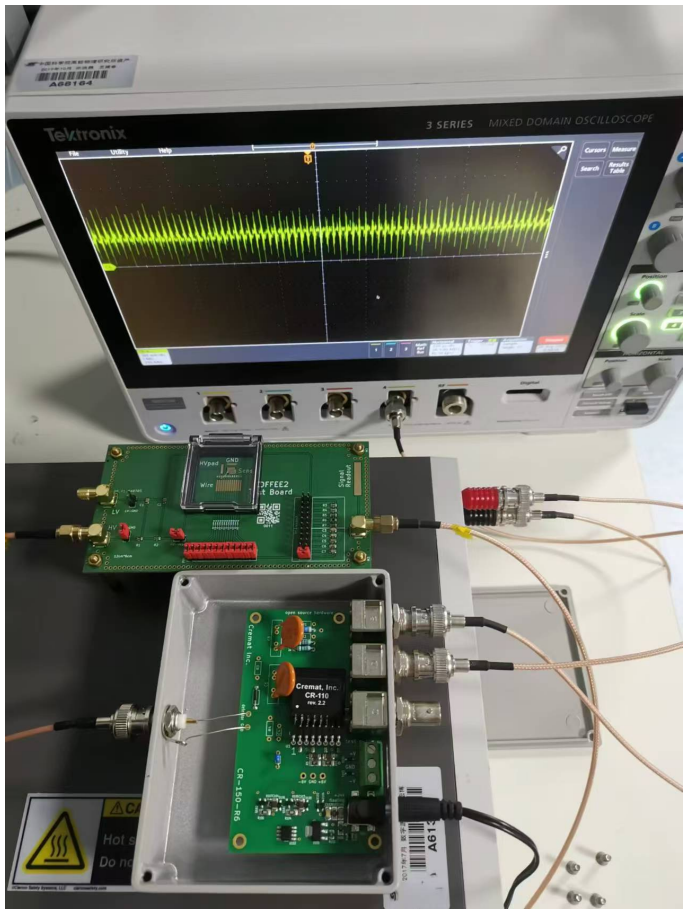
Test of Passive Sensors: Schematic

Sensor signal is delivered to the preamplifier via AC coupling.
An external charge sensitive preamplifier (link) used in test.

- Gain: $1\mathrm{mV/fC}$; Decay time constant: $140\mu s$; ENC RMS: 200 e

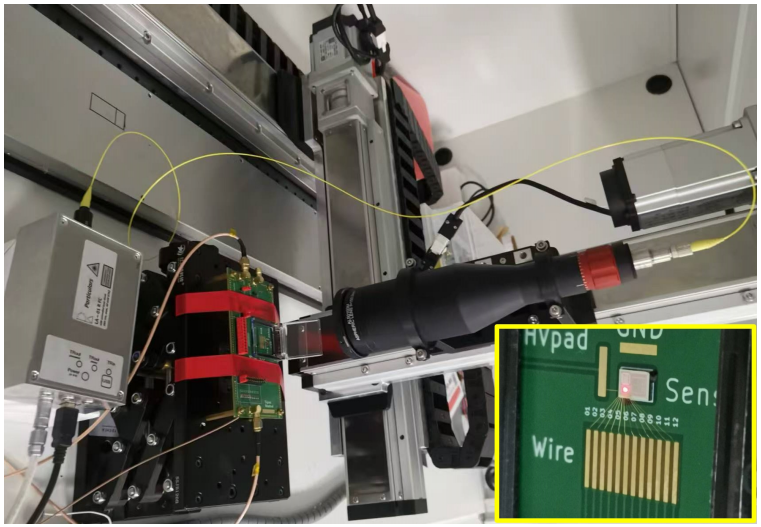


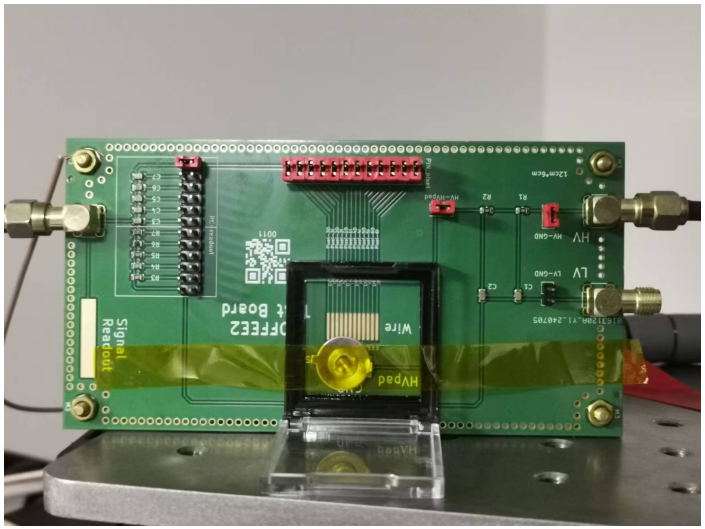


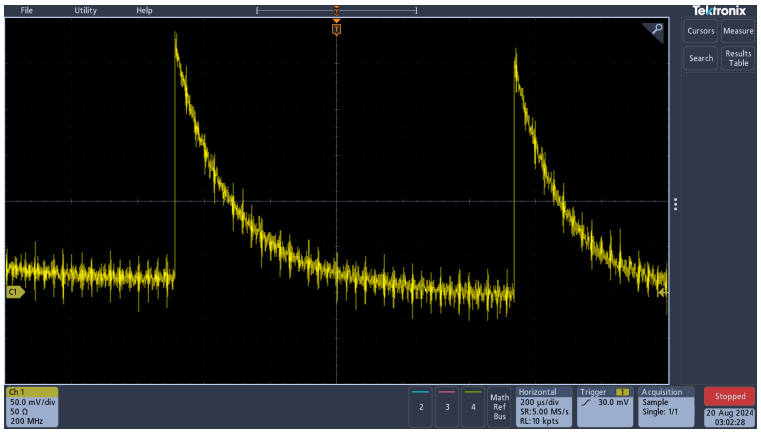


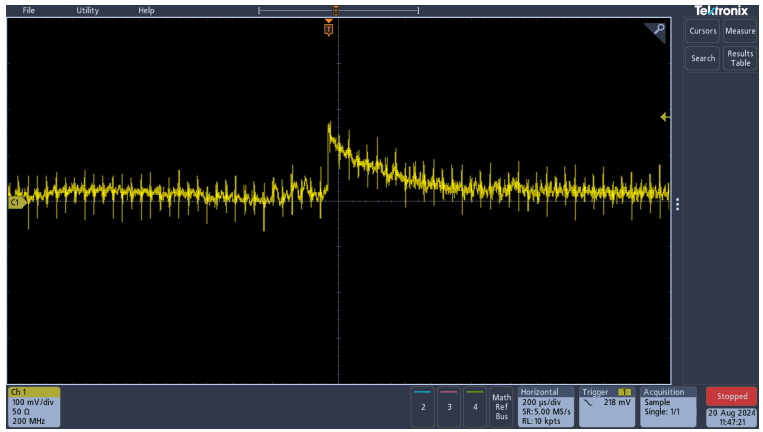
Test of Passive Sensors: Signal

- Clear response to both laser ($\lambda \sim 650\text{nm}$) and α radioactive source
  - 54 pixels read out at a time, via external charge sensitive amplifier



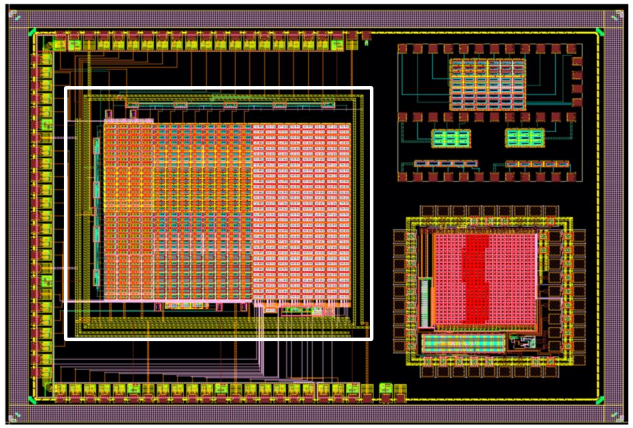






Active Pixel Matrix

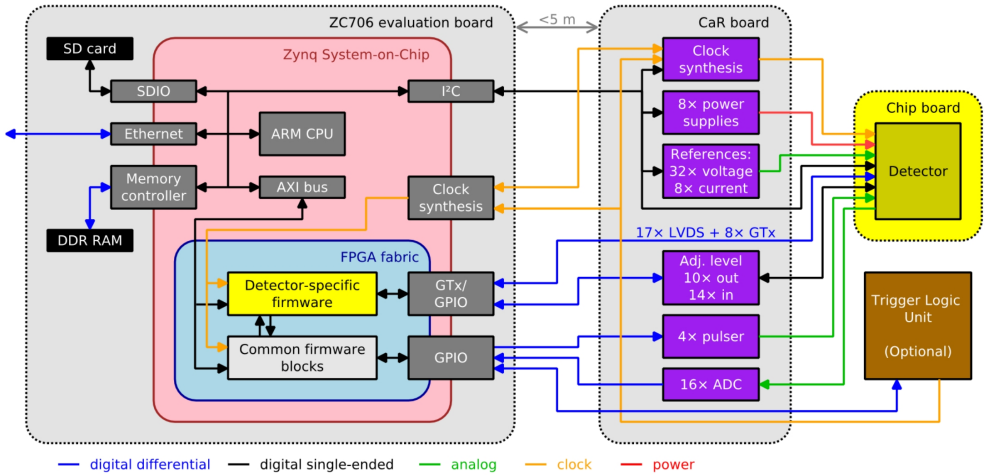
- 32 rows×20 columns active pixel matrix
- 3 variations of in-pixel electronics
  - CSA only
  - CSA + CMOS discriminator
  - CSA + NMOS discriminator
- Peripheral modules including analogue buffer, DACs and row/column switch

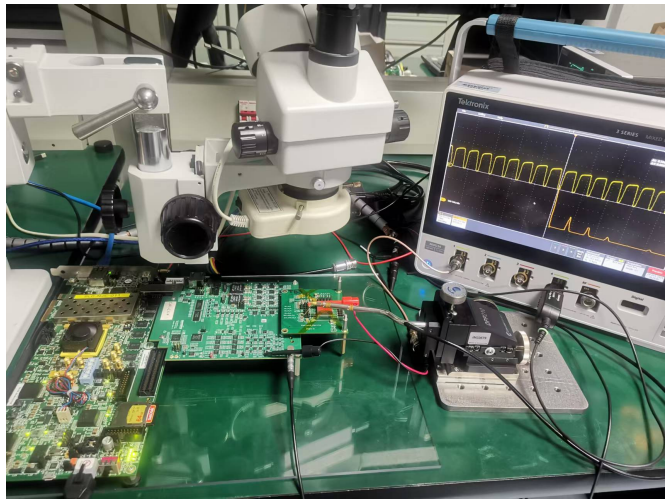


Active Pixel Matrix Test System

PC + ZC706 + Caribou board + dedicated chip board

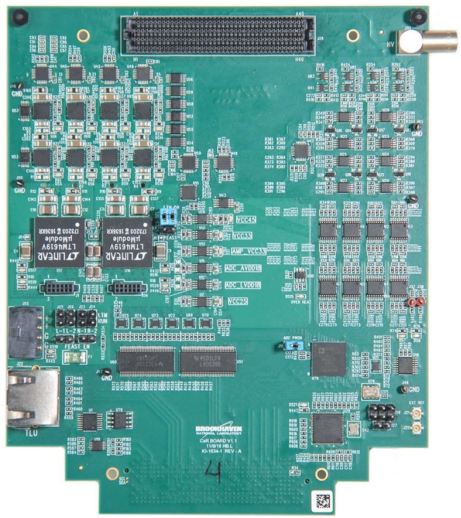
Caribou system architecture





Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector



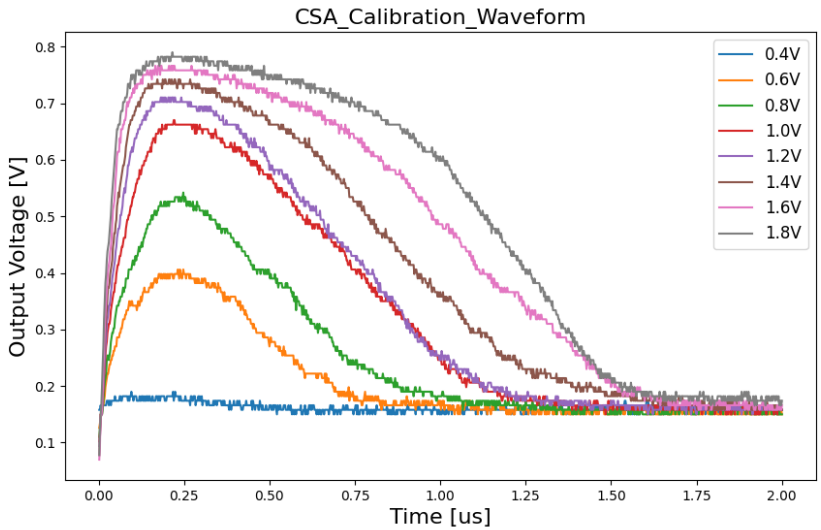
https://gitlab.cern.ch/Caribou/hardware/carboard

Resources for various target applications

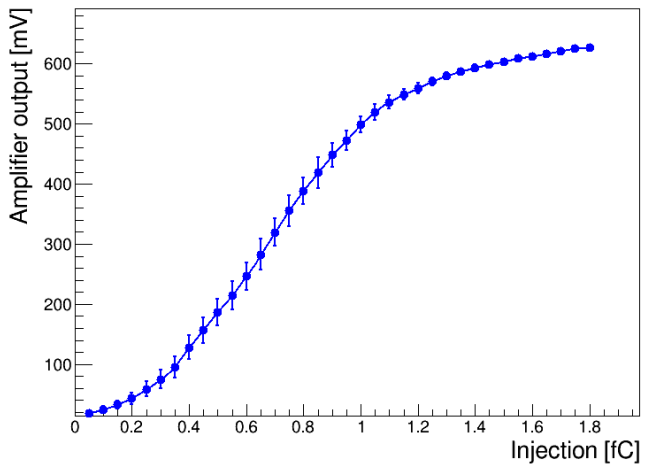
20 CaR boards v1.4 produced and distributed within RD50 common project

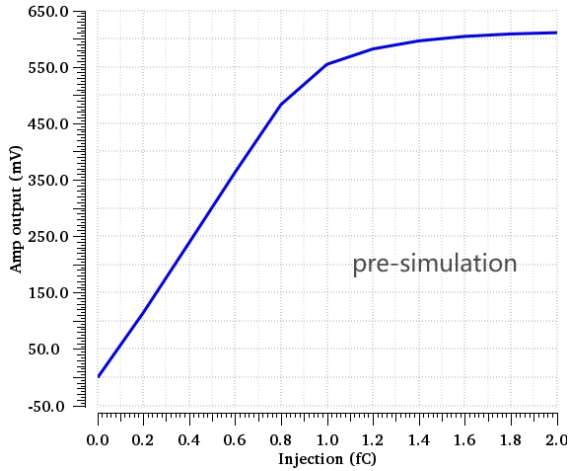
Active Pixel Test Preliminary Results

- CSA performance studied with charge injection



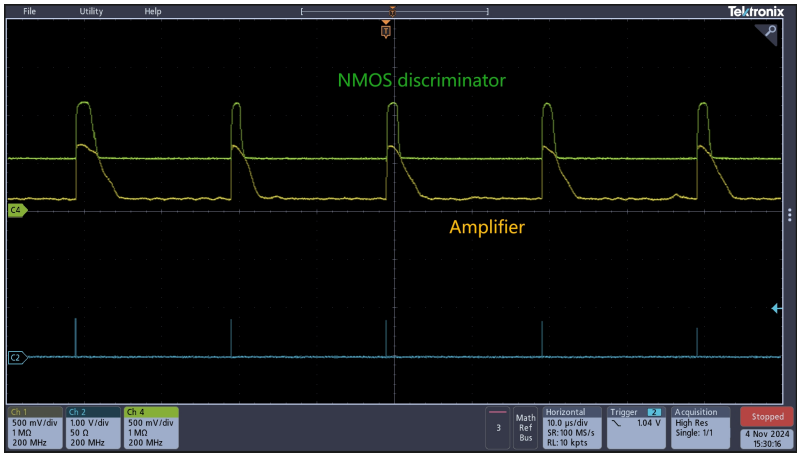
- Response curve consistent with simulation

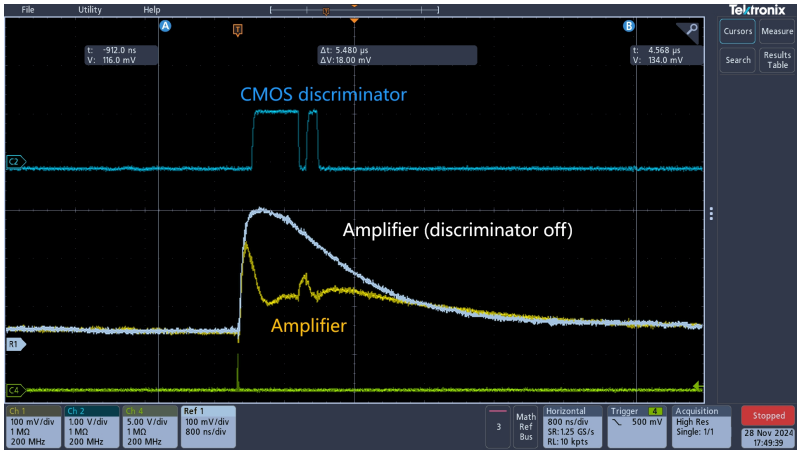




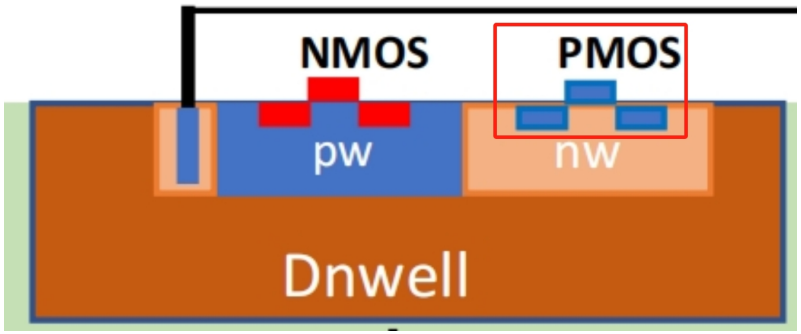
Active Pixel Test Preliminary Results

- Discriminator works, cross talk seen between CMOS discriminator and amplifier, can be mitigate by future design and offline analysis



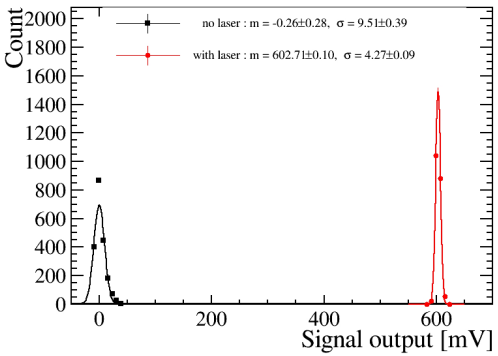


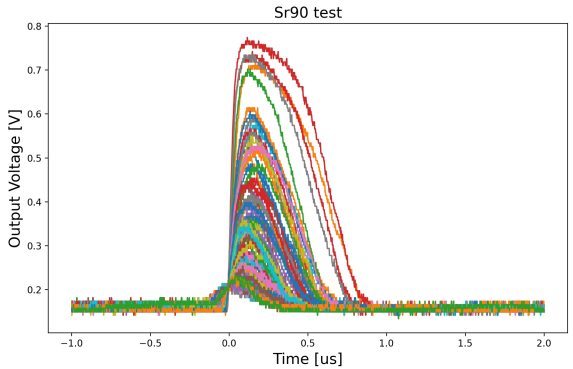
- The PMOS potential flip will cross talk to amplifier

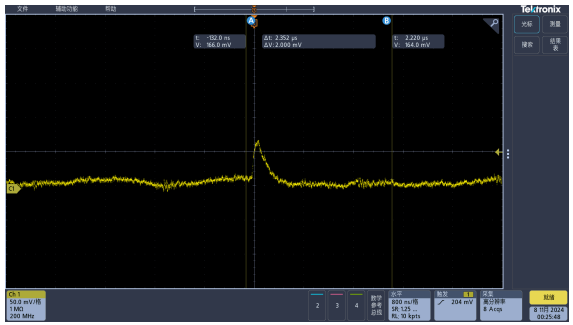


Active Pixel Test Results (preliminary)

- Clear signal response to red laser (left), β source (middle) and X-ray source (right)



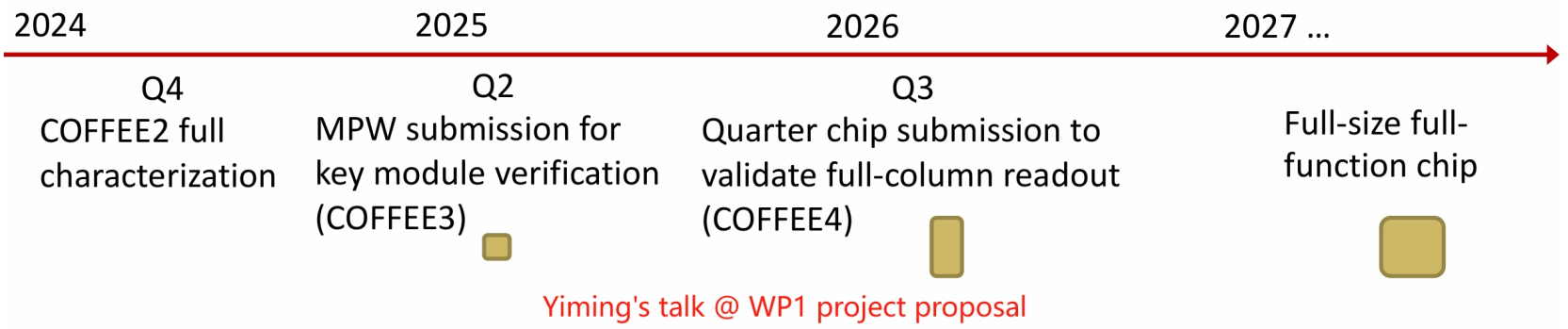




- For $^{55}\mathrm{Fe}$, signal amplitude consistent with expectation

Summary & Future

- First HVCMOS chip in 55nm process for future tracker
  - Test results show encouraging diode properties
  - Promising results with laser and radioactive source (α, β, X-ray)
  - Further test is ongoing
- More R&D ongoing for HVCMOS chip
  - Full functional COFFEE3 is currently being designed
  - Seeking for more MPW opportunities with high resistivity substrate



Welcome to join!