

Development of MAPS using 55nm HVCMOS process for future tracking detectors

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For the future era of high luminosity operation in LHCb experiment, the Upstream Tracker (UT) is planned to be upgraded to a higher granularity and radiation hard tracker. CMOS technology is a promising solution. Compared to hybrid silicon pixel sensors, CMOS processes enable smaller sensor sizes while maintaining a lower material budget. CMOS technology is also a potential candidate for the tracker of future CEPC experiment. Unlike many CMOS processes that require modifications to achieve sufficient signal generation, commercially available high-resistance wafer-based High Voltage CMOS (HVCMOS) is intrinsically radiation-hard. We have designed and submitted a prototype chip named COFFEE2, fabricated using a 55nm HV-CMOS process. This chip features a pixel array of 32 rows by 20 columns, divided into three regions, each with distinct in-pixel amplifier and comparator structures. Additionally, the chip includes a bandgap reference, row/column switch, and digital-to-analog converters (DACs) integrated into the peripheral circuitry surrounding the pixel matrix. We will present detailed electronic designs, simulation results, and preliminary test results from COFFEE2 chip.

Type of presentation (in-person/online)

online presentation (zoom)

Type of presentation (I. scientific results or II. project proposal)

I. Presentation on scientific results

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