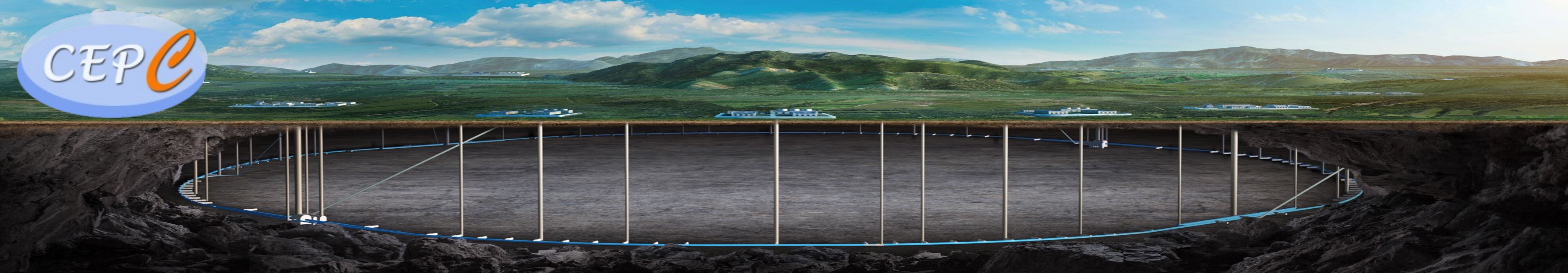

CEPC vertex Detector

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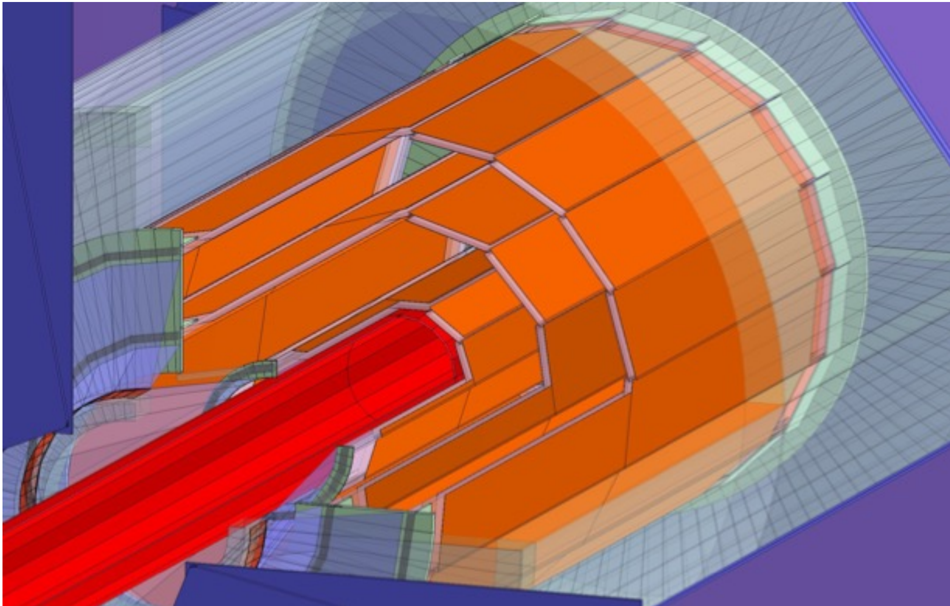
Chinese Academy of Sciences

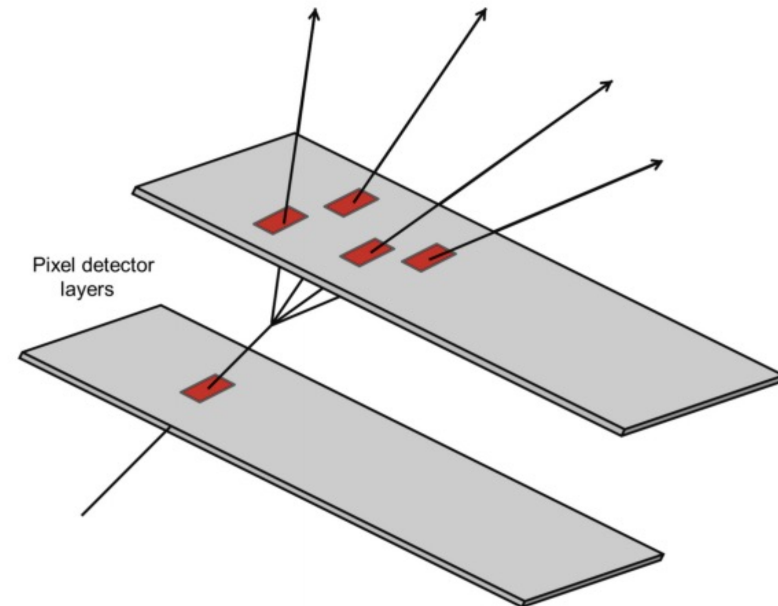
Content

- Introduction
- Requirements
- Technology survey and our choices
- Technical challenges
- R&D efforts and results
- Detailed design including electronics, cooling and mechanics
- Readout electronics & BEC
- Performance from simulation
- Research team and working plan
- Summary

Introduction: vertex detector

- Vertex detector optimized for first 10 year of operation
  - Higgs factory , low luminosity Z factory
- Motivation:
  - Aim to optimize impact parameter resolution and vertexing capability
  - Key detector for $H \to cc$ and $H \to gg$ physics, which is an important goal for CEPC



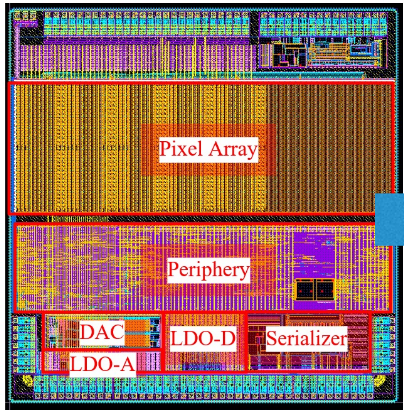


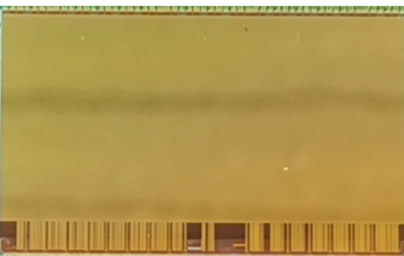
Vertex Requirement

- Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - **Challenges:** b-layer radius (11mm) is smaller compared with ALICE ITS3 (18mm)
- High data rate: (especially at Z pole , ~43MHz, 1Gbps per chip)
  - **Challenges**: 1Gbps per chip high data rate especially at Z pole
- Low material budget (less than 0.15%X0 per layer)
- Detector Cooling with air cooling (power consumption<=40 mW/cm^2)
- Spatial Resolution (3-5 um)
- Radiation level (~1Mrad per year in average)

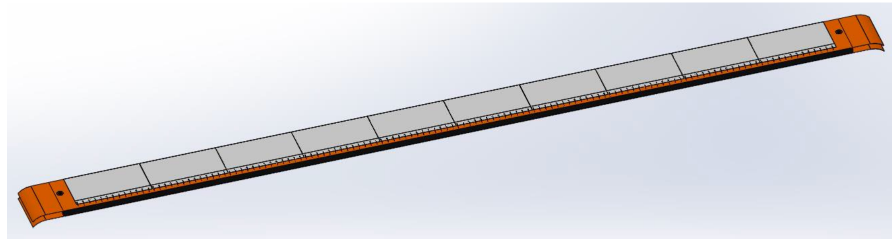
CEPC vertex detector prototype R & D

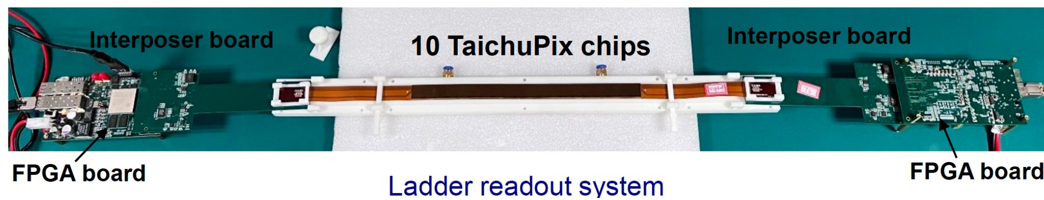
CMOS Sensor chip development



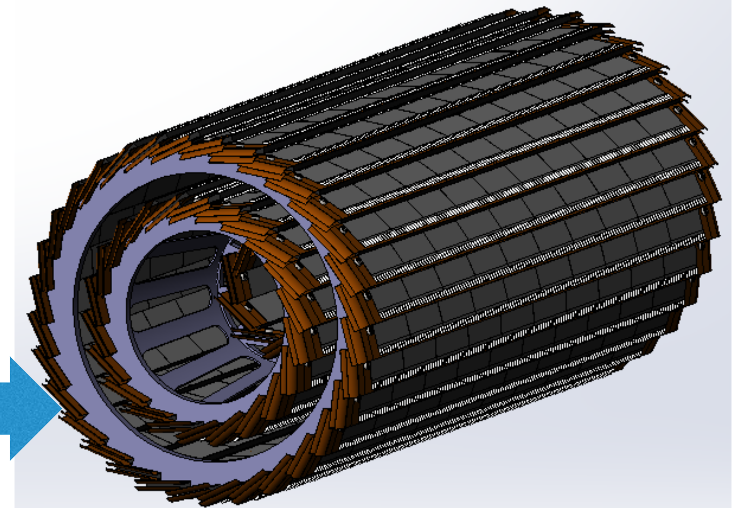


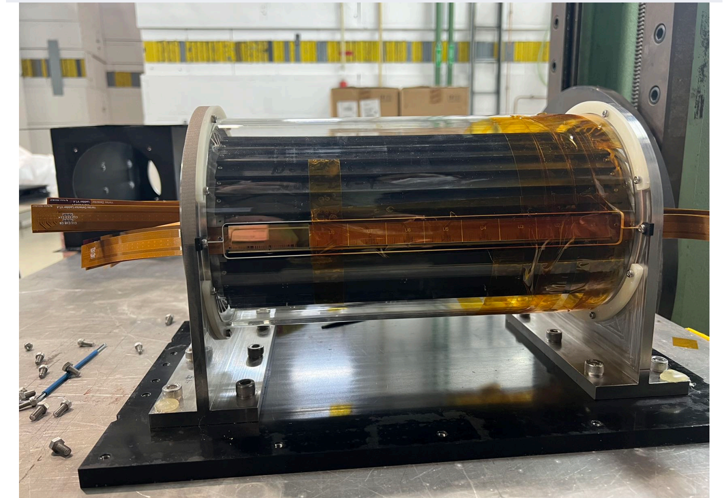
Detector module (Ladder) Prototyping





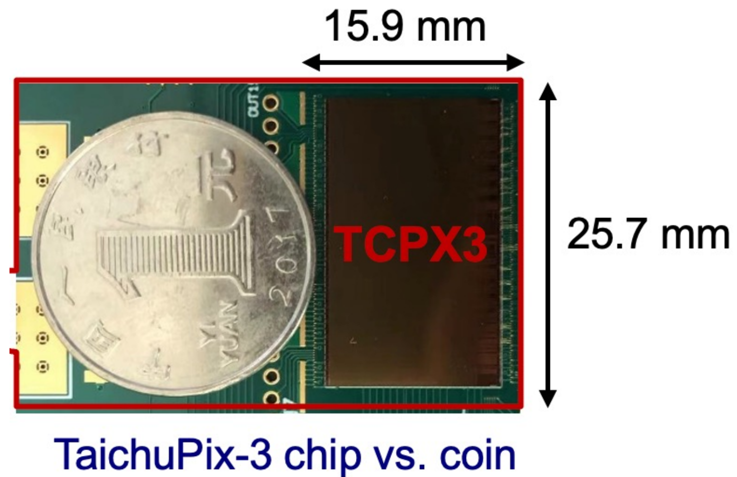
Vertex detector prototype



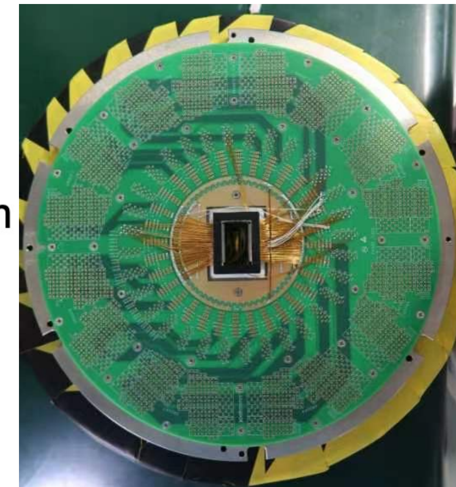


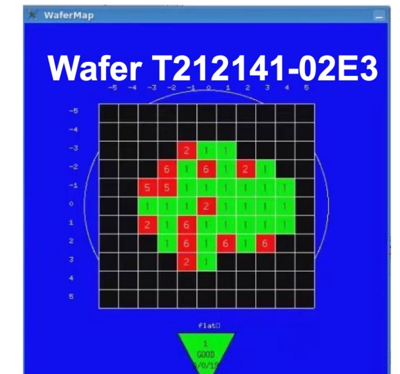
R&D efforts: Full-size TaichuPix3

- Full size CMOS chip developed, 1st engineering run
  - 1024×512 Pixel array, Chip Size: 15.9×25.7mm
  - 25μm×25μm pixel size with high spatial resolution
  - Process: Towerjazz 180nm CIS process
  - Fast digital readout to cope with ZH and Z runs (support 40MHz clock)



TaichuPix-3 chip vs. coin





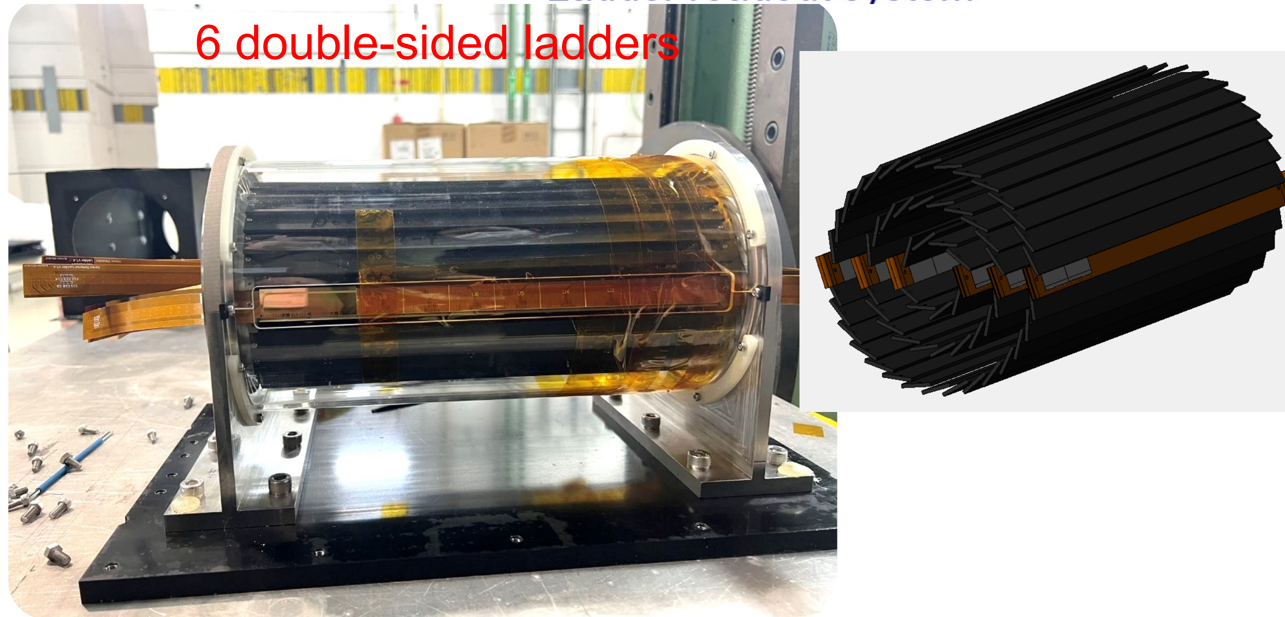
An example of wafer test result

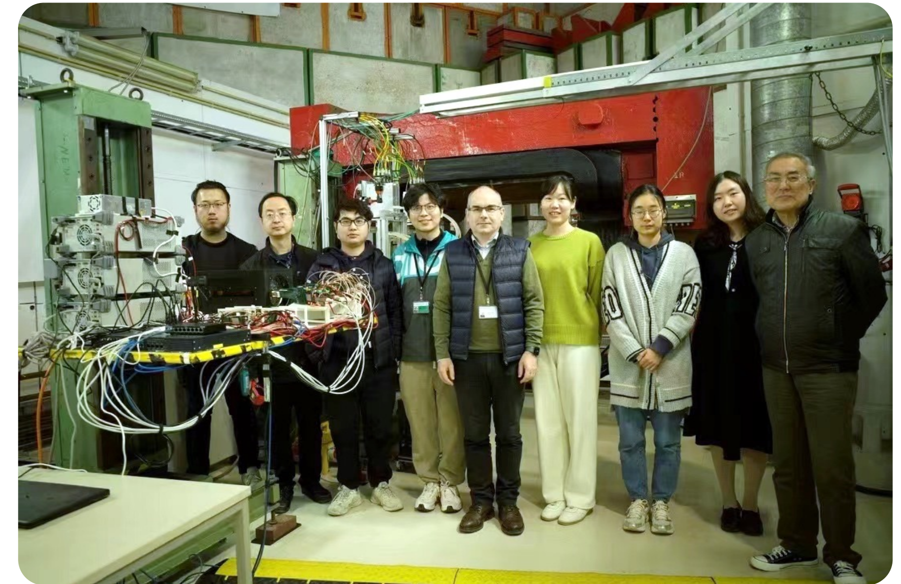
	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS

R&D effort: vertex detector prototype

TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution ~ **4.9 μm**

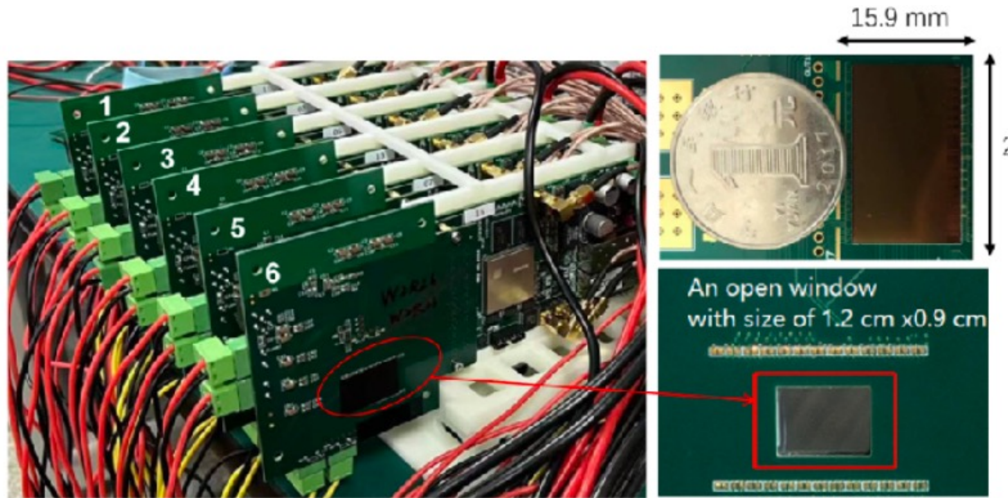


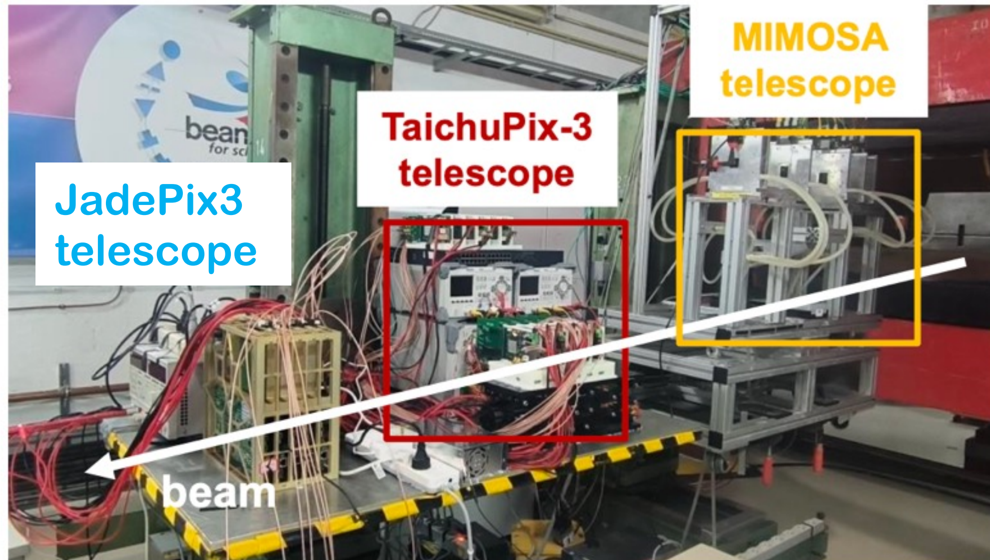


	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

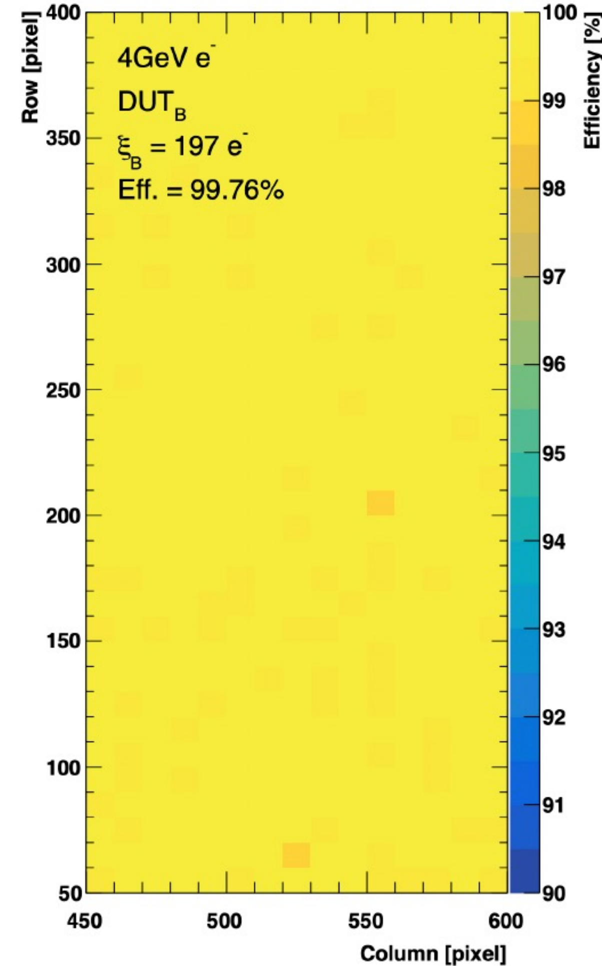
R&D efforts and results: Jadepix3/TaichuPix3 beam test @ DESY

Spatial resolution 4~5um, Efficiency >99%

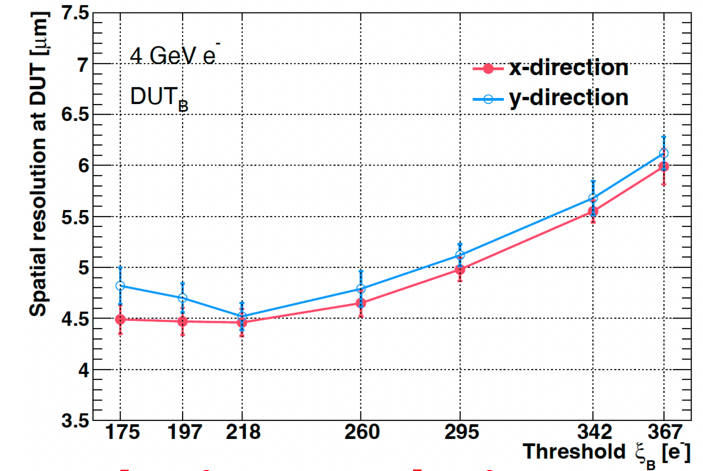




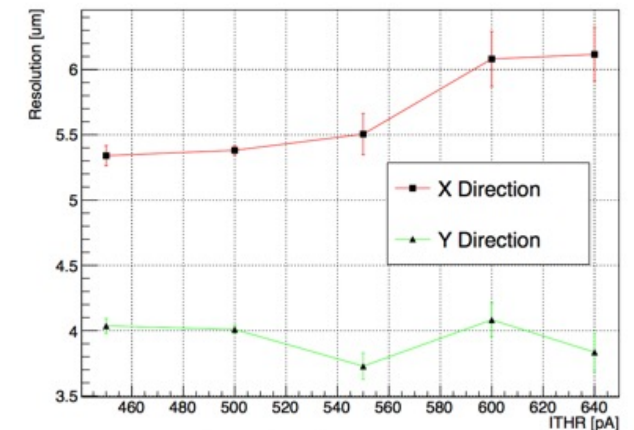
TaichuPix3 efficiency



TaichuPix3 resolution



JadePix3 resolution

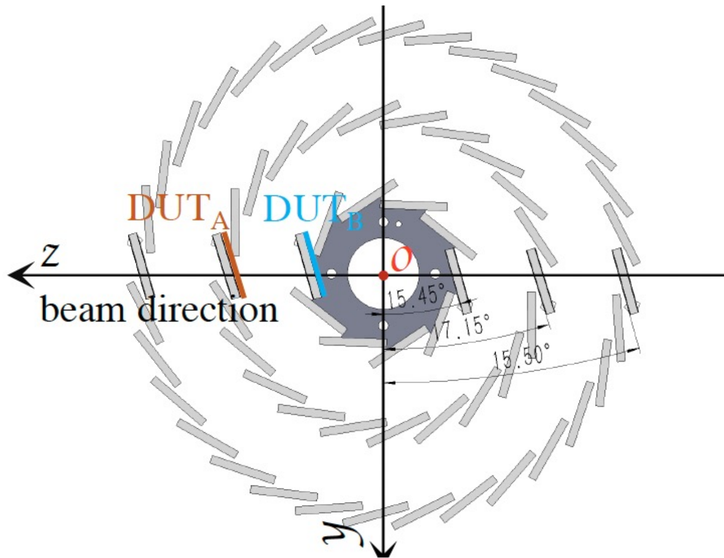


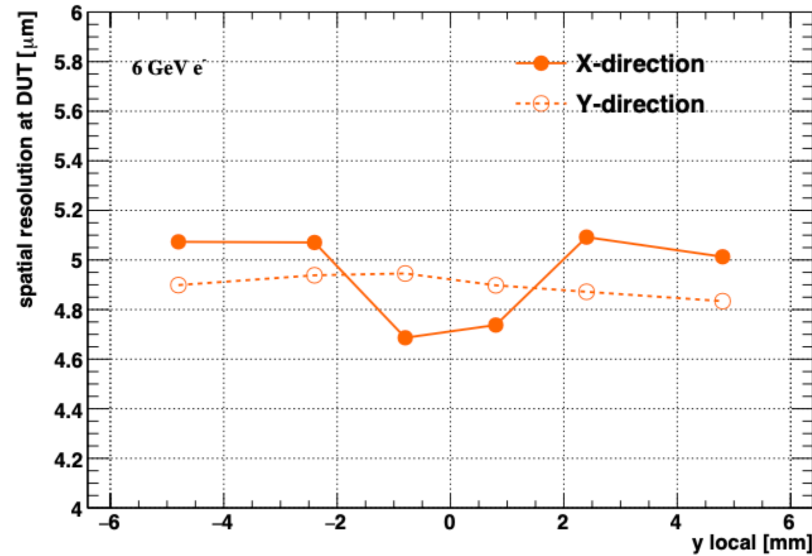
Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

R&D efforts and results: vertex detector prototype beam test

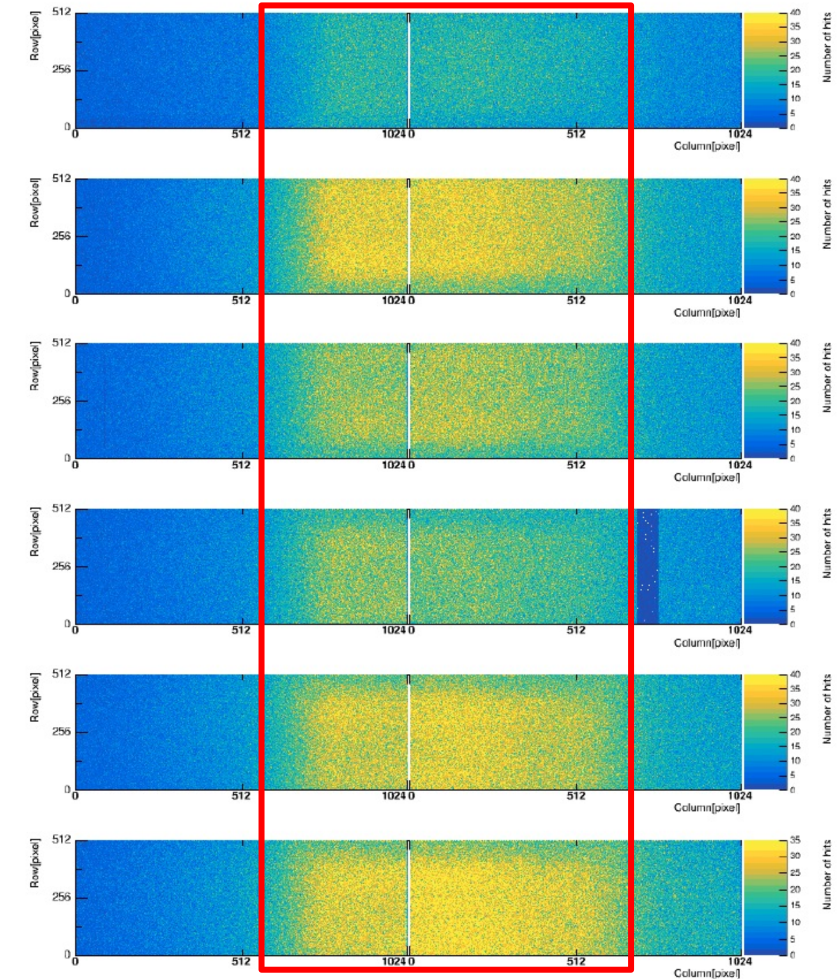
Spatial resolution ~ **5 μm**

Hit maps of multiple layers of vertex detector





Beam spot

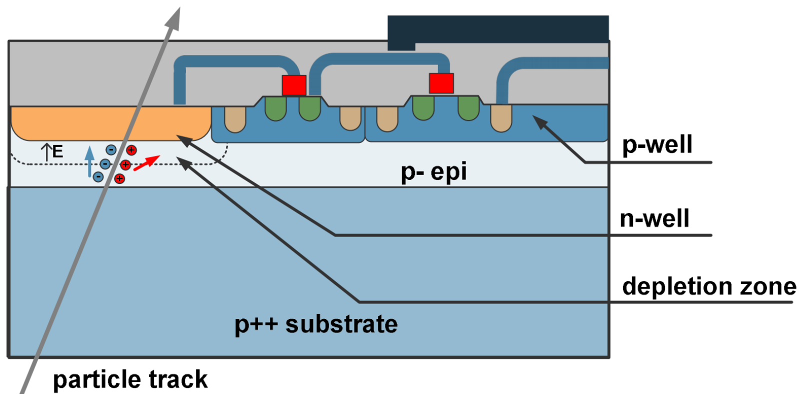


	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

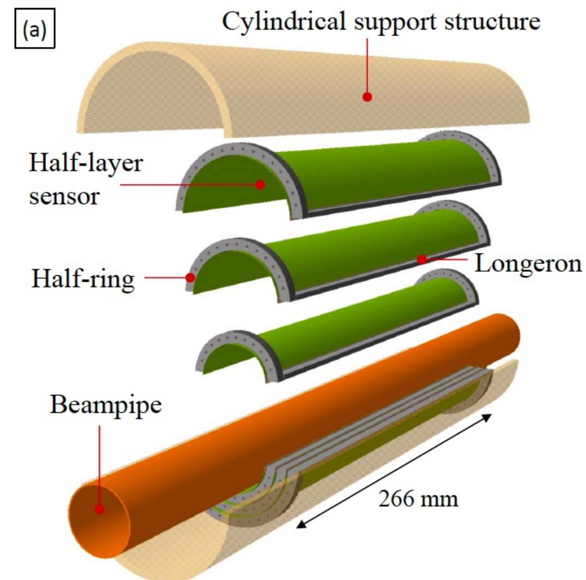
Technology survey and our choices

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

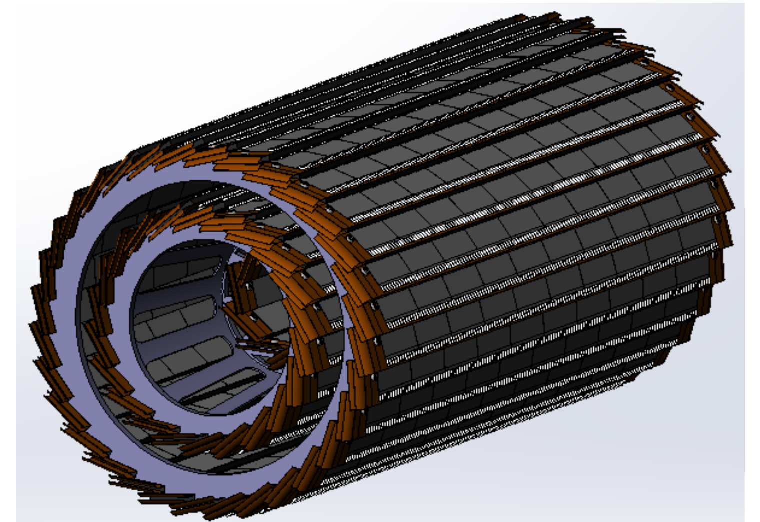
Monolithic active Pixel CMOS (MAPS)



Baseline: curved MAPS



Alternative: ladder based MAPS



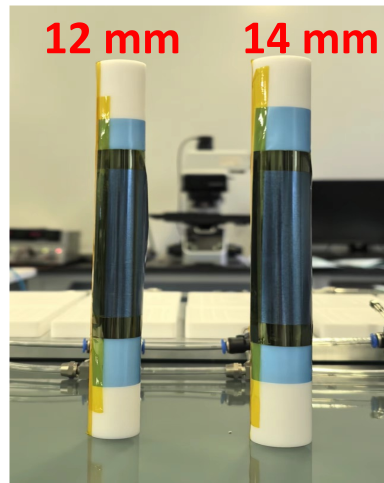
[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

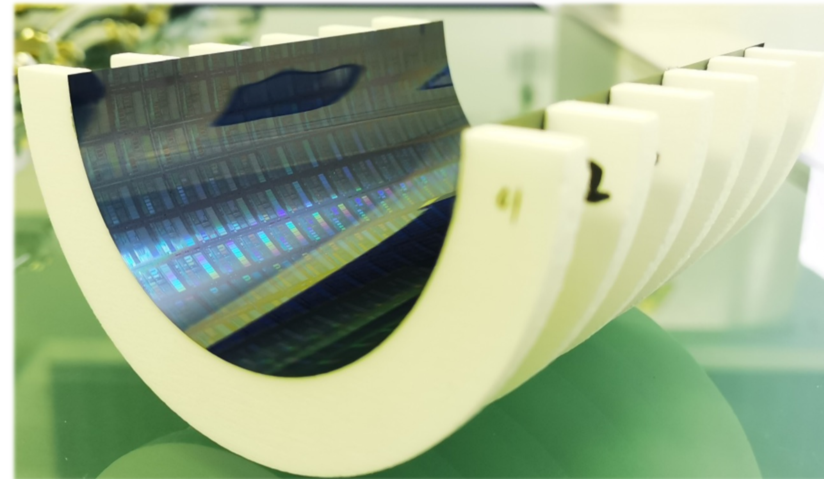
R&D efforts curved MAPS

– CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)

– Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12mm

  - The dummy wafer has been thinned to 40μm

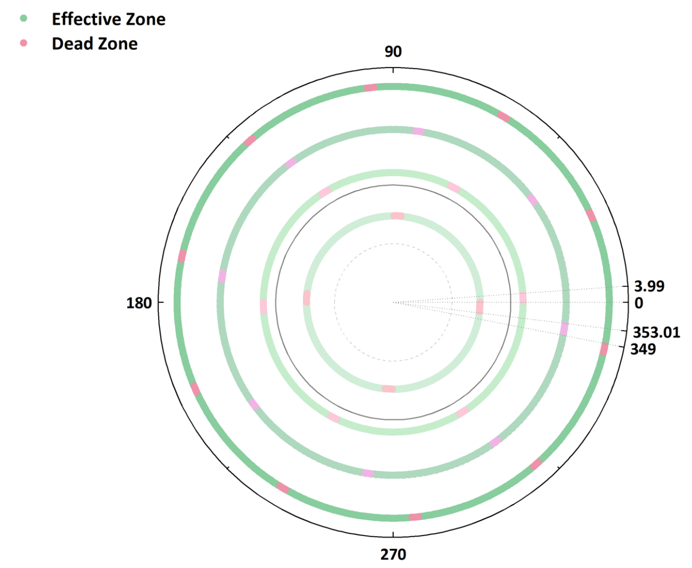




	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

Baseline: bent MAPS

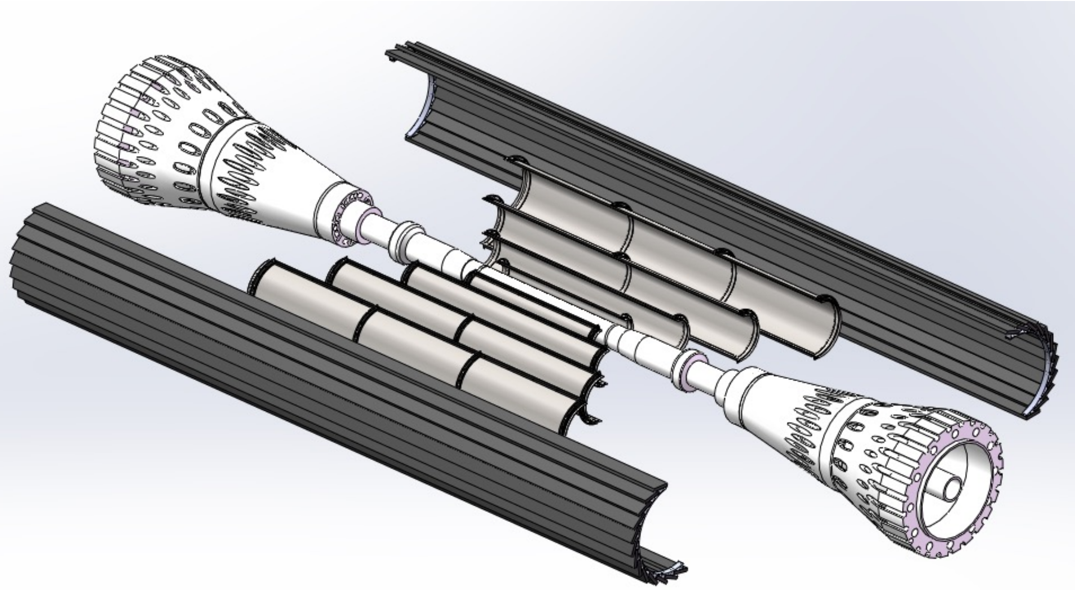
- 4 single layer of bent MAPS + 1 double layer ladder
  - Material budget is much lower than alternative option
- Use single bent MAPS for Inner layer (~0.15m^2)
  - Low material budget 0.06%X0 per layer
  - Different rotation angle in each layer to reduce dead area

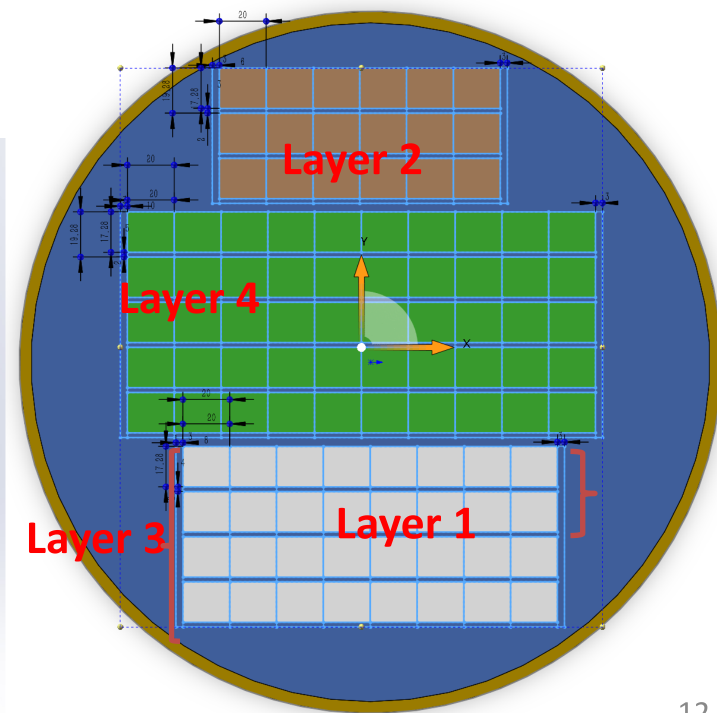


Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

Long barrel layout (no endcap disk) to cover cos θ<=0.991

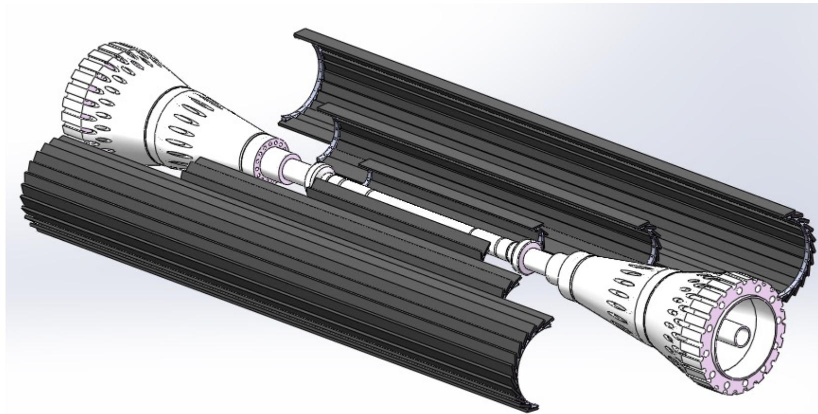
layer	Radius	Material
Layer 1	11mm	0.06% X0
Layer 2	16.5mm	0.06% X0
Layer 3	22mm	0.06% X0
Layer 4	27.5mm	0.06% X0
Layer 5/6 (Ladders)	35-40 mm	0.33% X0
Total		0.57% X0



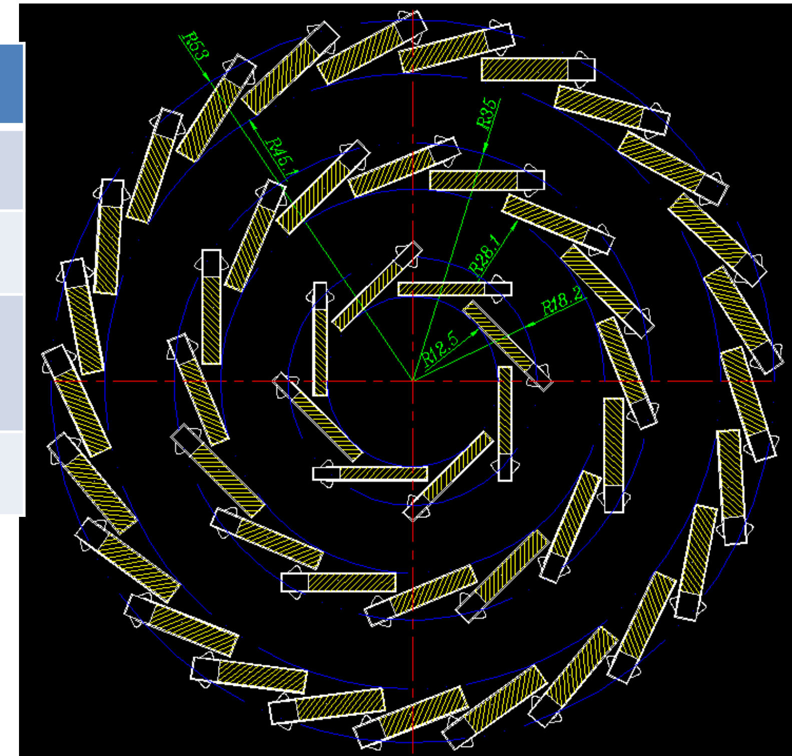


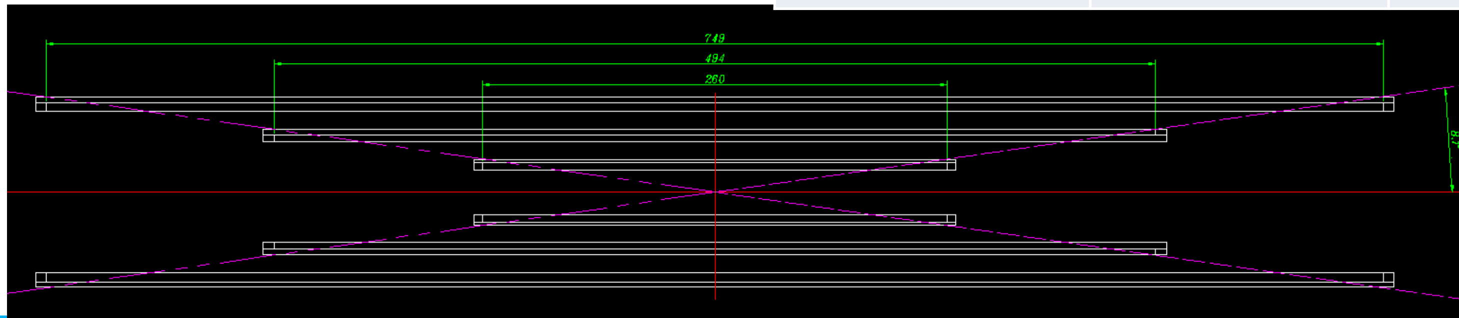
Alternative： CMOS ladder

- Alternative: CMOS chips with a long ladder layout
  - 3 double-side layer with long ladders design
  - We have built a vertex prototype based on the short ladders design
  - No effective solution for inner layer cooling yet.



layer	Radius	Material
Layer 1/2	12.5 -18 mm	~0.33% X0
Layer 3/4	28 - 35mm	~0.33% X0
Layer 5/6 (Ladders)	45 - 53mm	~0.33% X0
Total		~1% X0





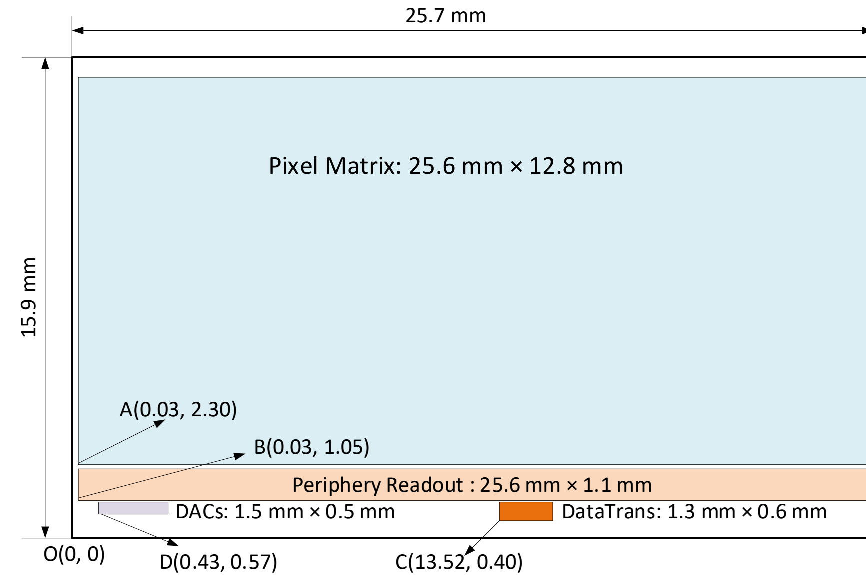
Data rate estimation of vertex detector

	Hit rate (MHz/cm^2)	Data rate@triggerless ($Gbps/cm^2$)
Higgs	0.61	0.18
WW	3.16	0.98
Low lumi Z pole	3.9	1.2

- Data rate is dominated by background from pair production
- WW runs and low Lumi Z runs (20% of high lumi Z)
- Data rate @1.2Gbps per chip for triggerless readout

Chip design for ref- TDR and power consumption

- Power consumption
  - **Fast priority digital readout** for 40MHz at Z pole
  - 65/55nm CIS technology
  - Power consumption can reduced to ~40mW/cm^2
- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 3 m/s air speed, estimated by thermal simulation

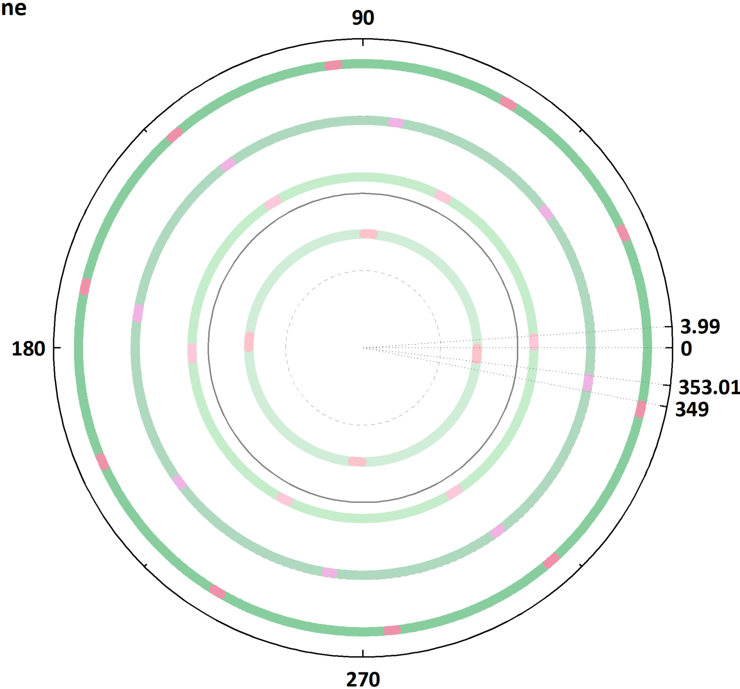


	Matrix	Periphery	DataTrans.	DACs	Total Power	Power density
65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z)	60 mW	80 mW	36 mW	10 mW	186 mW	~40 mW/cm^2

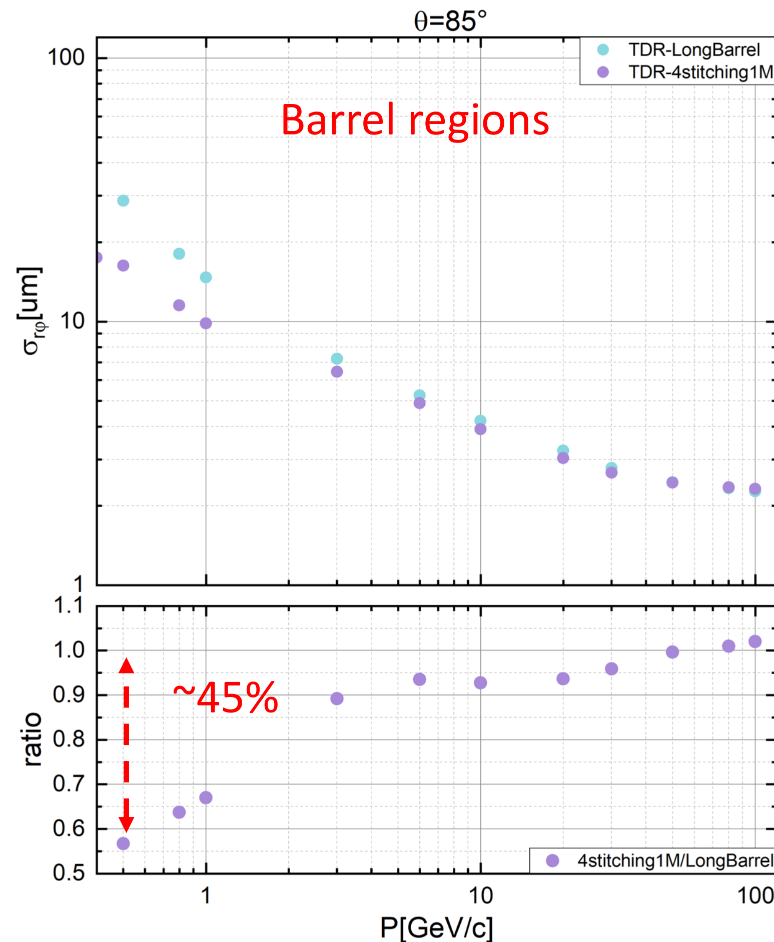
Performance: impact parameter resolution

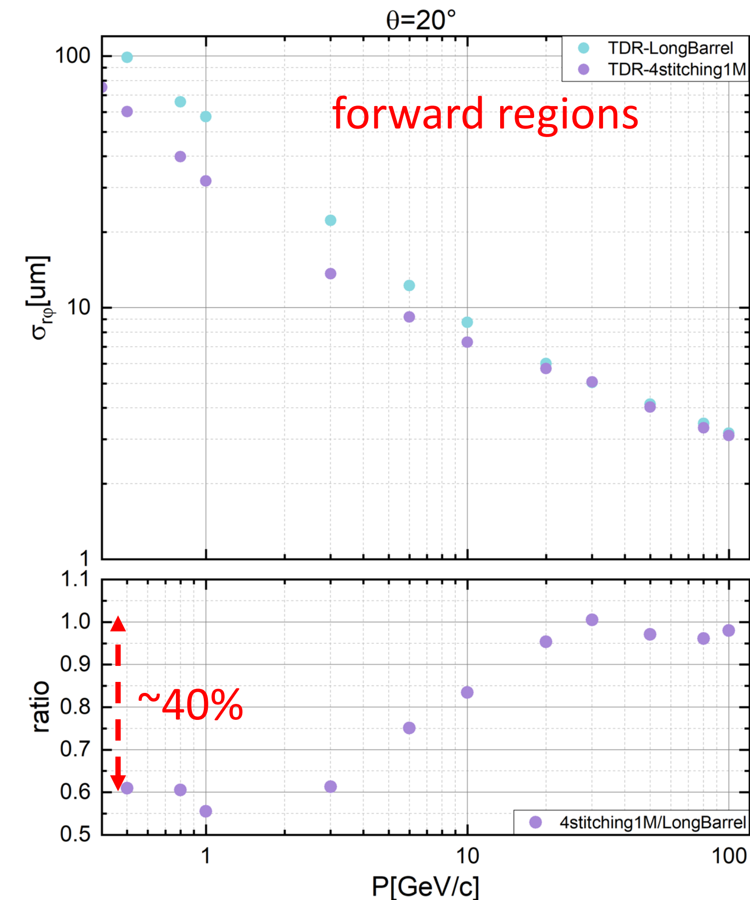
- Compared to alternative (ladder) option
  - baseline (stitching) has significant improvement (~45%) in low momentum case

Different rotation angle in each layer to reduce dead area



Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.





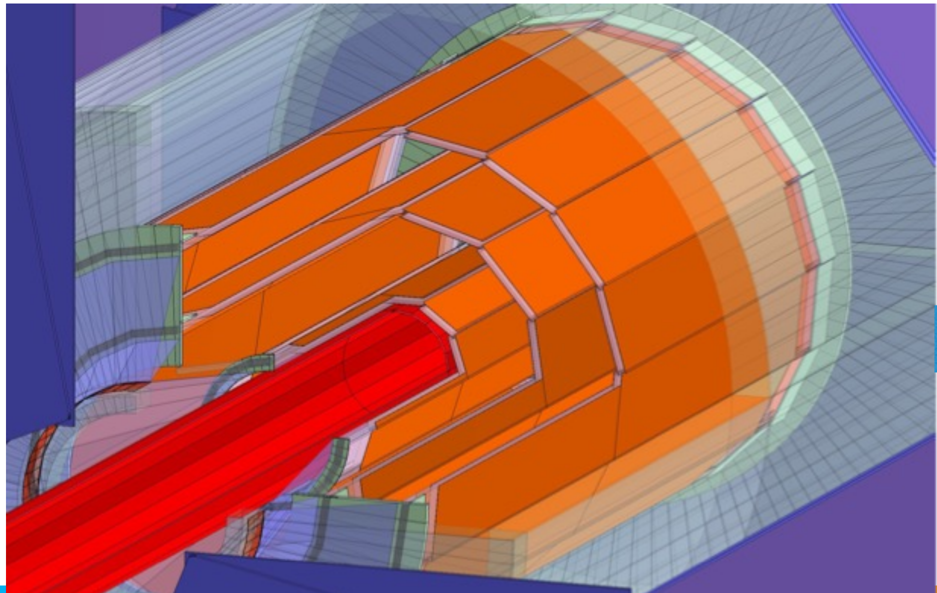
Contributions and Collaborations

- IHEP Beijing: Chip designs, electronics, DAQ and prototype assembly
- IPHC/CNRS: Collaboration in framework of FCPPL, BELLE II upgrade
- IFAE: Collaboration in Taichu chip design
- ShanDong U.: Stitching chip design, Taichu chip design
- CCNU: Jadpix chip design
- Northwestern Polytechnical U. : Taichu Chip design
- Nanchang U. : Taichu chip design
- Nanjing U. : testbeam study

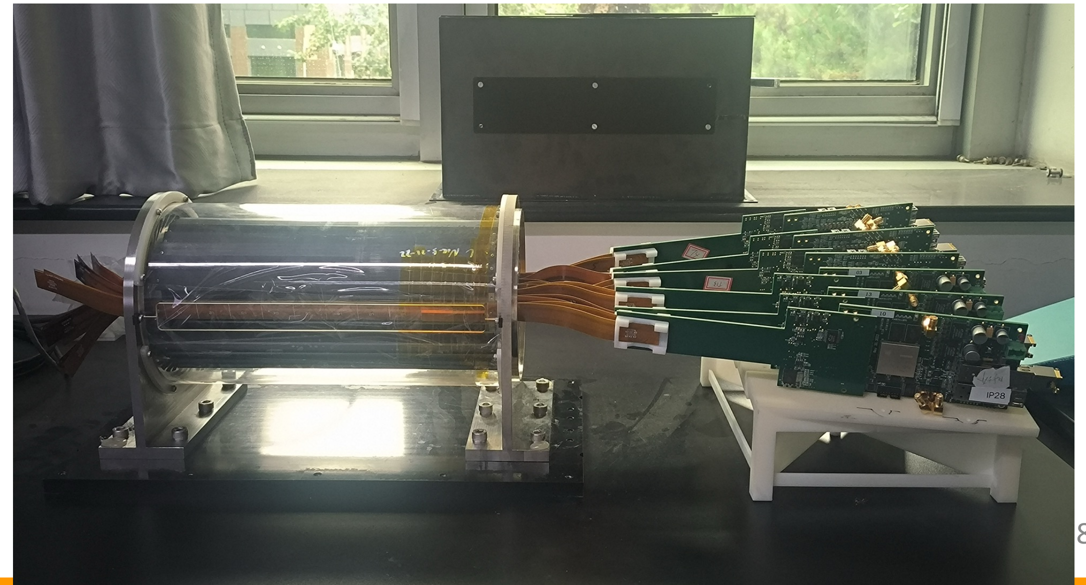
Summary

- 1st full-size Prototype based the ladder design for CEPC vertex detector has been developed
- The Curved MAPS option has been chosen as baseline for the reference detector TDR.
  - More R & D needed for this option
  - Preparing a work package proposal towards research for vertex detector in future lepton collider
  - Exploring synergies with other projects

CEPC vertex conceptional design (2016)



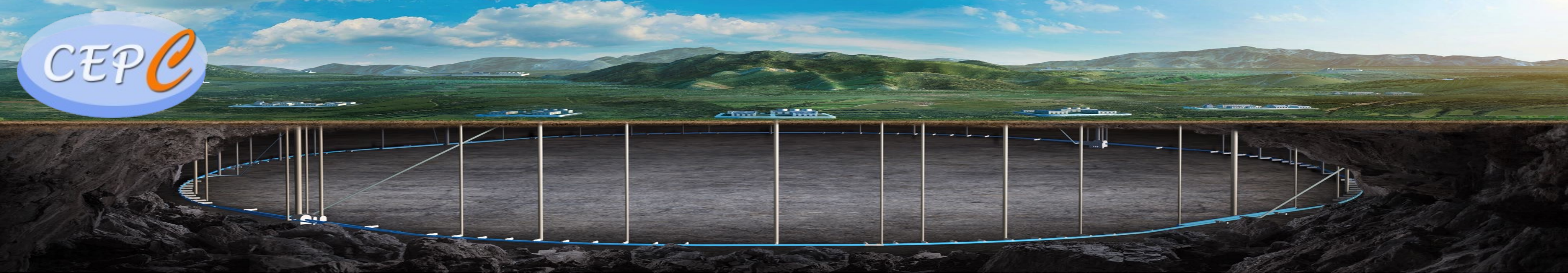
CEPC vertex prototype (2023)



Preliminary idea about working package

- Aim to develop vertex detector for future lepton collider
  - 3-5um spatial resolution
  - 40-43.3MHz clock, Can handle 1Gbps data rate in single chip level
  - Power consumption ~40mW/cm^2
  - Stitching design, can be used in for curved MAPS vertex detector

	Deliverables	Goal
2025	TJ180nm CIS stitching engineering run	Verify the stitching technology for high data rate
2026	TJ65nm CIS MPW chip (joint MPW runs ?)	Validate the basic design for 65nm technology
2027-2028	TJ65nm CIS engineering run	Validate final design



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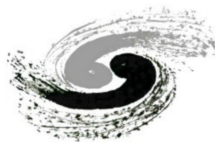
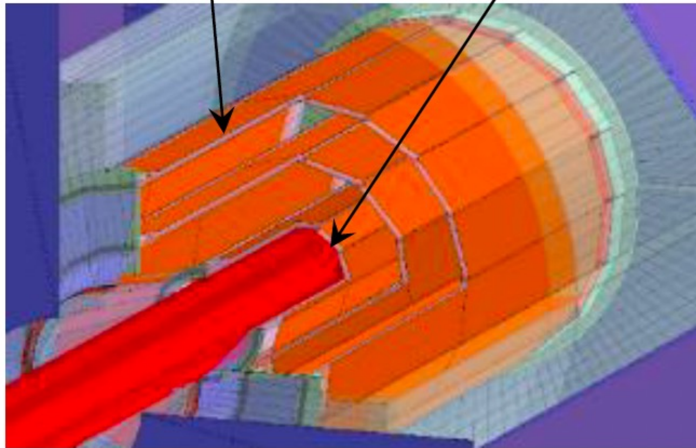


中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Backup

Silicon Pixel Chips for Vertex Detector



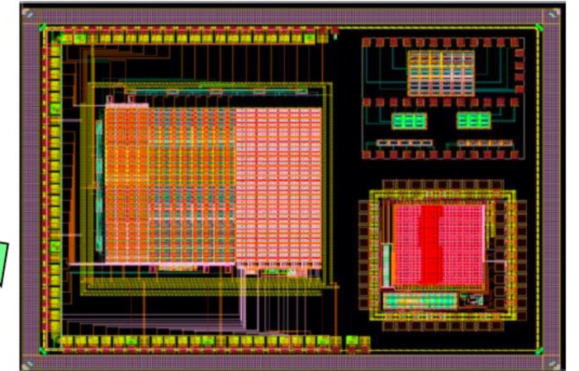
Goal: σ(IP) ~ 5 μm for high P track

CDR design specifications

- **Single point resolution ~ 3µm**
- **Low material (0.15% X_0 / layer)**
- **Low power (< 50 mW/cm^2)**
- **Radiation hard (1 Mrad/year)**

Silicon pixel sensor develops in 5 series: JadePix, TaichuPix, CPV, Arcadia, COFFEE

Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process

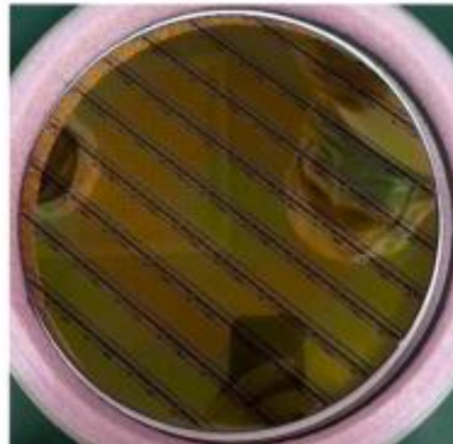


JadePix-3 Pixel size ~16×23 μm^2

Tower-Jazz 180nm CiS process
Resolution 5 microns, 53mW/cm^2

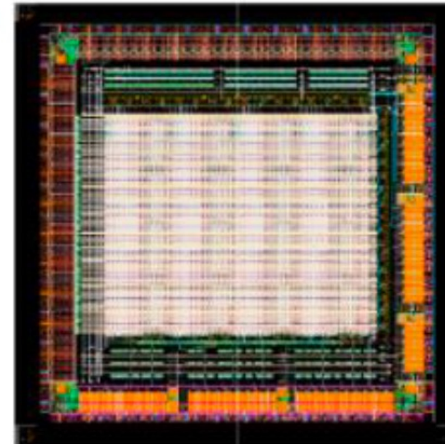
MOST 1

TaichuPix-3, FS 2.5x1.5 cm^2
25×25 μm^2 pixel size



MOST 2

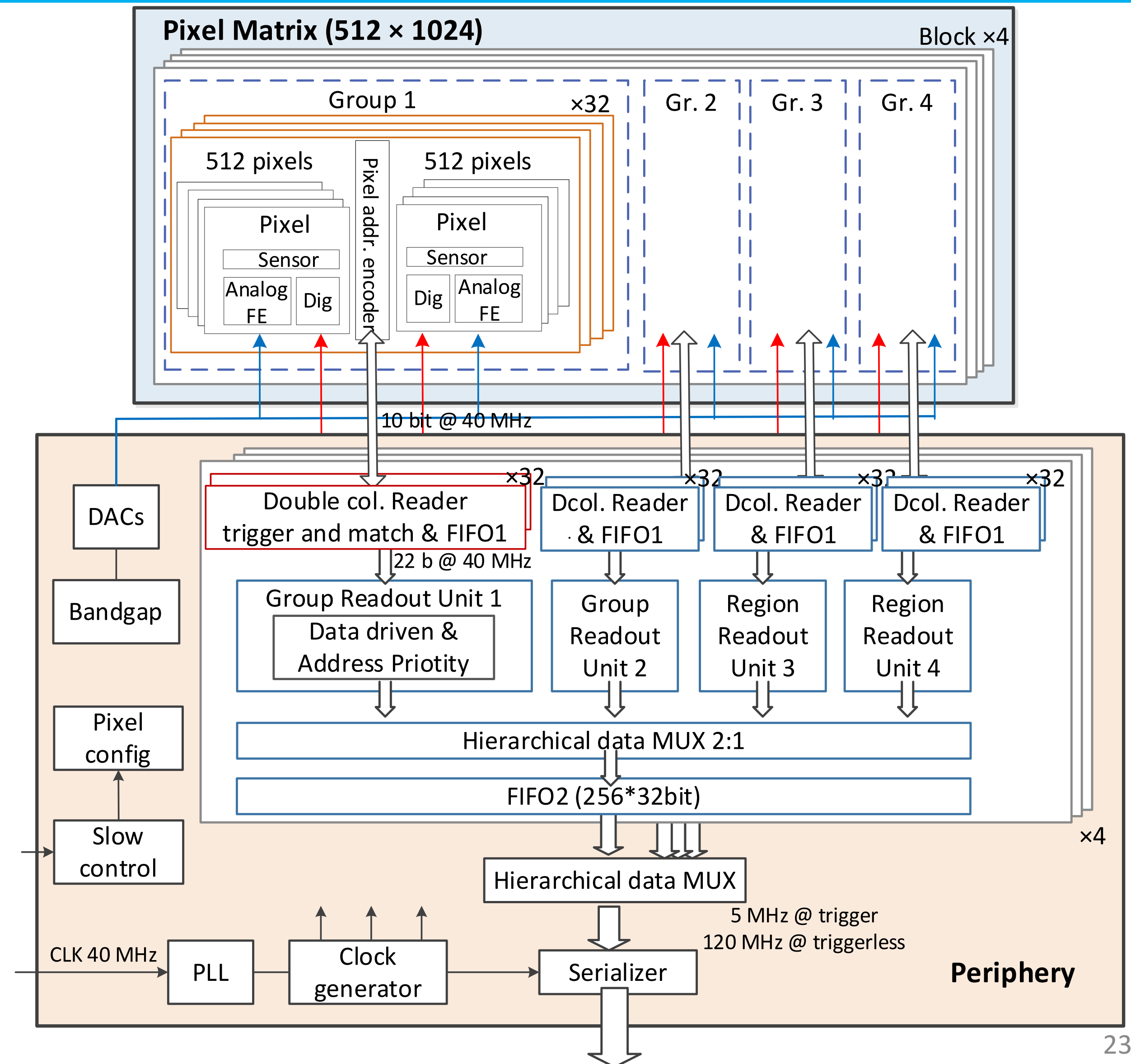
CPV4 (SOI-3D), 64×64 array
~21×17 μm^2 pixel size



Arcadia by Italian groups for IDEA vertex detector
LFoundry 110 nm CMOS

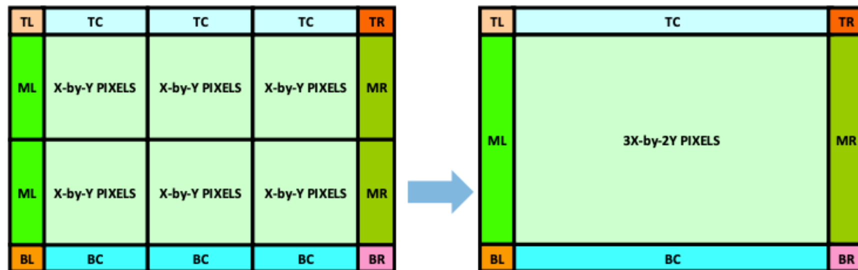
TaichuPix design

- Pixel 25 μm × 25 μm
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- Column-drain readout for pixel matrix
  - Priority based data-driven readout
  - Readout time: 50-100 ns for each pixel
- 2-level FIFO architecture
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- Trigger-less & Trigger mode compatible
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp
    only matched event will be readout
- Features standalone operation
  - On-chip bias generation, LDO, slow control, etc

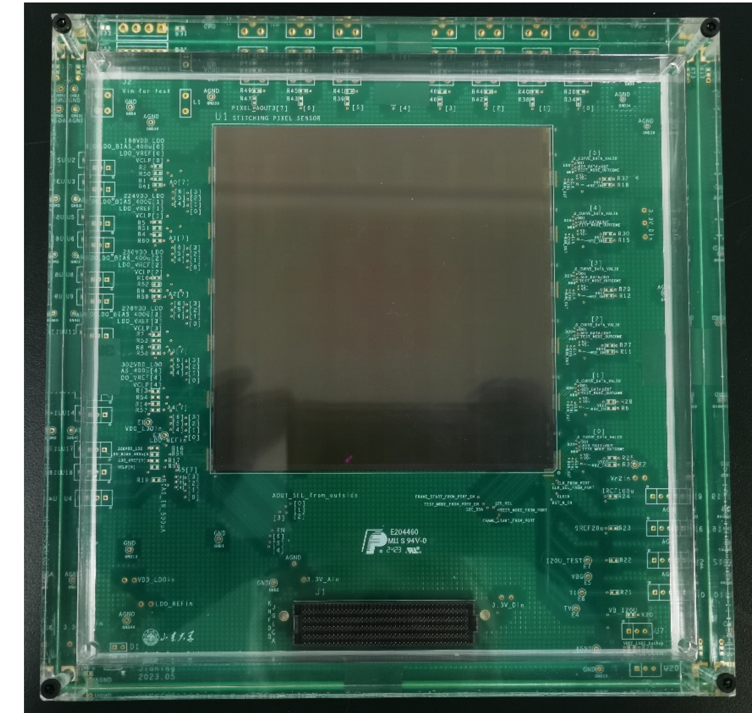


R&D efforts and results: R & D for curved MAPS

- Stitching chip design (by ShanDong U.)
  - 350nm CIS technology Xfabs
  - Wafer level size after stitching ~11 ×11 cm^2
  - reticle size ~2 ×2 cm^2
  - 2D stitching
  - Engineering run, chip under testing



Stitching chip : 11 ×11 cm^2



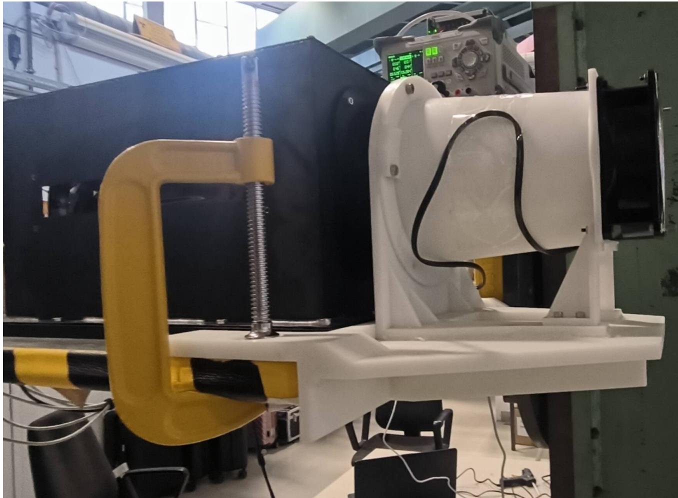
Key technology	Status	CEPC Final goal
Stitching	11*11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

R&D status and final goal

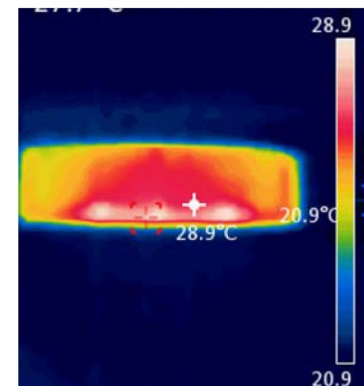
Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon design
Spatial resolution	4.9 μm	3-5 μm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm
Stitching	11×11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

R&D efforts: Air cooling in vertex prototype

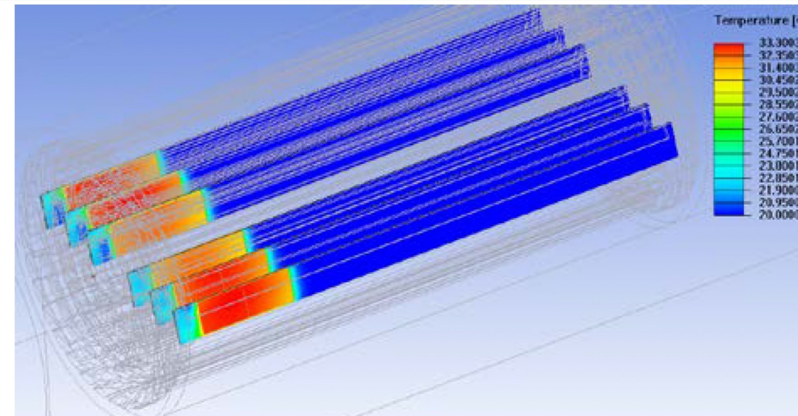
- Dedicated air cooling channel designed in prototype.
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm^2 (17.5 MHz in testbeam)
  - Before (after) turning on the cooling, chip temperature 41 °C (25 °C)
    - In good agreement to our cooling simulation
    - No visible vibration effect in spatial resolution when turning on the fan



Chip temperature under cooling during beam test: Max 28.9 ℃



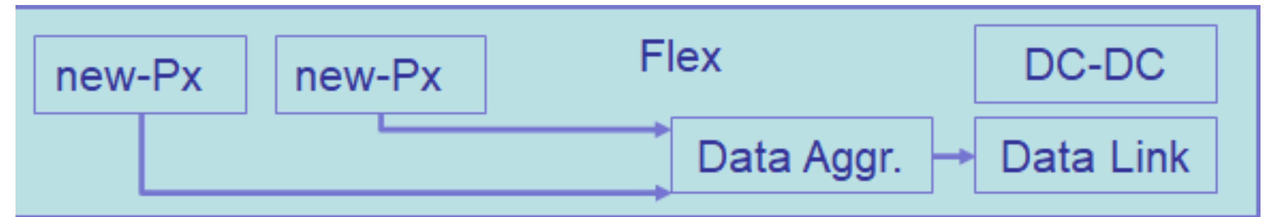
Prototype cooling simulation： Max 33.3 ℃

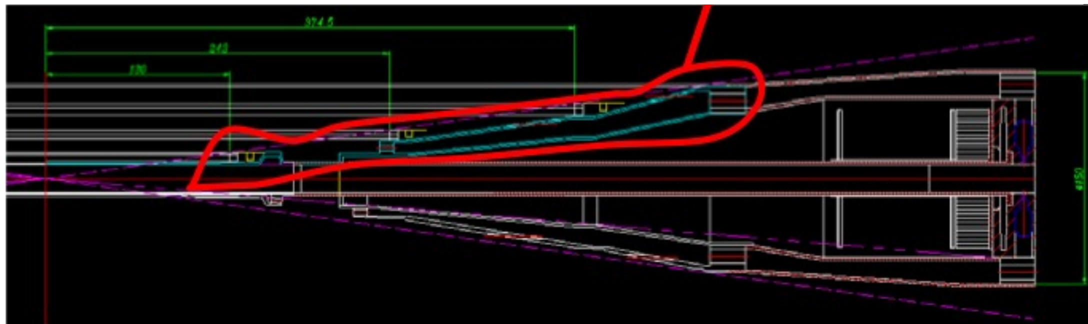


Key technology	Status	CEPC Final goal
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power

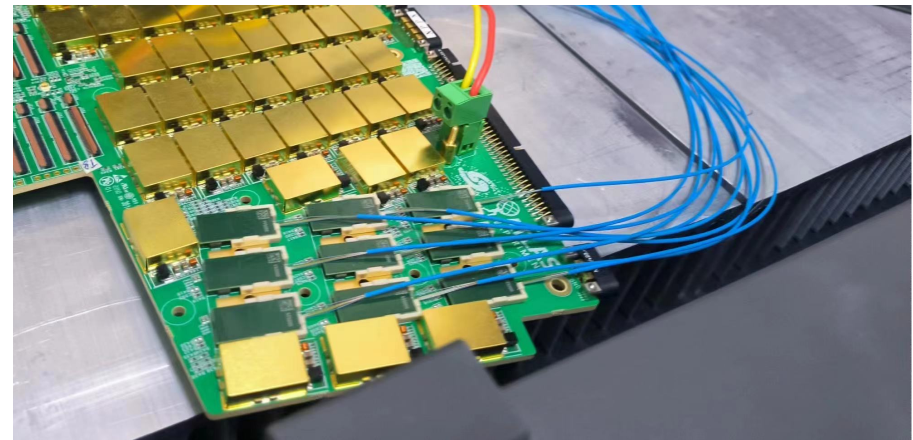
Vertex technologies: Cables and services

- Limited space in the MDI region for cables and services
  - Utilizes DC-DC powering; MAPS silicon substrate requires a common negative bias
  - Signal are transmitted through a flexible PCB and then converted to optical fiber.

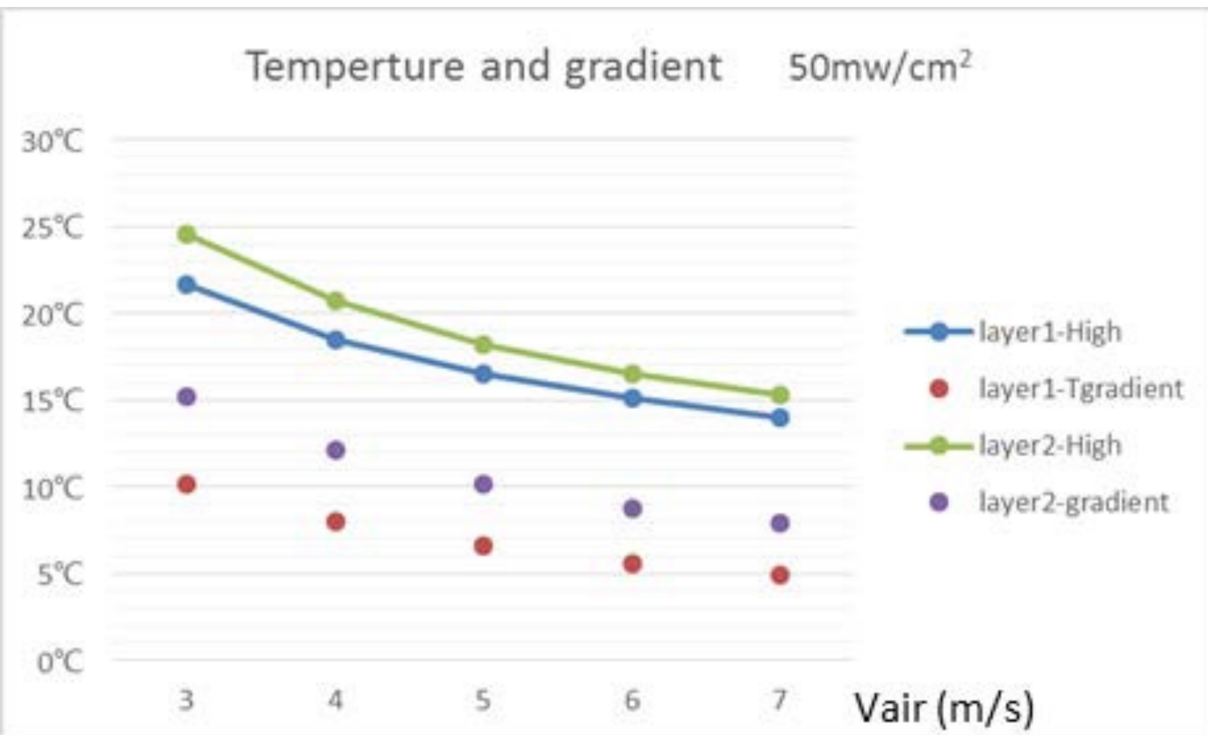


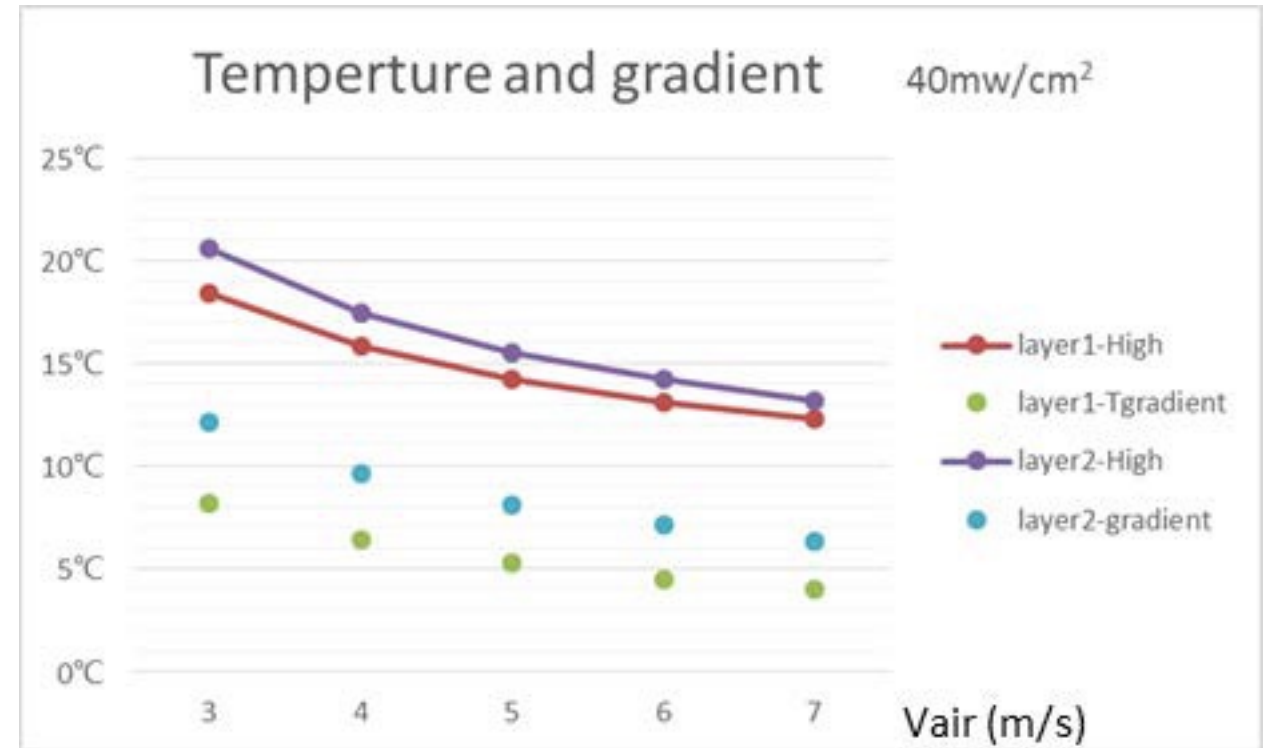


Example from ATLAS HGTD upgrade



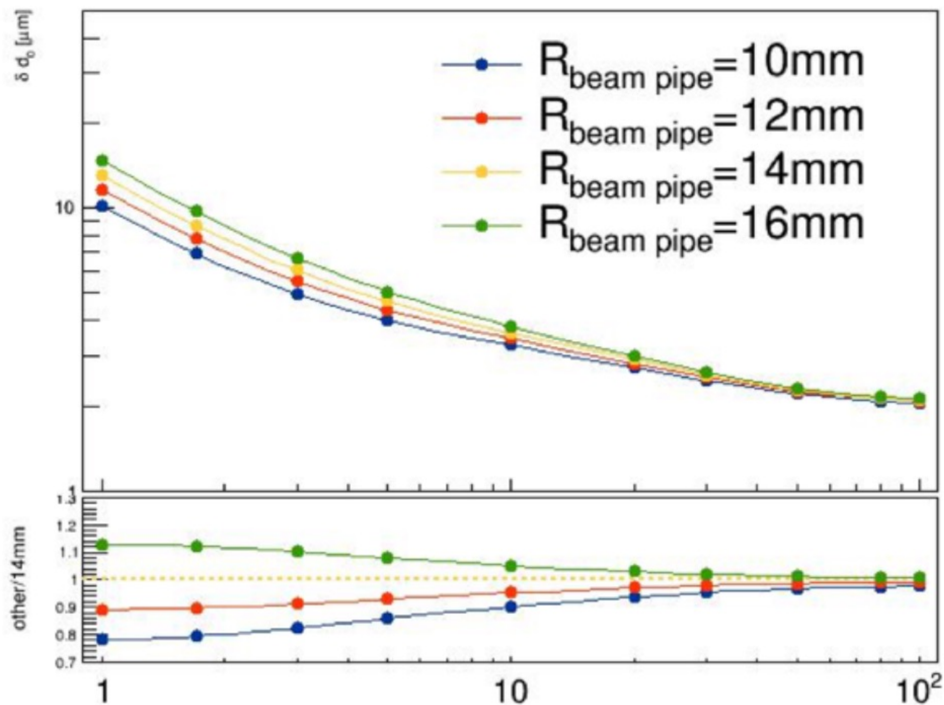
Backup : air cooling simulation

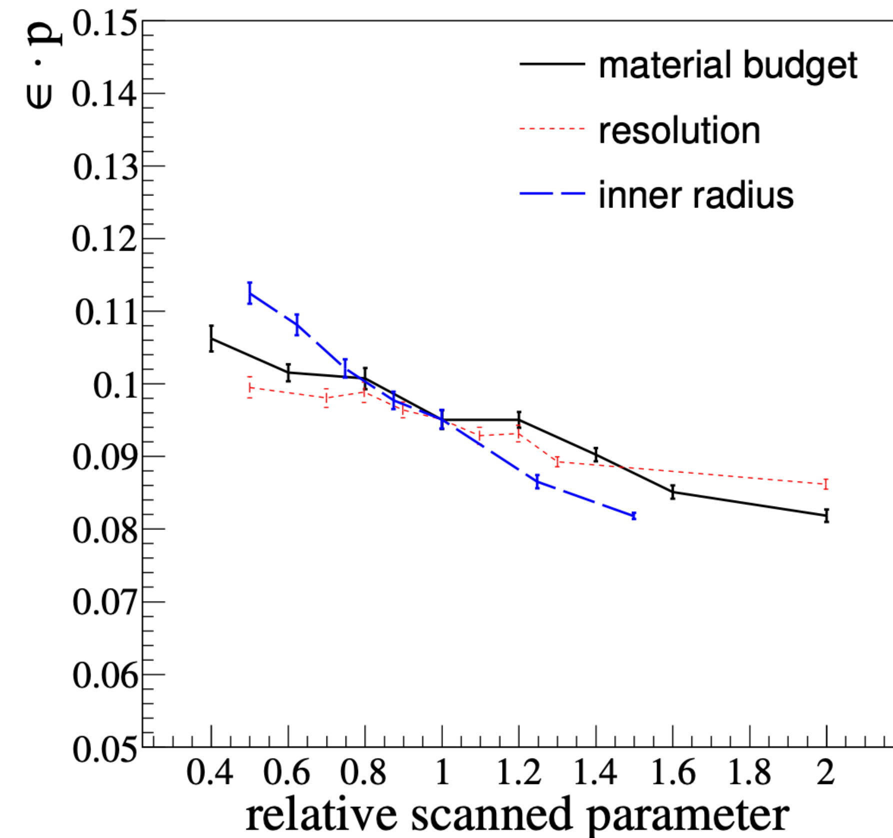




Vertex Requirement

- 1st priority: Small inner radius, close to beam pipe (11mm)
- 2nd priority: Low material budget <0.15% X0 per layer
- 3rd priority: High resolution pixel sensor： 3~5 µm

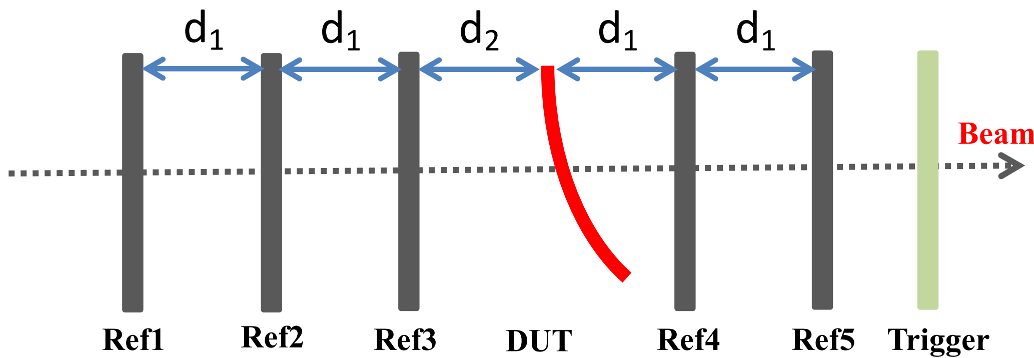


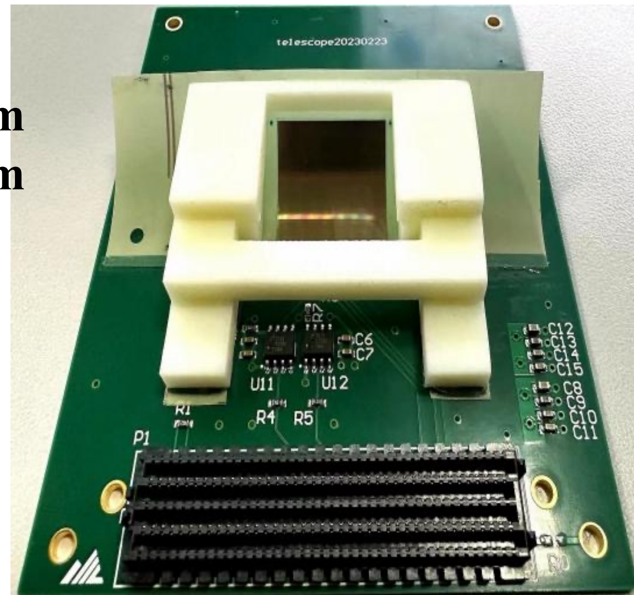


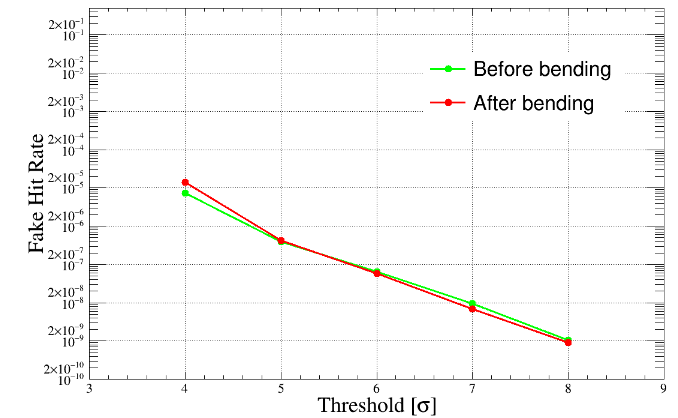
R&D efforts : Curved MAPS testbeam

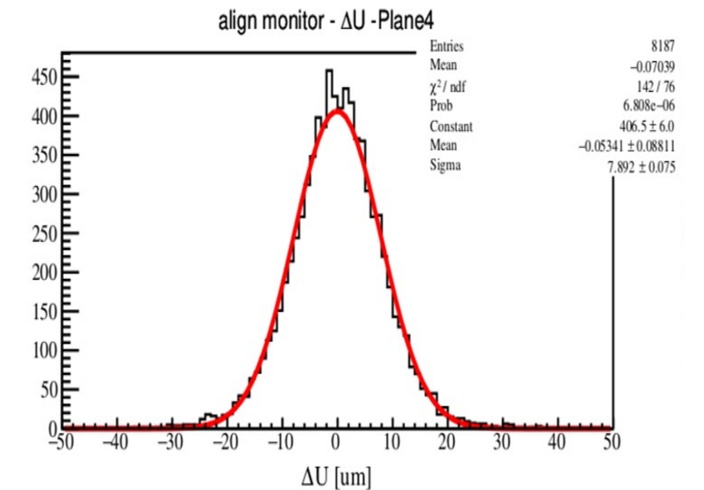
- R & D of curved maps with MIMOSA28 chip
  - No visible difference in noise level or spatial resolution before/after bending

d1 = 25 mm
d2 = 30 mm

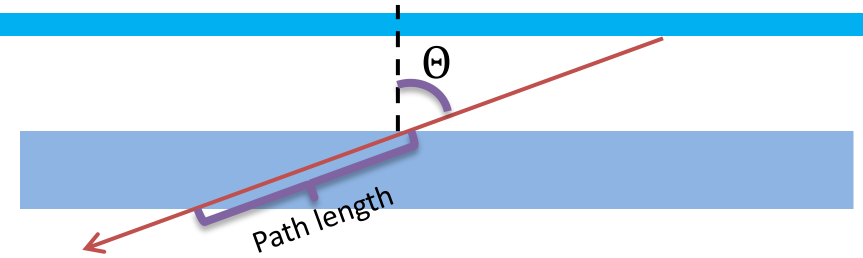




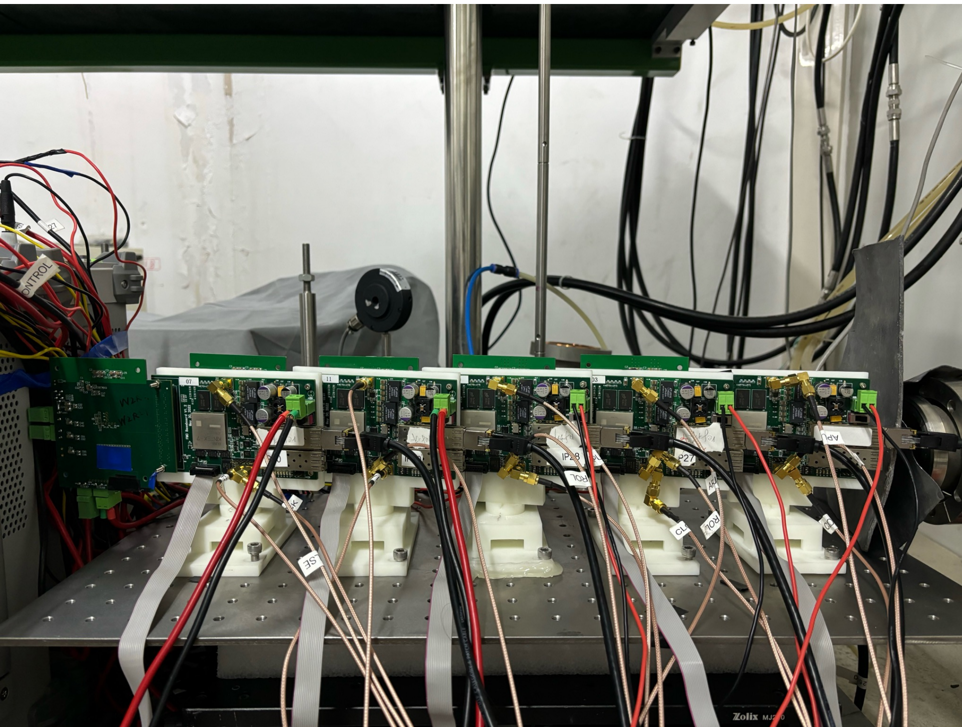




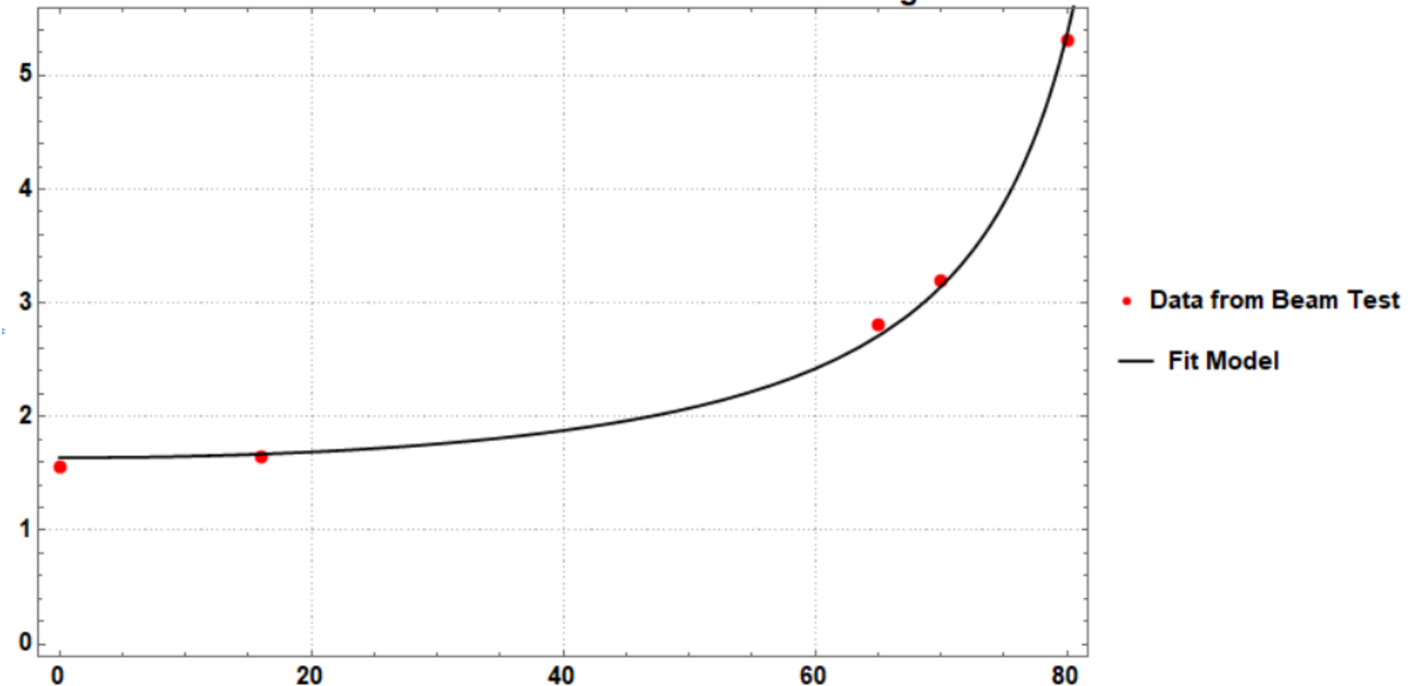
Long barrel : cluster size vs incident angle



Cluster size $= a \times sec\theta + b$



Cluster size



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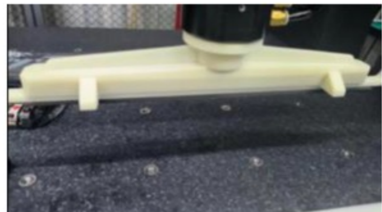
TaichuPix3 vertex detector prototype

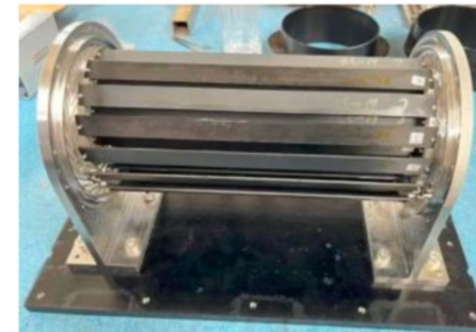
New pickup tools

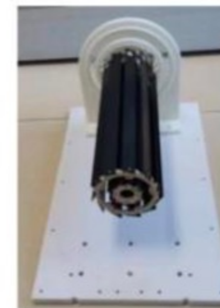


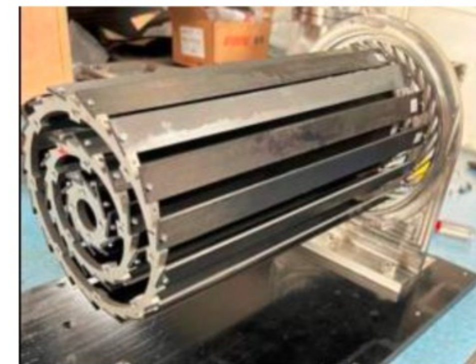
Dummy ladder glue automatic dispensing using gantry

Ladder on wire bonding machine

Dummy Ladder on holder







The first vertex detector (prototype) ever built in China

Ladder support tools

Ladder loaded on vertex detector

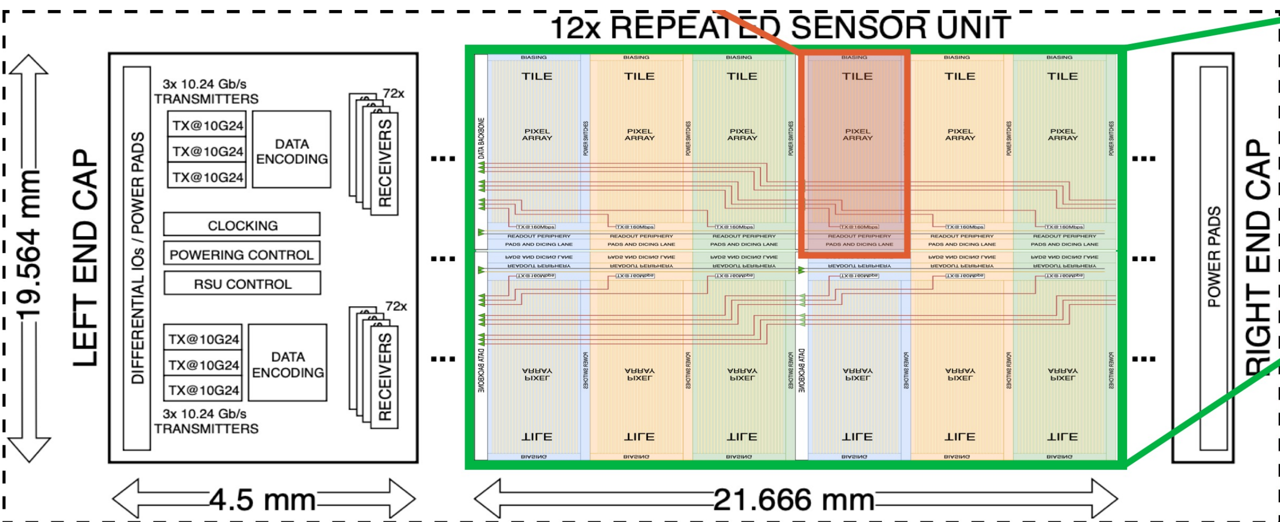
Ladder Electronics

– Baseline: stitching and RDL metal layer on wafer to replace PCB

– Alternative: flexible PCB

- Signal, clock, control, power, ground will be handled by control board through flexible PCB

Baseline: ALICE ITS3 like stitching



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

Alternative: flexible PCB

Ladder readout system

叠层 — Stack Up

	Thickness		Material					
	12.5	um	Coverlay (yellow)					
	20	um	Coverlay Adhesive			Soldmask (green)		
Layer 1	24	um	ED Base Copper	12	um	um +	Plated	18 um .
	13	um	Polyimide (Adhesiveless)					
	12.5	um	Adhesive					
Layer 2	12	um	ED Base Copper	12	um			
	25	um	Polyimide (Adhesiveless)					
Layer 3	12	um	ED Base Copper	12	um			
	12.5	um	Adhesive					
	13	um	Polyimide (Adhesiveless)					
Layer 4	24	um	ED Base Copper	12	um	um +	Plated	18 um .
	20	um	Coverlay Adhesive					
	12.5	um	Coverlay (yellow)					

Flex Thickness — 绕折区 — 补强区

FPC厚度: 213 um   Spec: 210 um   +/- 50 um

Created By: HLJ

Date: