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DRD3
WG2/WP2

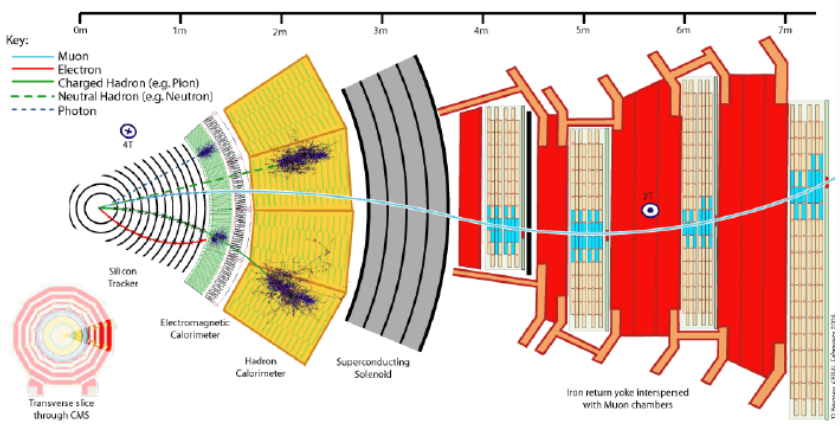
ASIC Development for Timing Measurements using LGAD Sensors

Abderrahmane GHIMOUZ

On the behalf of the HEP group

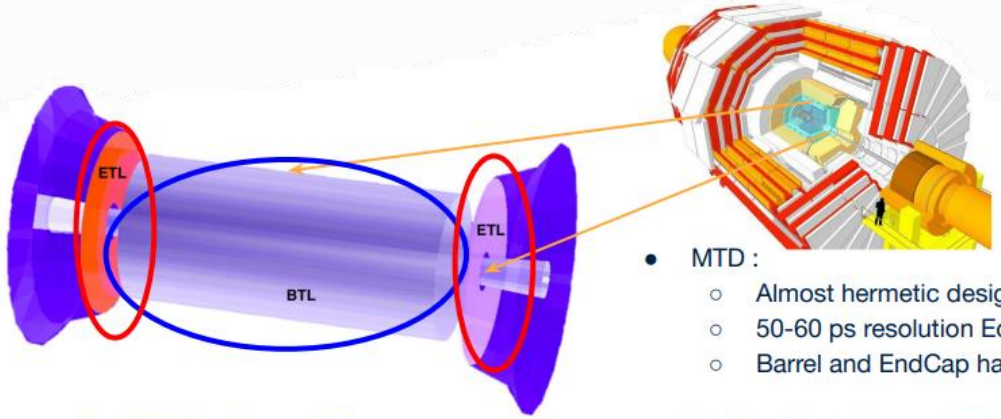
2nd Dec. 2024

Need for timing



The need for timing measurement with the CMS detector for the HL-LHC upgrade:

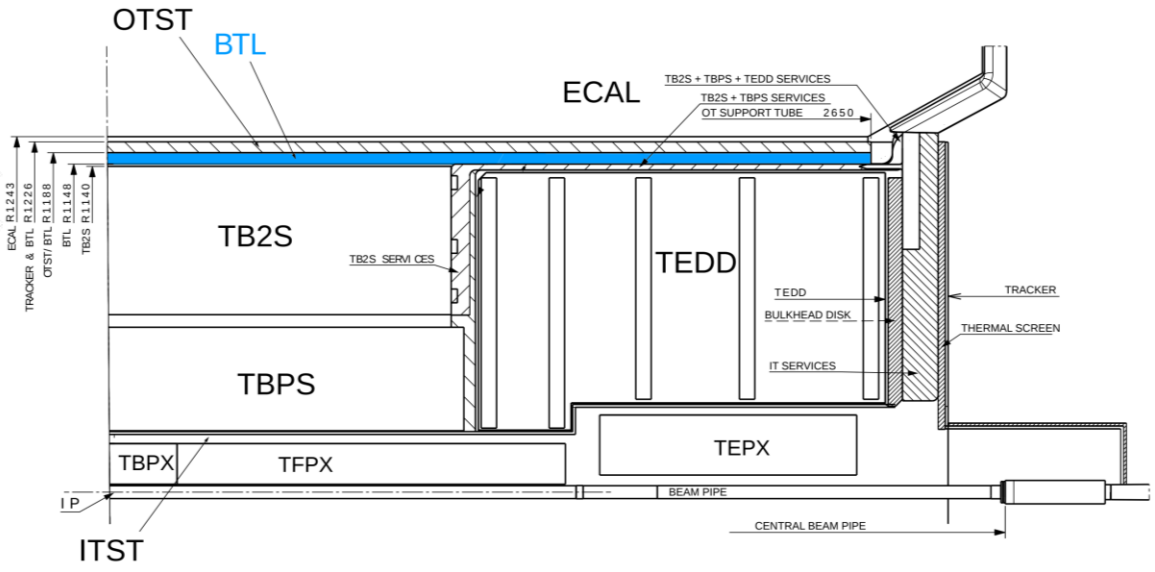
- **Pile-Up Mitigation**: achieves 30-40 picoseconds resolution to separate up to 200 overlapping collisions.
- **Particle Identification**: utilizes precise timing to distinguish particles with speed differences as small as 0.1%.
- **New Physics Sensitivity**: improves detection capability for rare events and particles beyond the standard model.



- MTD :
  - Almost hermetic design, $|\eta| < 3.0$
  - 50-60 ps resolution EoL
  - Barrel and EndCap have different needs

- Barrel Timing Layer - BTL :
  - Sensors: LYSO+SiPM
  - Inner radius: 1148 mm - 40mm thick
  - Length: ± 2.6 m
  - Fluence at 3000 fb^{-1} ~1.7x10^{14} n$_{eq}$/cm^2

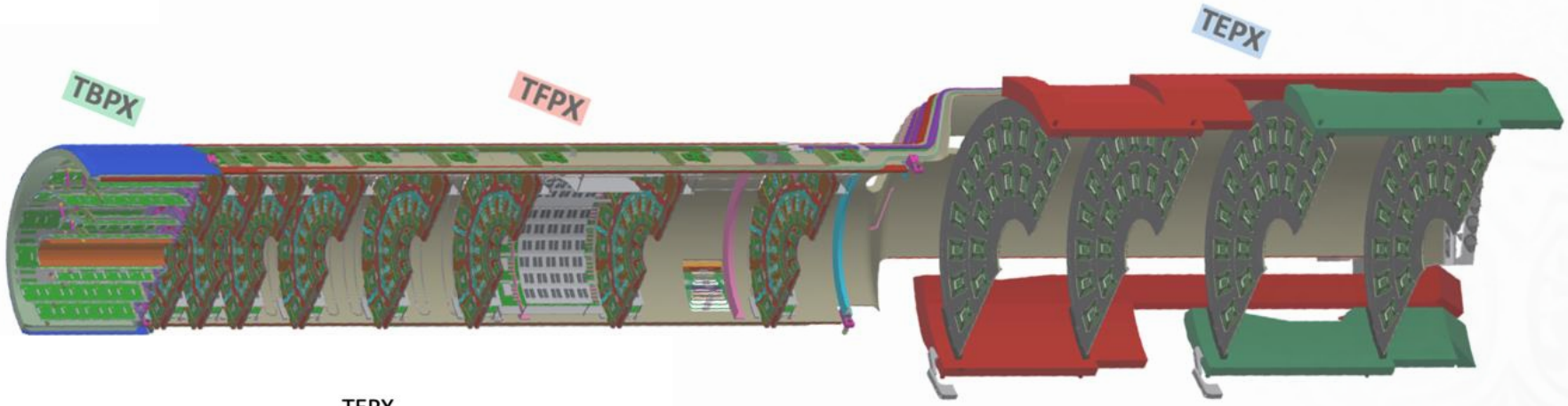
- EndCap Timing Layer - ETL :
  - Sensors: LGAD
  - Radius: 315 mm < r < 1200 mm
  - z-position 3.0 m - 45 mm thick
  - Fluence at 3000 fb^{-1} ~ 1.6x10^{15}n$_{eq}$/cm^2

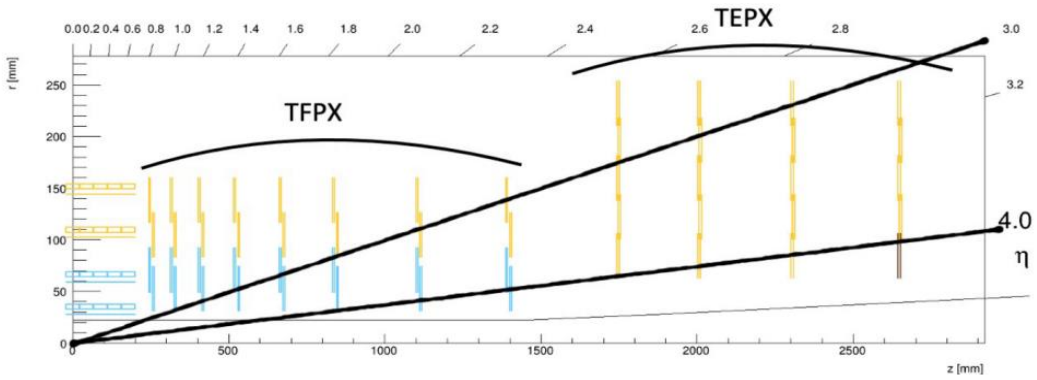


Credit : CMS CERN Collaboration

Need for timing

How to improve further ?





- CMS 'Phase 2' timing covers region up to $|\eta| = 3$ (BTL: LYSO + SiPM, ETL LGAD pads)
- possible extension to $|\eta| = 4$ in 'Phase 3': replacing 1 or 2 TEPX pixel disks with LGAD pixels

TEPX (Tracker Endcap Pixel)

- **Disks**: 4 per endcap (8 total)
- **Pixel Size**: 25 x 100 µm
- **Radial Coverage**: 60–300 mm
- **Longitudinal Position**: Up to ~2.7 m from the interaction point
- **Sensor**: Silicon pixel sensors
- **Readout**: RD53 chip, up to 750 Mb/s per module
- **Radiation Tolerance**: Up to 1.5 x 10^{16} neq/cm², 1 Grad

Credit : Dr. Wolfram Erdmann

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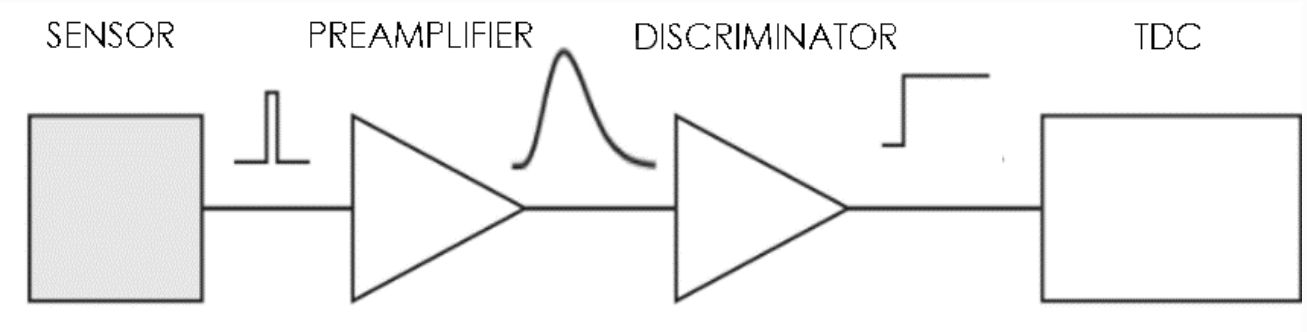
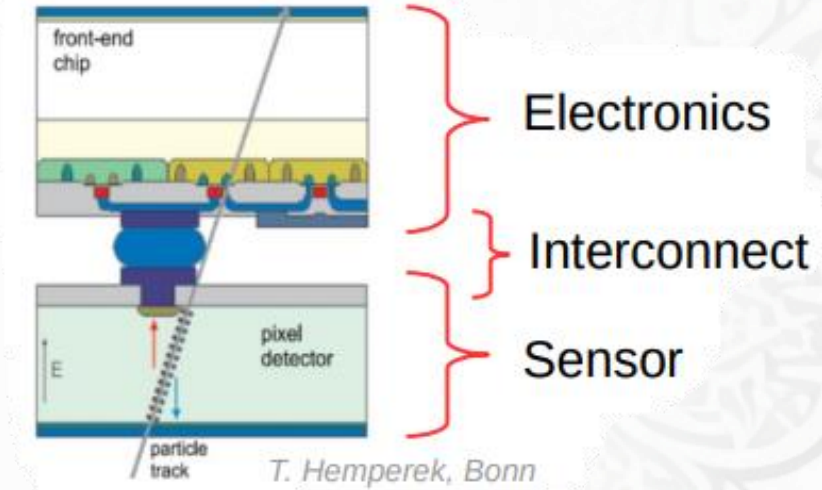
Context of the R&D

To **design** a readout **ASIC** targeting a future **CMS** upgrade. It should be capable of operating with **pixel** detectors based on **LGAD** technology. It is designed in a **28 nm CMOS** technology, for **timing** measurements.

Timing equation





Time resolution of a timing measurement Front End Electronics (FEE)

$$\sigma_t^2 = \underbrace{\sigma_{\text{Landau}}^2 + \sigma_{\text{Distortion}}^2}_{\text{To understand (characterization)}} + \underbrace{\sigma_{\text{Timewalk}}^2 + \sigma_{\text{TDC}}^2 + \sigma_{\text{Jitter}}^2}_{\text{To model and optimize (FEE architecture)}}$$

R&D details

Part 1
LGAD Sensor

- Sensor performance;
- Sensor characterization;
- System requirements.

Part 2
Behavioral modeling

- Model based design using MATLAB® Simulink®;
- Sensor model;
- Architecture of the system;
- Performance of each building block.

Part 3
28nm IMPLEMENTATION

- Technology performance;
- Design methodology;
- ASIC design
- 28nm CERN Community.

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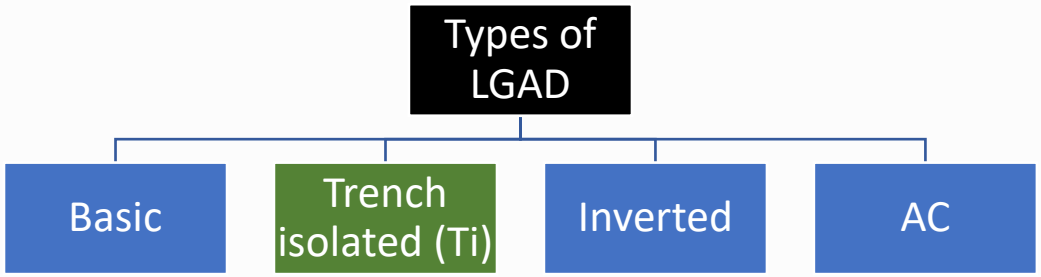
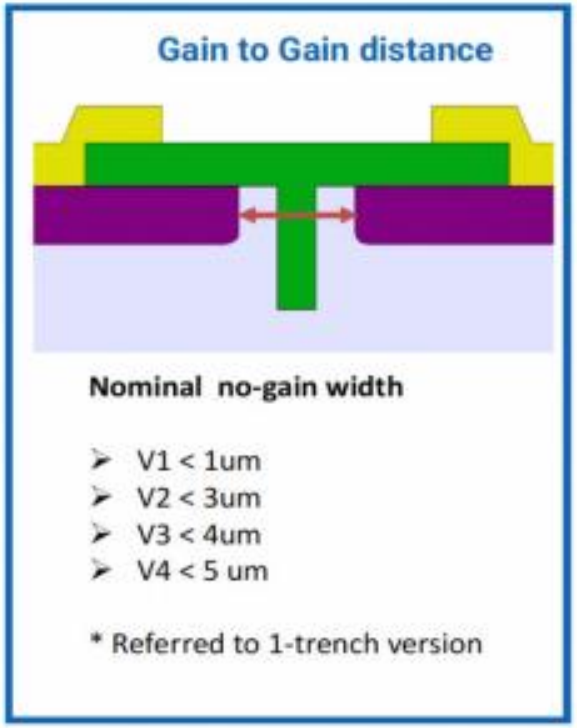
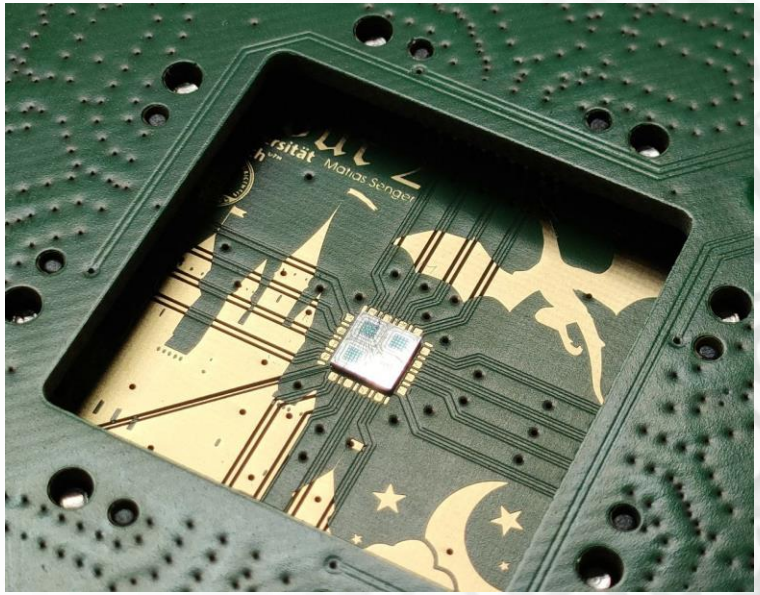
Part 1
LGAD Sensor

Type of LGAD sensors : Ti-LGAD







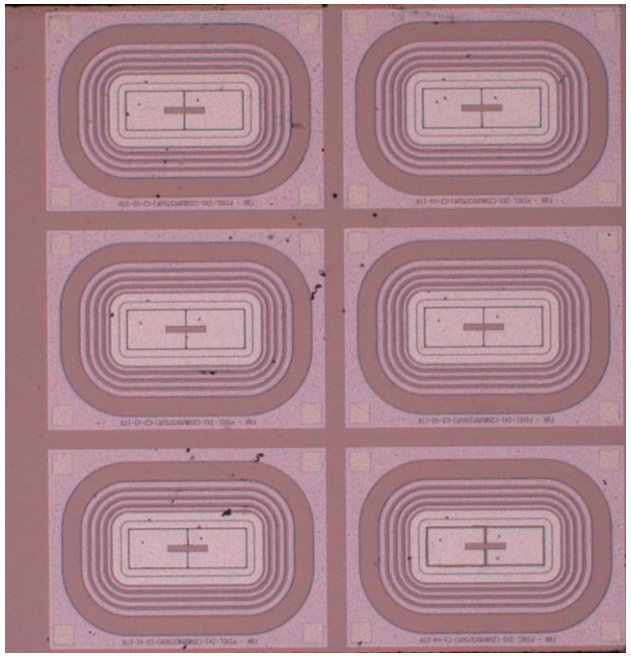
Credit : Matias Senger

Collaboration with the University of Zurich

Part 1
LGAD Sensor

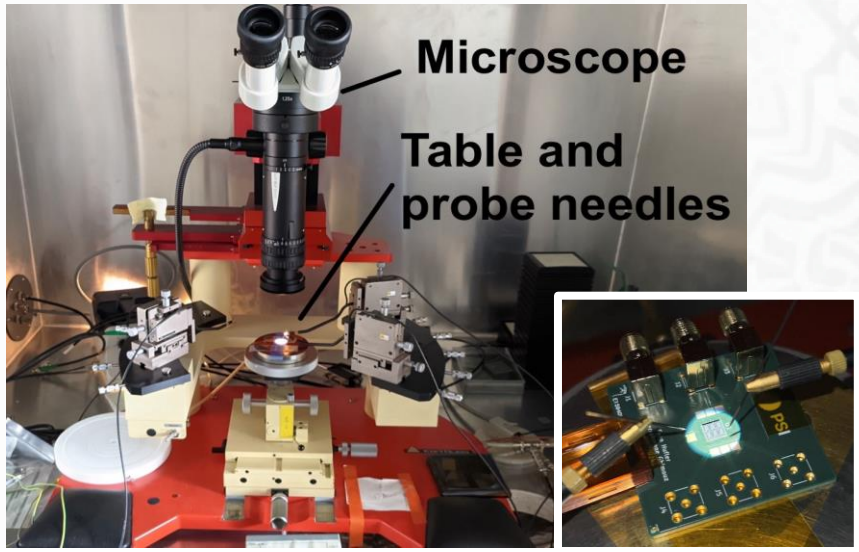
Characterization of Ti-LGAD sensors (setup)

ETHZ Student project (Fynn Hufler)

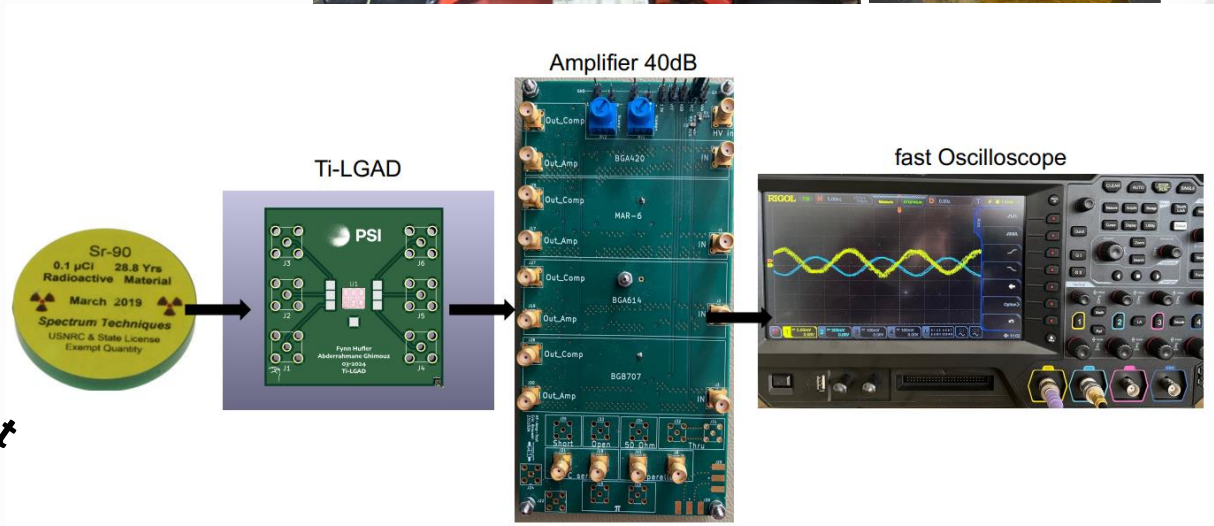


Ti-LGAD sensor sample

Capacitance measurement



Signal measurement



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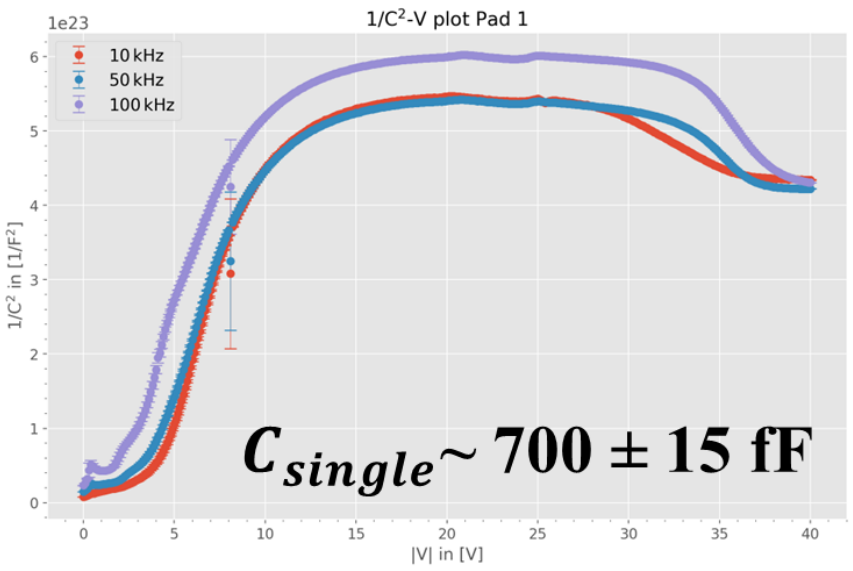
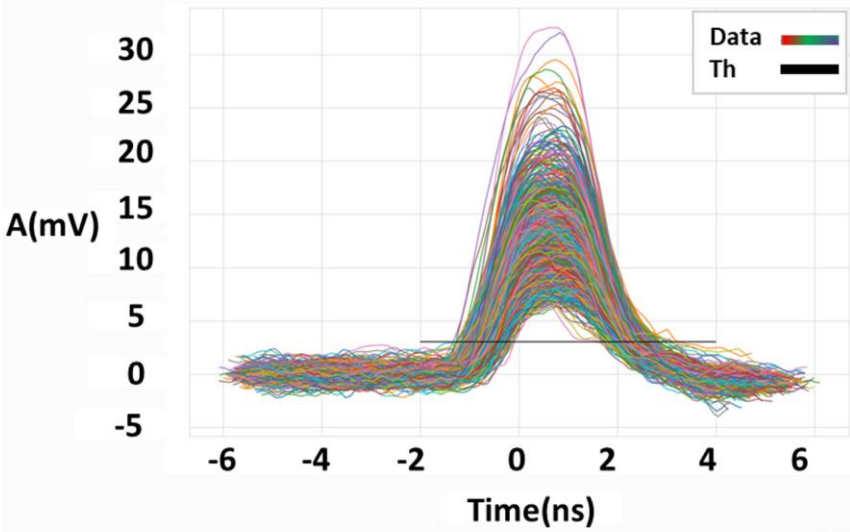
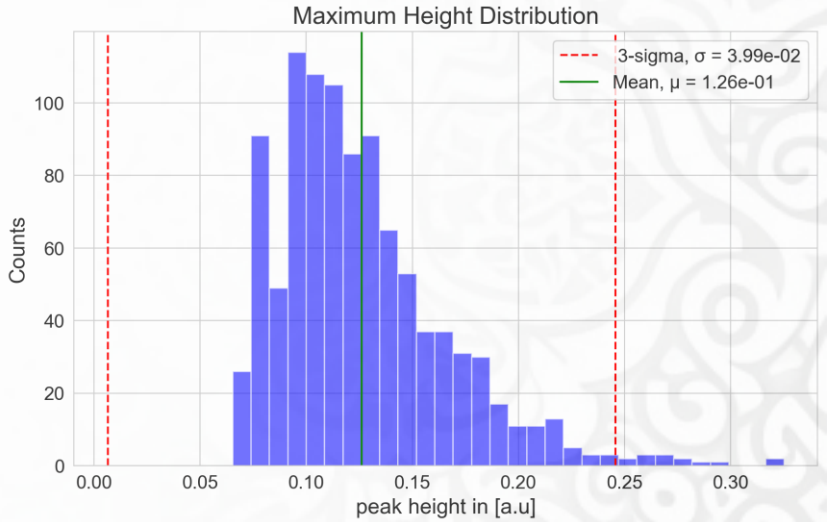
Part 1
LGAD Sensor

Characterization of Ti-LGAD sensors (results)

ETHZ Student project (Fynn Hufler)







- ✓ Capacitance measurements of Ti-LGAD sensors showed **uniform values** with stable performance across **conditions** and mean capacitance for single pixels between **0.63 - 0.70 pF.**
- ✓ The expected **features** of the generated signals were **confirmed**.

Advanced Characterization of other sensors starting soon

Part 1
LGAD Sensor

System requirement

Property	Value
Pixel size	100 x 100 μm^2
Input capacitance	~ 0.5 pF (including parasitic)
Time res RMS	30 ps
Max latency	500 KHz to 1 MHZ per pixel
Max dead time	< 250 ns
Total power density	1 W/cm2
Threshold level	1000 e^-
Dynamic range (Q)	Equivalent 1000 e^- to 100 Ke^-
Pixel rate at hottest pixel	50 KHz

State of the art study to propose different solutions

- Defining the specifications of the preamplifier;
- Defining the technique to measure time;
- Testing the resolution limit of the selected solutions;
- Integrating error corrections;

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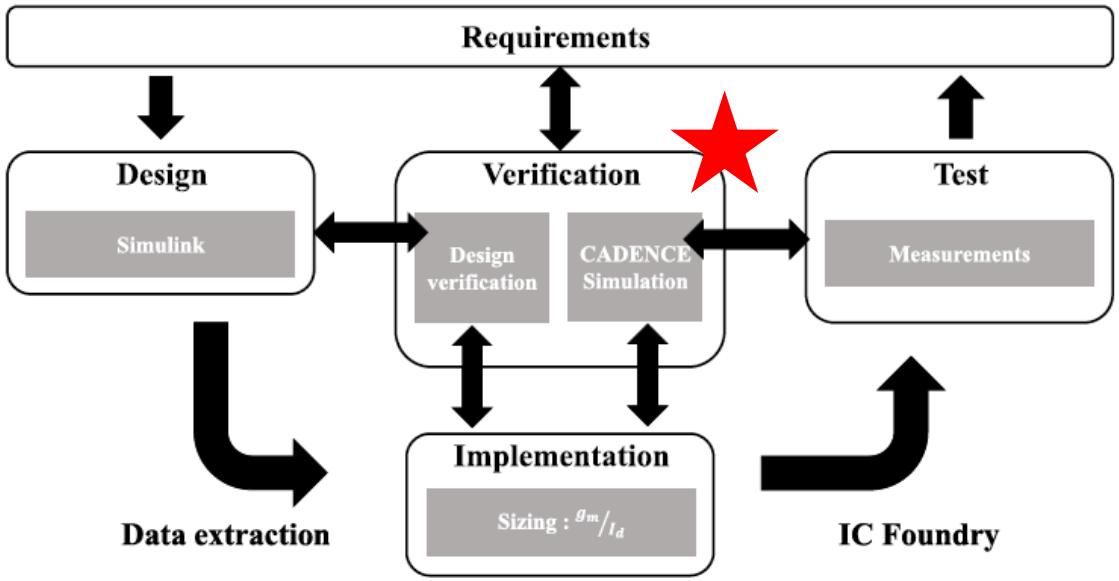
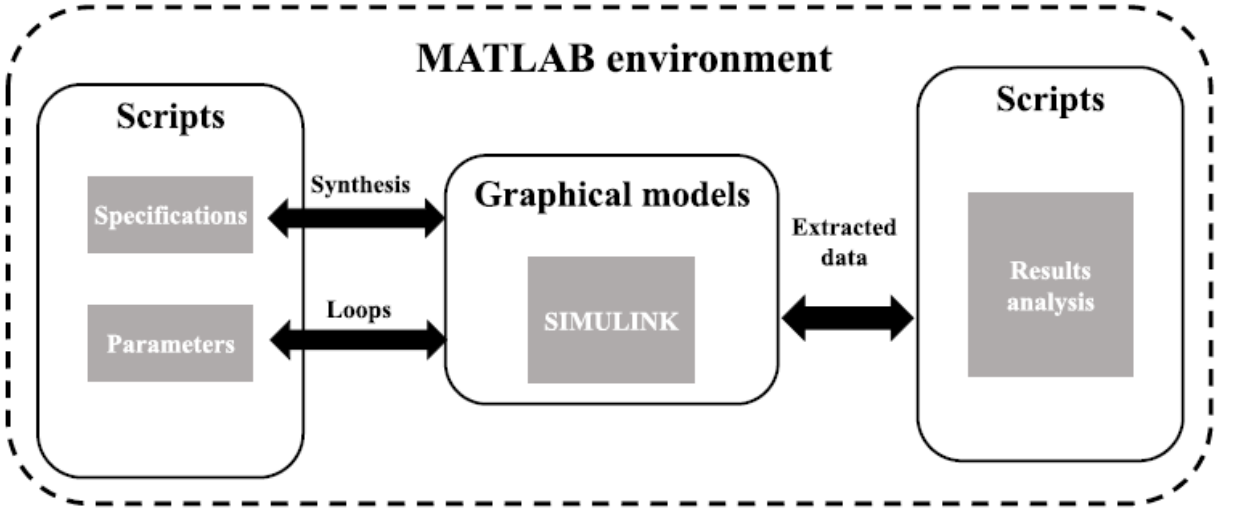
Part 2
Behavioral modeling

Model Base design concept



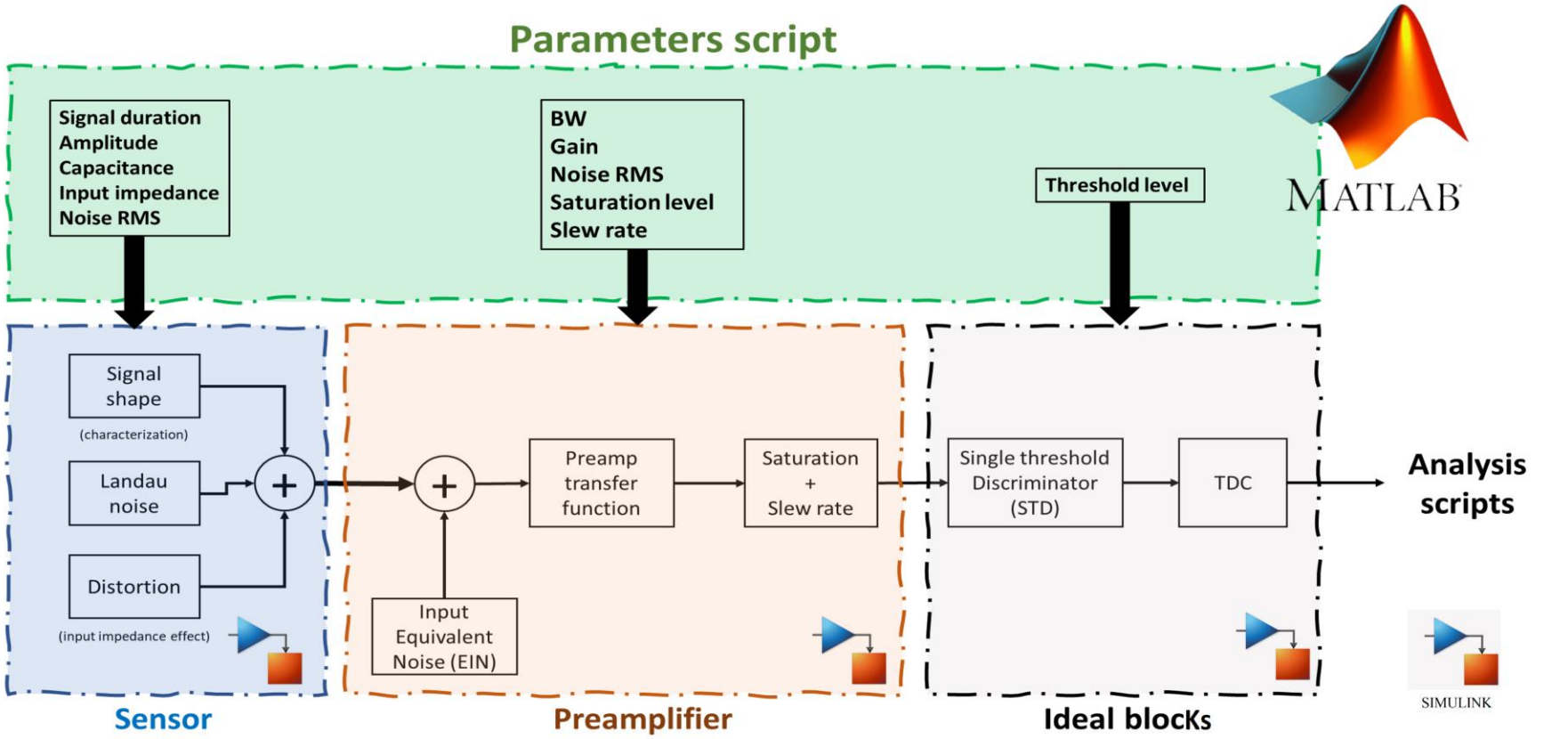


★ **Integration with PixESL framework flow**
Davide Ceresa

Defining the best parameters to achieve the desired specifications with efficiency using the model-based design approach: implementation in MATLAB® for ASIC design.

Part 2
Behavioral modeling

Implementation in MATLAB® SIMULINK ®



In this first step, we focus on studying the effect of the key parameters of the preamplifier on the timing resolution (few Ke^-signals) using an ideal Discriminator and TDC. The integration between the sensor and the preamp is modeled as well.

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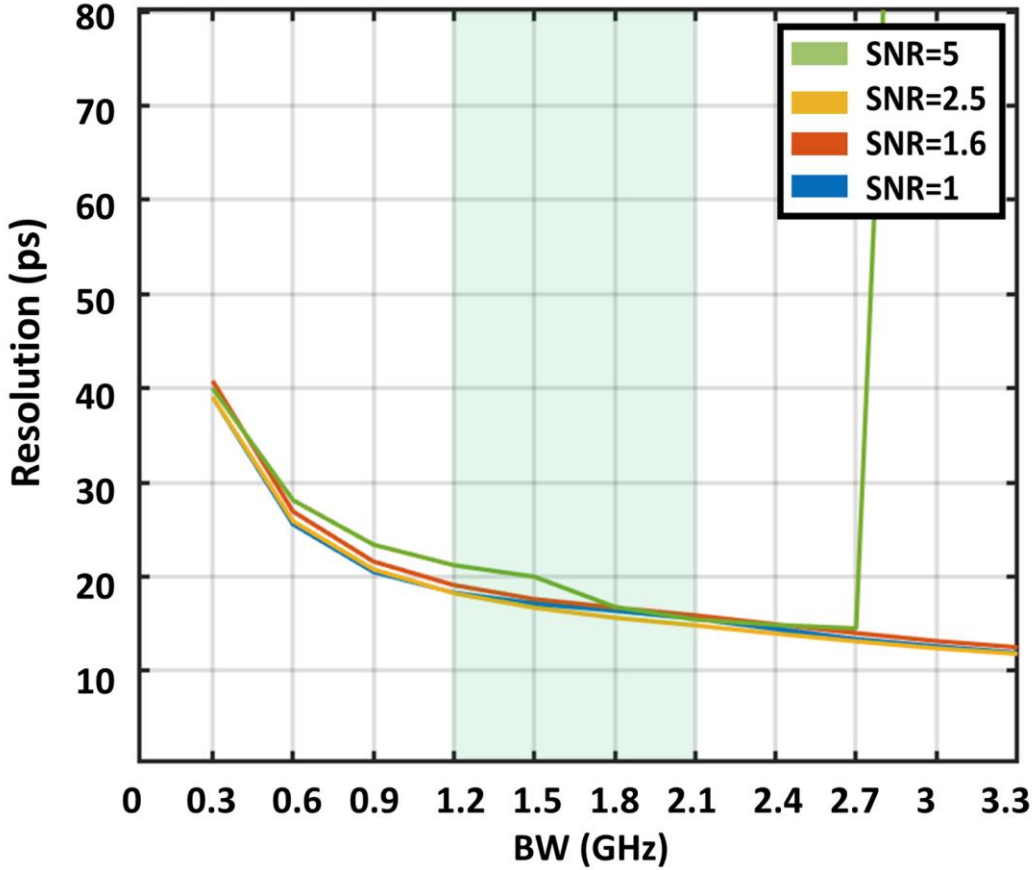
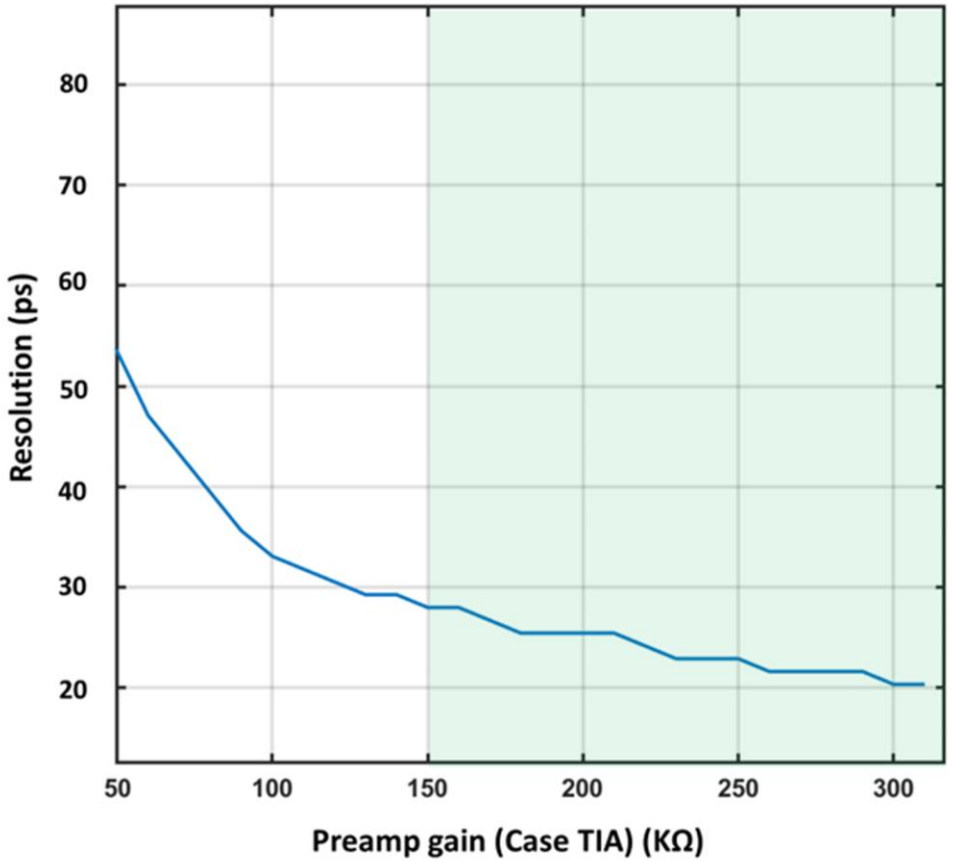
Part 2
Behavioral modeling

Results of the modeling of sensor + preamp stage

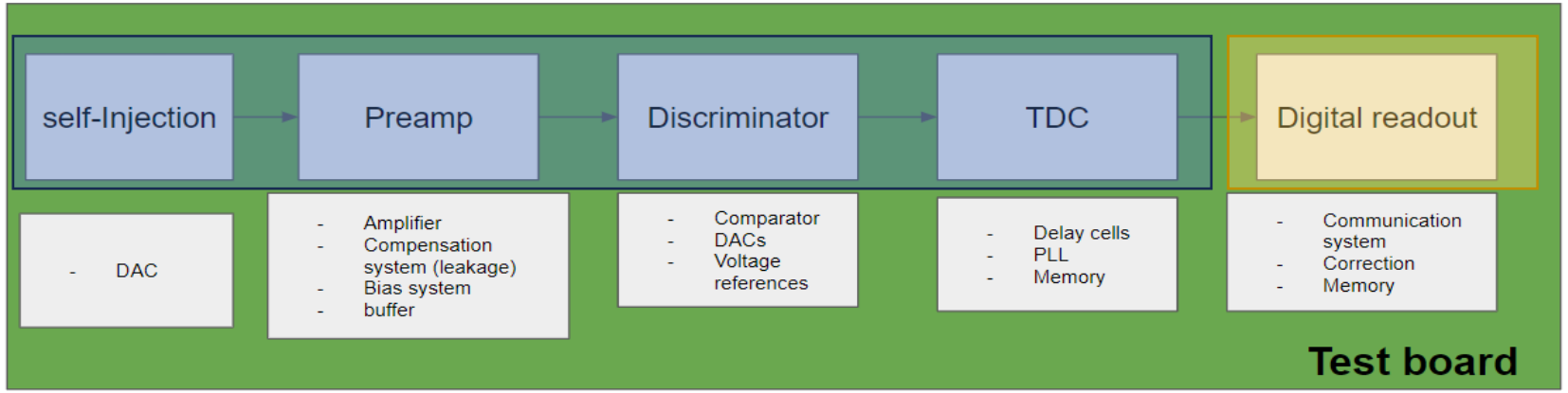




Ghimouz, A. (2024). R&D of a timing measurement ASIC for possible HL-LHC upgrade. *Nuclear Instruments and Methods in Physics Research Section a Accelerators Spectrometers Detectors and Associated Equipment*, 169802. https://doi.org/10.1016/j.nima.2024.169802

Part 3
Goal

The concept of the targeted ASIC



The ***First Gen*** of the proposed ASIC is aimed to test different flavors and timing measurement concepts.
It is designed to be integrated with the Ti-LGAD sensors (Hybrid configuration).

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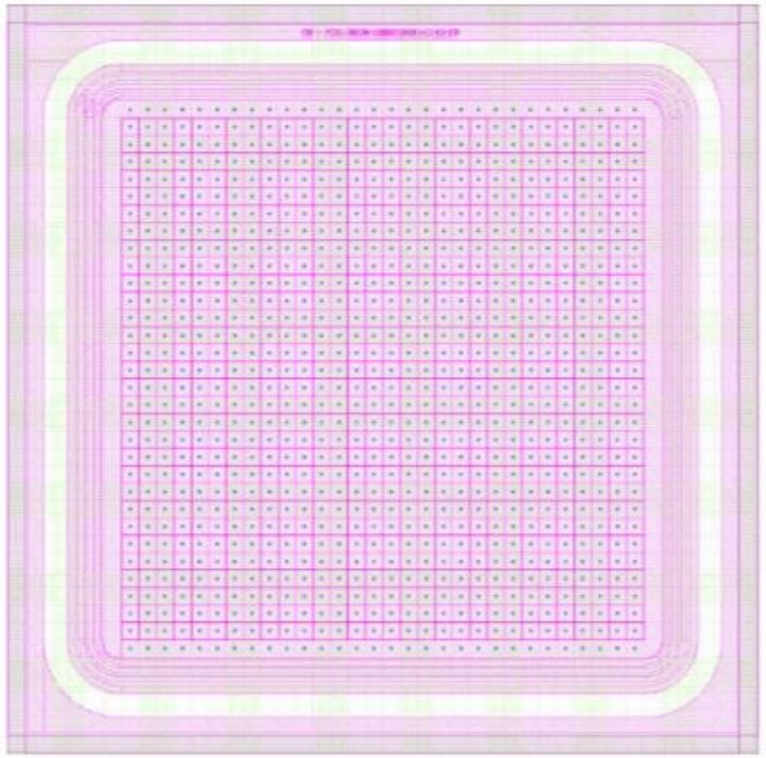
Part 3
Goal

Details about the first Gen ASIC (Current status)



Credit : Anna Macchiolo

- **64 Channels in 8x8 Pixel Array**
- **Full Readout Capabilities (multi-flavour):**
  - Different preamplifier topologies
  - Multiple TDC designs
  - Integrated calibration system
  - Test structures
  - Utilization of specific IPs from the 28nm forum library (Process initiated)
- **Bump-Bonding to Ti-LGAD Sensor (From UZ):**
  - Sensor configuration: 30x30 pixel array
  - Pixel dimensions: 100 x 100 μm^2
- **Project Status:**
  - Target submission date: May 2025
  - Design effort: 2.5 FTE at PSI
  - Expected team expansion through collaborations with interested groups

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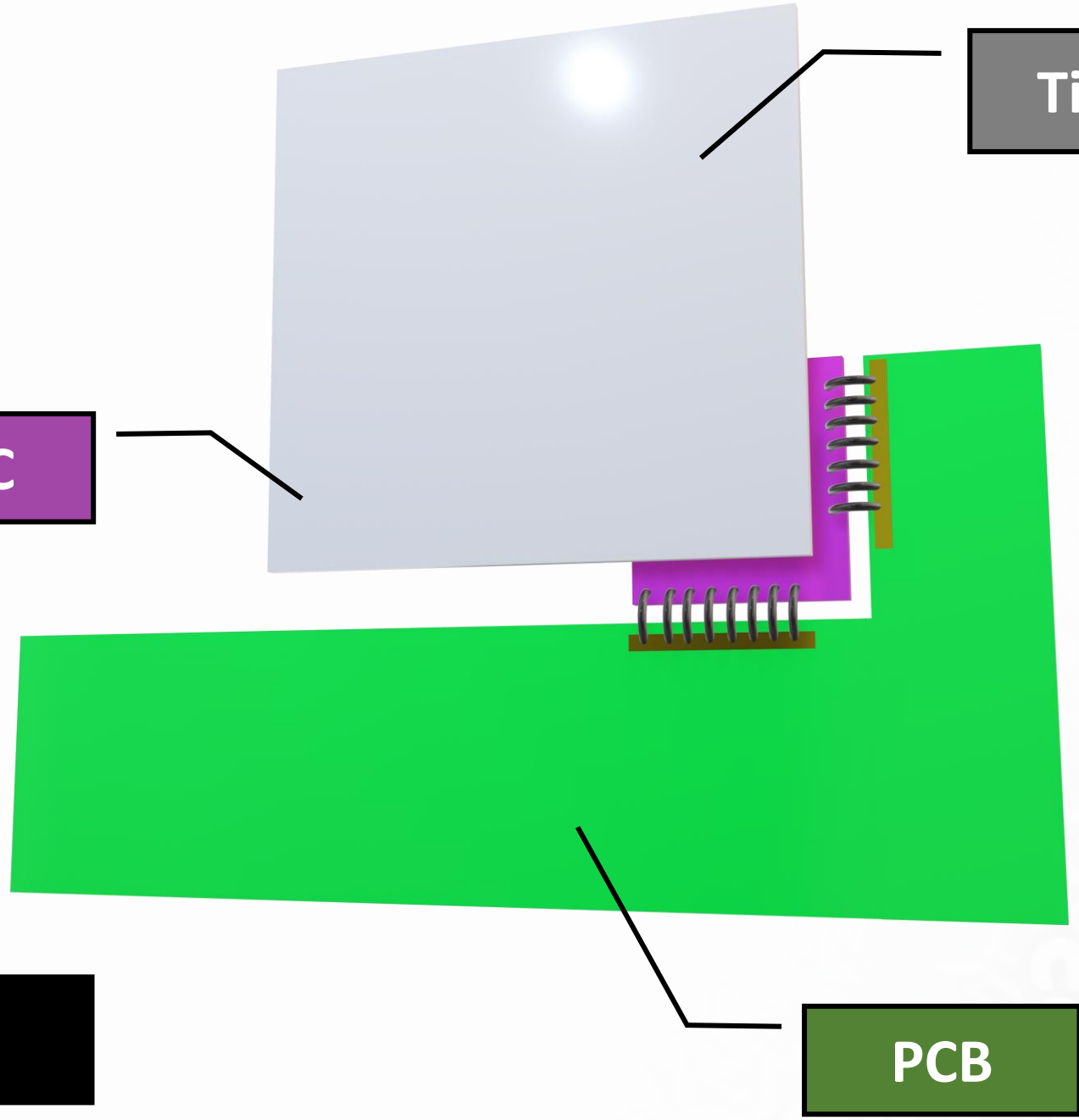

Implementation

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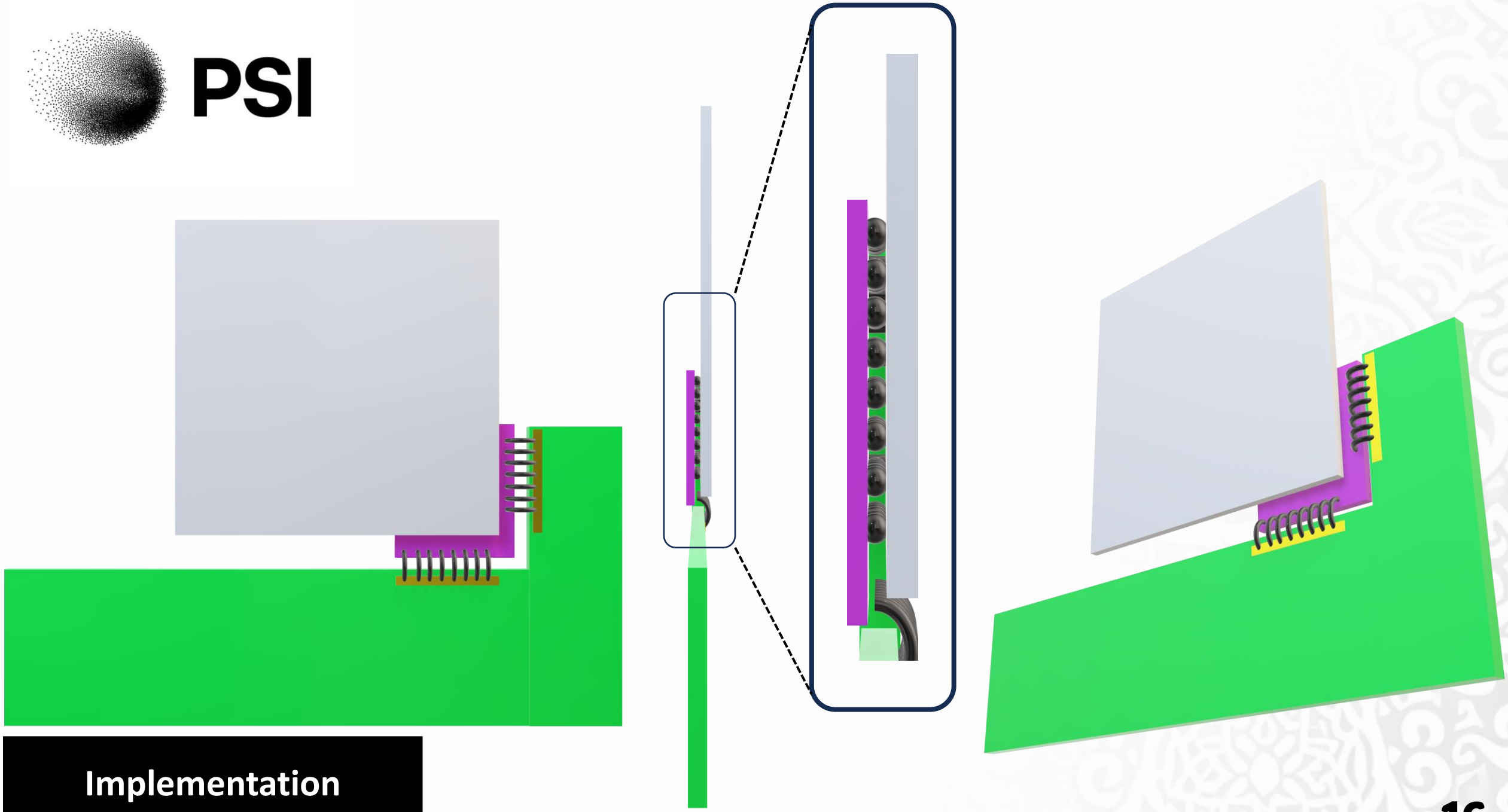
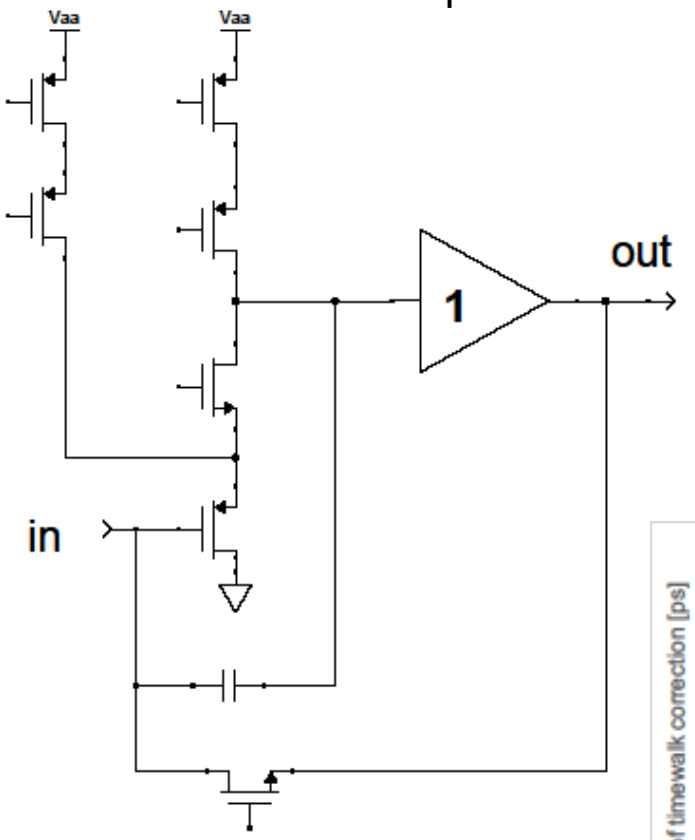


Implementation

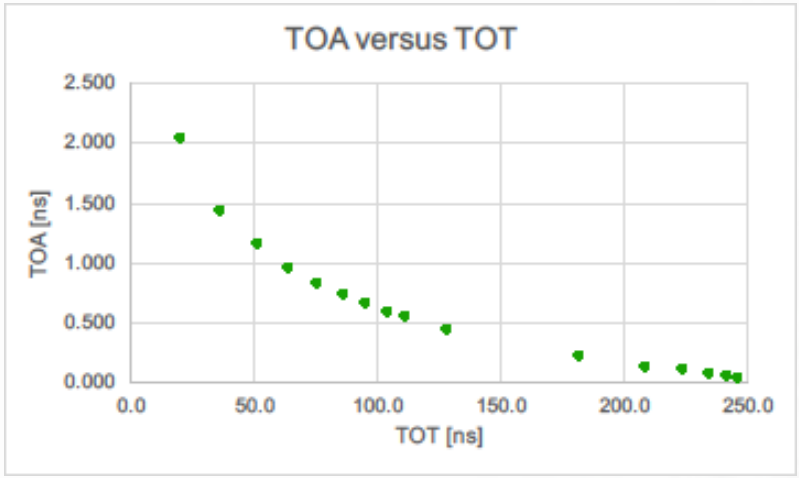
Part 3
Preamplifier

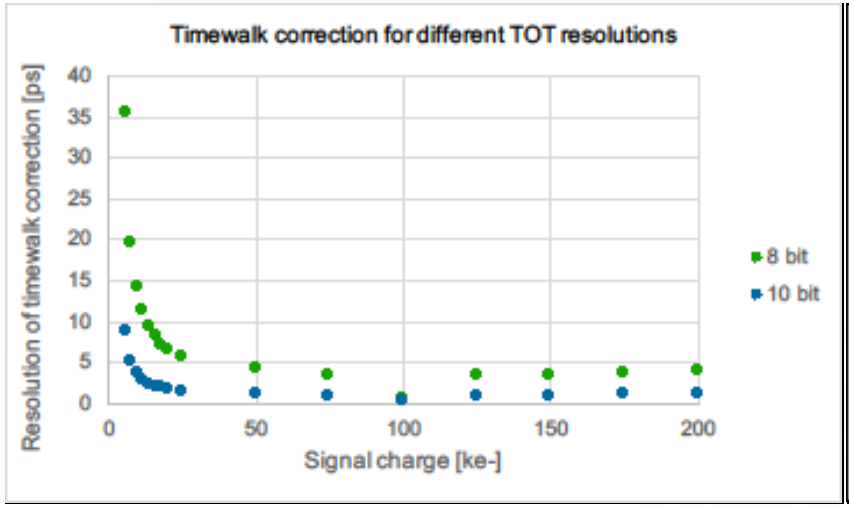
First flavour CSA (Hans-Christian Kaestli)

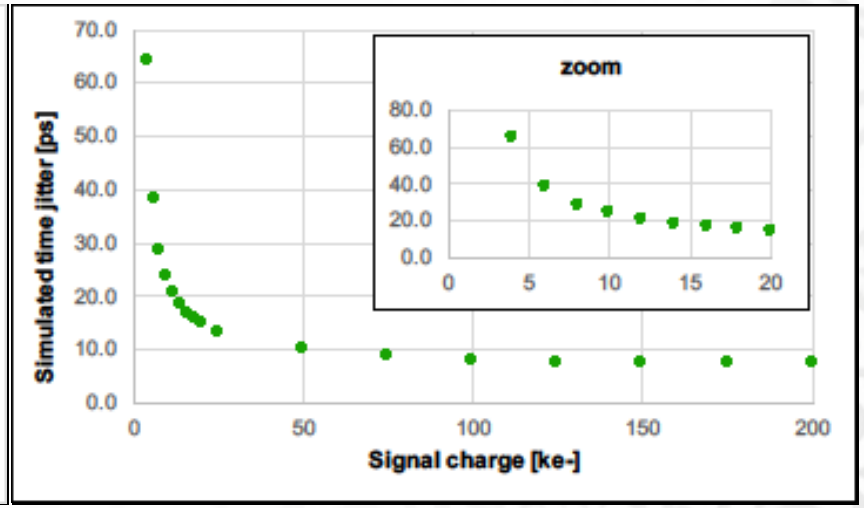
Concept



Initial post-layout simulations results







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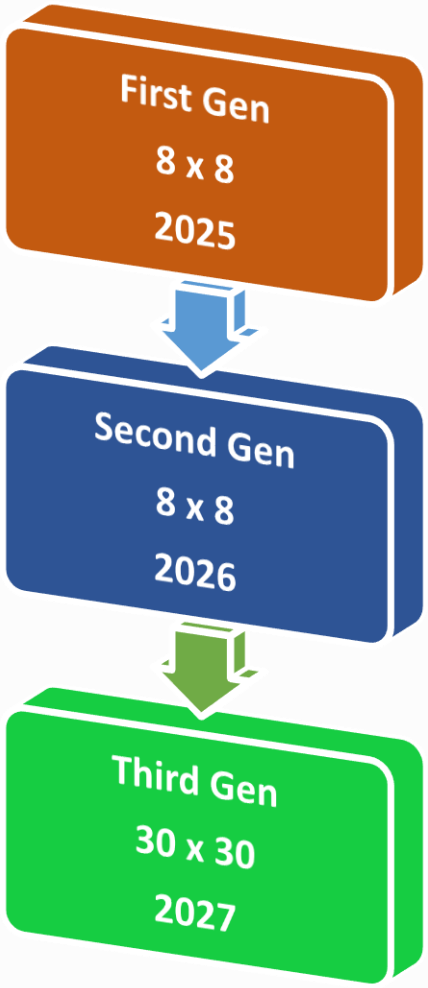
Part 3
timeline

Details about the ASIC (Future plan)



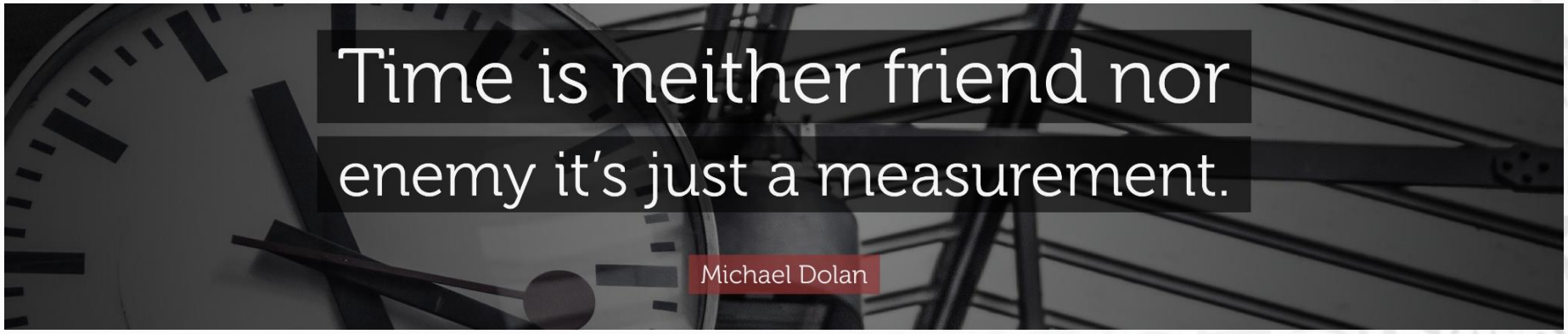
- **First Generation**
  - Validate the selection of **optimal topologies**
  - Assess performance of the current **design methodology**
  - Test initial sensor integration with **bump-bonding**
  - Evaluate performance under **beam** conditions
  - Characterization of **the sensors**

- **Second Generation**
  - Optimize ASIC with chosen topologies for each block
  - Optimize the readout using the **PixESL framework.**
  - Improve bump-bonding integration with the sensor
  - Evaluate performance under beam conditions
  - Characterization of the sensors

- **Third Generation**
  - Develop full **30x30 channel ASIC**
  - Optimize power efficiency and readout performance
  - Finalize bump-bonding with the complete sensor
  - Evaluate performance under beam conditions
  - Characterization of the sensors

Conclusion

- **The Initial system specifications are confirmed** ➔ A multiflavored, multichannel chip is under development.
- **The Behavioral Model is continuously evolving** ➔ Studying multiple solutions to reach the timing requirements ➔ multi-flavors chip
- **Exploring 28nm CMOS technology** ➔ Lookup table extracted, and first design test results are obtained.
- **The project** carried out in collaboration with PSI, UZH, CERN 28nm Community and CERN DRD3/7.



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Thank you
Questions are welcome

Abderrahmane GHIMOUZ

2nd Dec. 2024

ANNEXE

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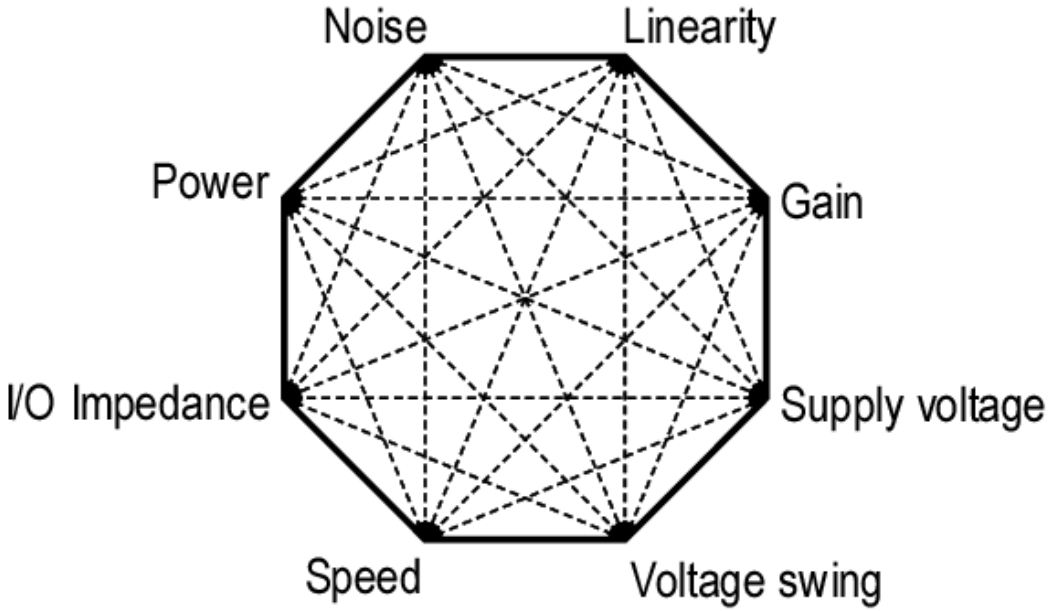
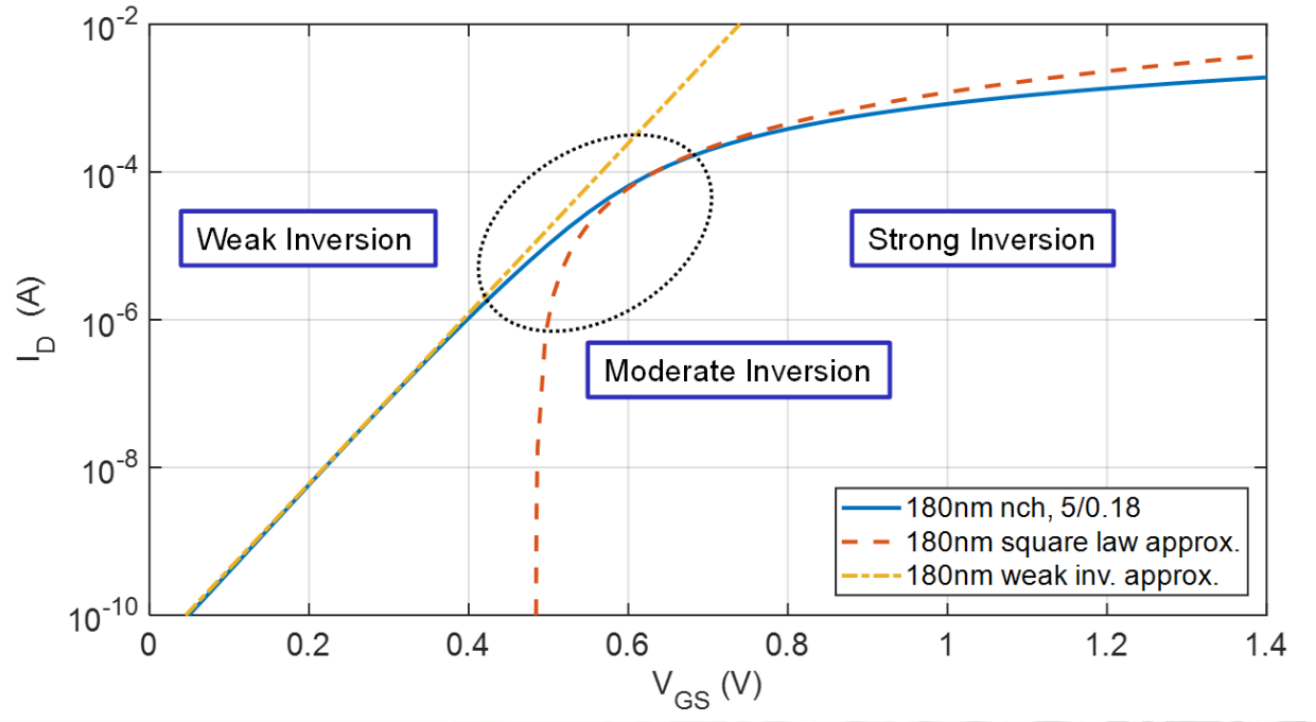
Part 3
28nm Technology

Design methodology : Exploring the $^{g_m}/_{I_D}$





Credit : Boris Murmann

Why analog design is challenging ?

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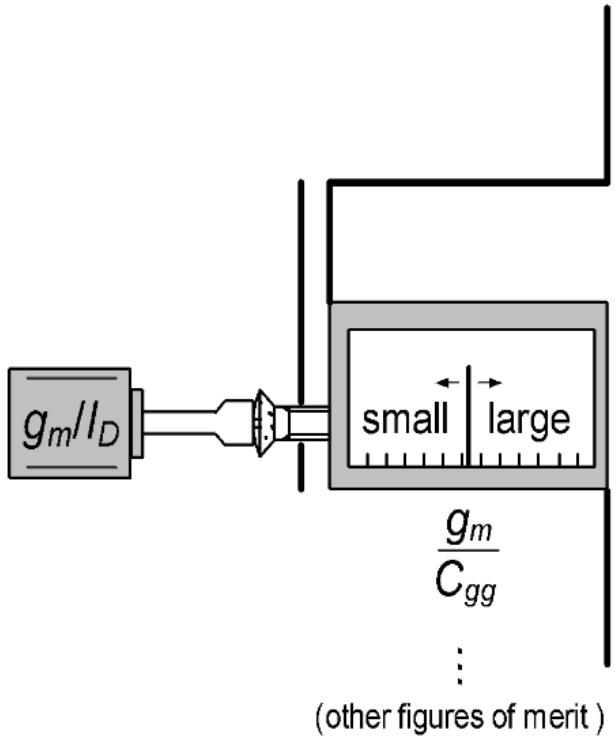
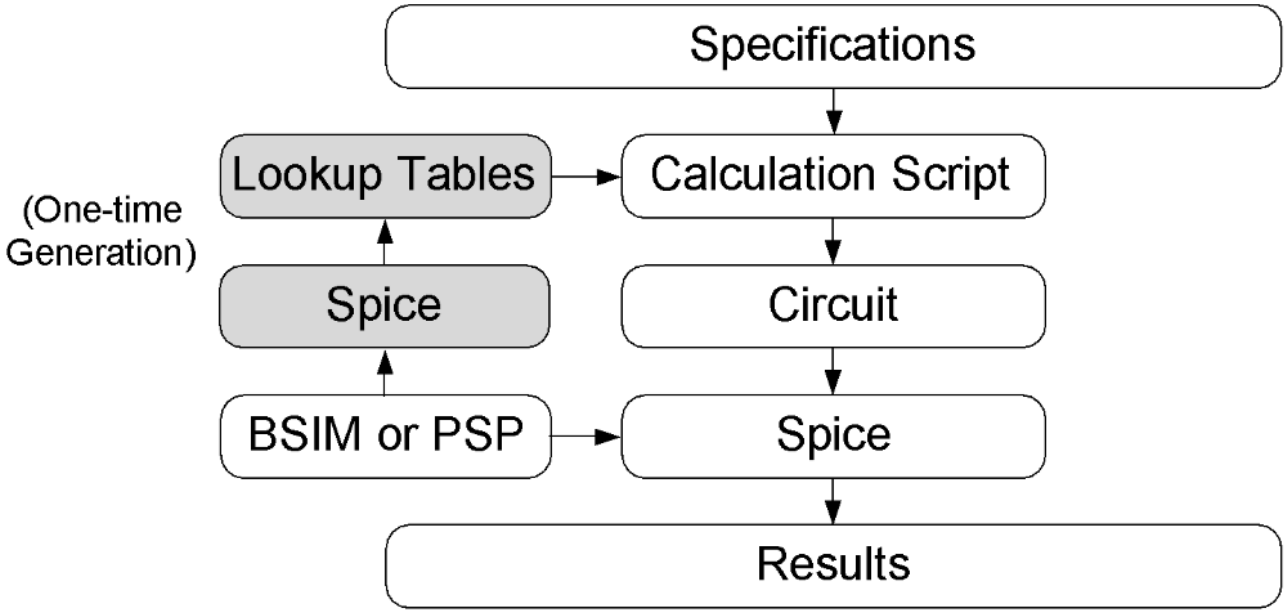
Part 3
28nm Technology

Design methodology : Exploring the $^{g_m}/_{I_D}$





Credit : Boris Murmann

The $^{g_m}/_{I_D}$ methodology uses the ratio of transconductance to drain current to optimize analog circuit design. By generating lookup tables from SPICE simulations, designers can quickly evaluate performance metrics and efficiently achieve desired specifications.

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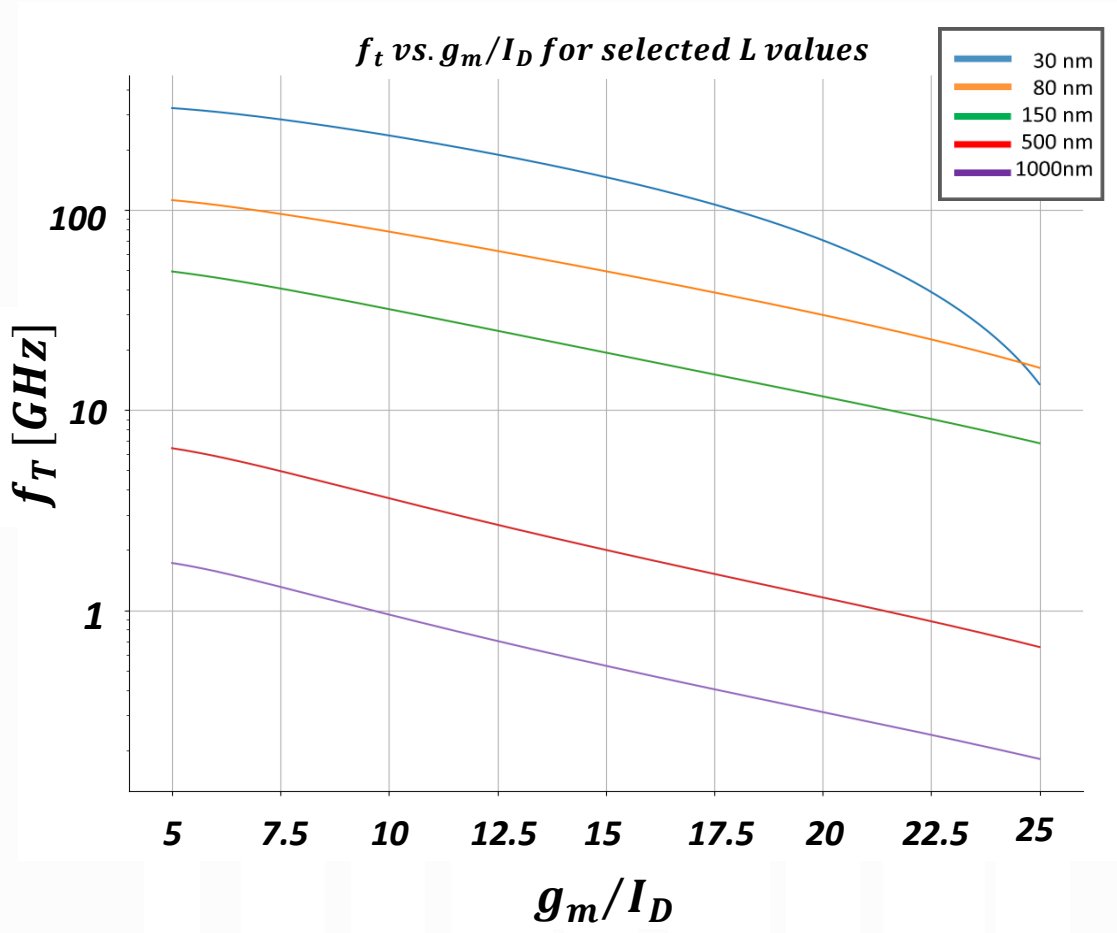
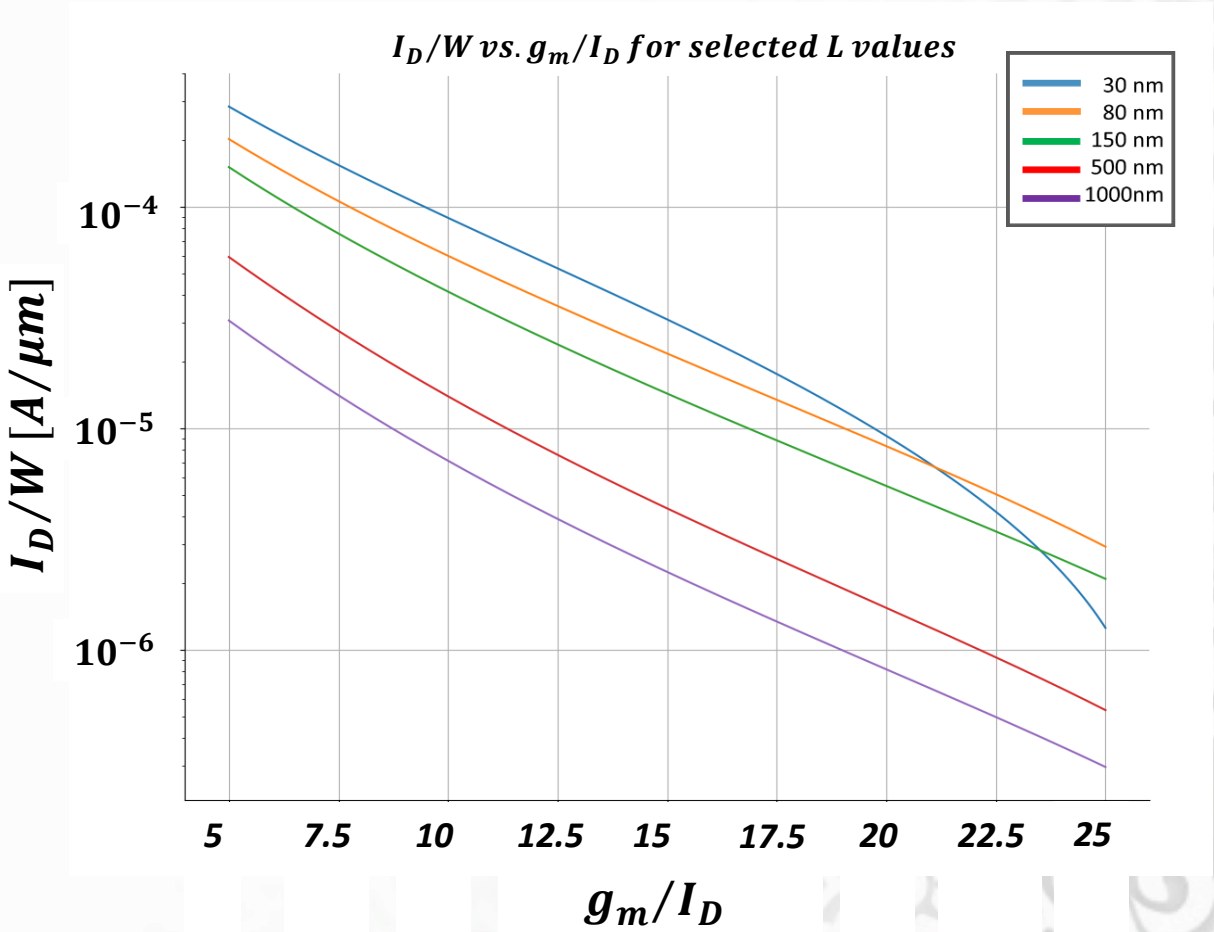
Part 3
28nm Technology

The extraction of the $^{g_m}/_{I_D}$ Lookup tables of the 28nm technology

Speed



Efficiency



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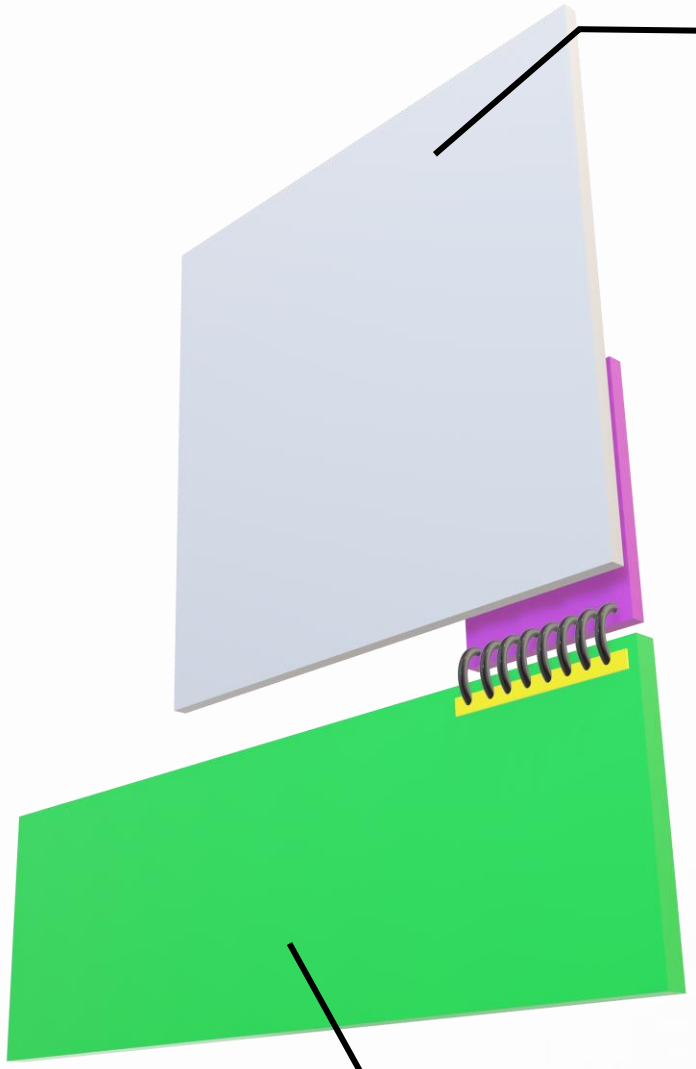

1st implementation

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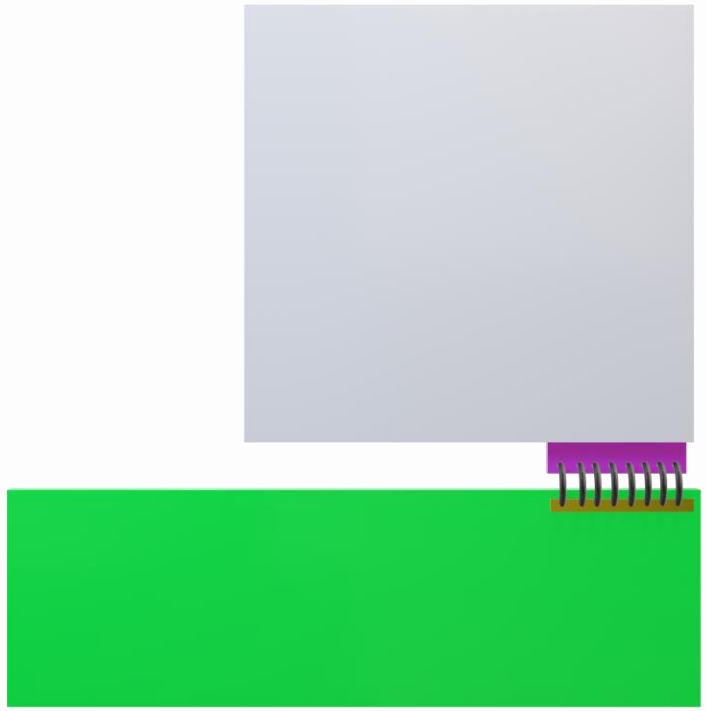

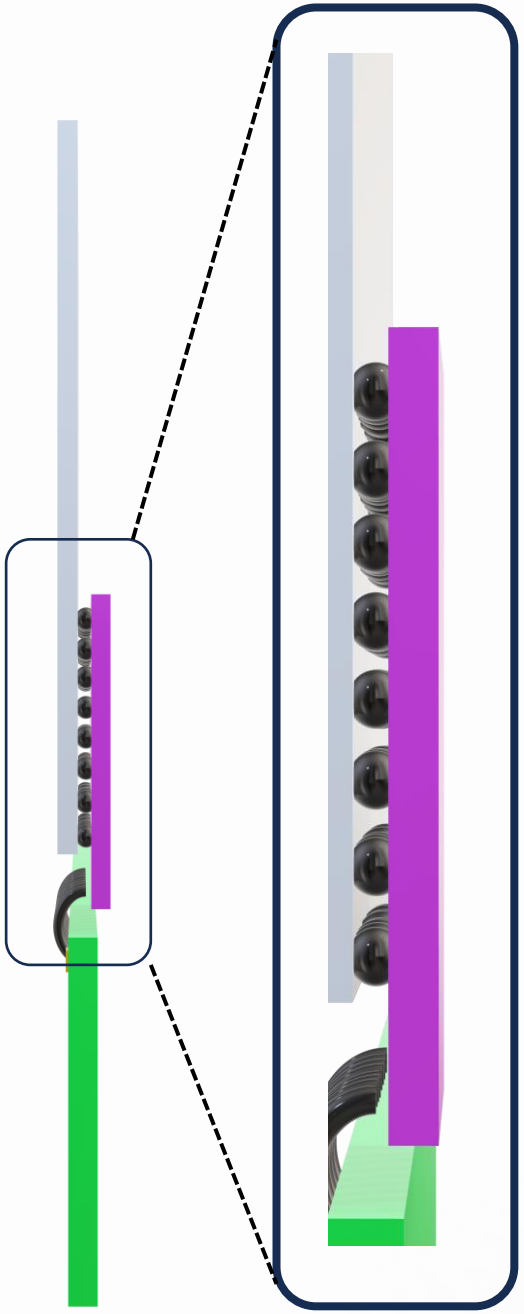

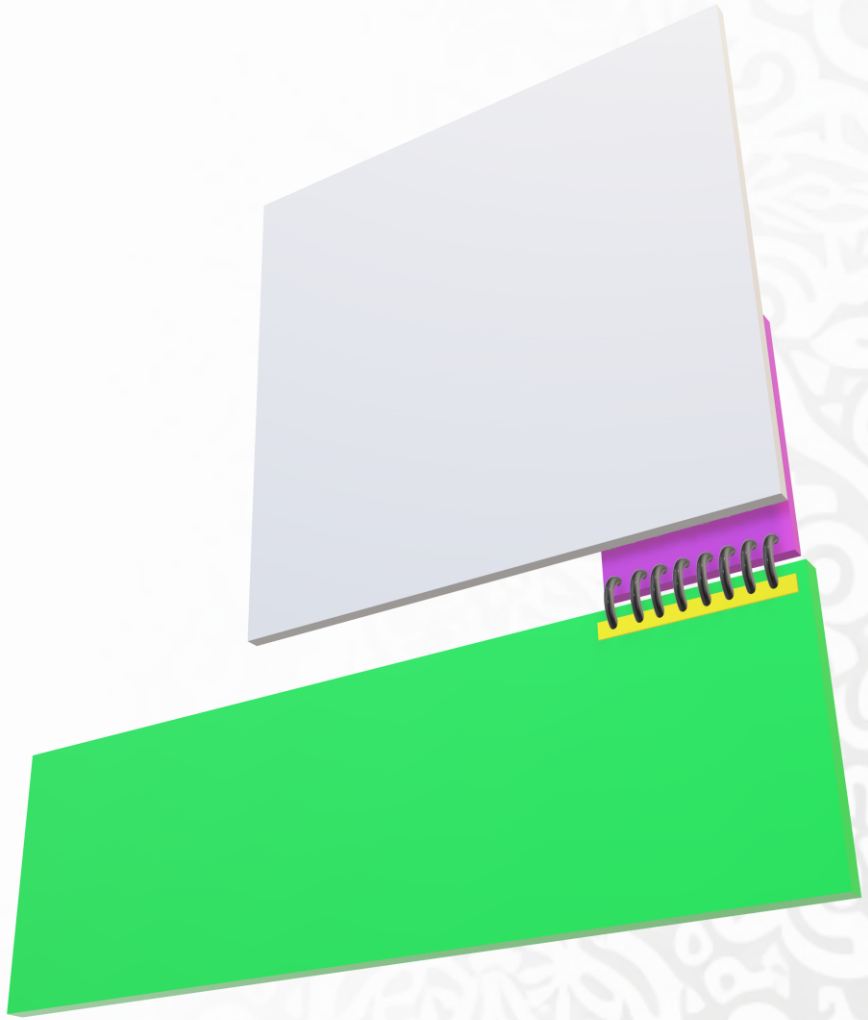

1st implementation