

ASIC Development for Timing Measurements using LGAD Sensors

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The CMS experiment will enhance its capabilities with precision timing detectors covering $|\eta| \leq 3$ to manage high rates and reduce pile-up in the HL-LHC era starting in 2030. Future upgrades may extend timing across the full tracker acceptance ($|\eta| \leq 4$), with LGADs as a potential option for pixel detector end-cap replacements. This project focuses on the development of an ASIC in 28 nm CMOS technology, optimized for TI-LGAD sensors, capable of achieving sub-30 ps timing resolution. Key features include a low-jitter preamplifier, a discriminator stage, and a Time-to-Digital Converter (TDC), with radiation tolerance up to $1\text{-}5 \times 10^{15}$ neq/cm².

The ASIC design will balance performance, power efficiency, and integration while addressing HL-LHC challenges. Initial prototypes will feature a limited number of channels for systematic testing of timing resolution and radiation hardness. Successful designs will scale to full-channel ASICs compatible with various LGAD types, ensuring flexibility for future sensor developments.

Fabrication will occur via MPW/mini@sic runs, with testing in realistic radiation environments. Results will support the CMS Tracker upgrade, contribute to advancements in 4D tracking technologies, and enable future high-energy physics experiments.

Type of presentation (in-person/online)

in-person presentation

Type of presentation (I. scientific results or II. project proposal)

II. Presentation on project proposal

Author: GHIMOUZ, Abderrahmane (Paul Scherrer Institute (CH))

Presenter: GHIMOUZ, Abderrahmane (Paul Scherrer Institute (CH))

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