Update on the DC-coupled Resistive Silicon Detector for 4D tracking

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on behalf of the 4DSHARE project

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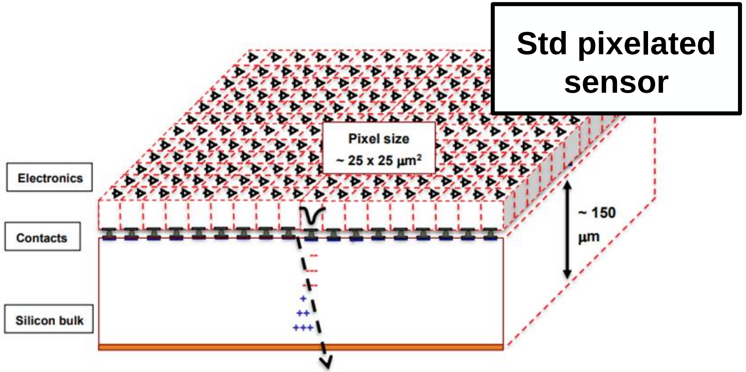
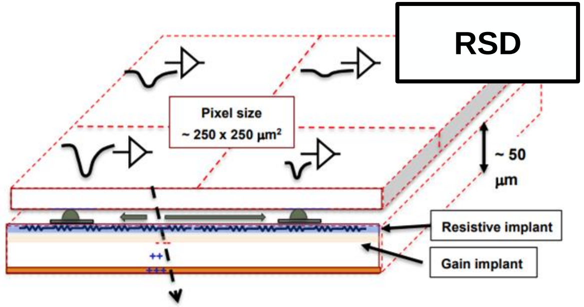
2nd DRD3 week on Solid State Detectors R&D – CERN – 2-6 Dec

The paradigm for silicon trackers using "resistive LGAD"





- **Binary read-out: σ_{Pixel} ~ 0.3·pitch**
- **AC-LGADs: σ ~ 0.03- 0.05 ·pitch**
- **AC-LGADs** time resolution with thin detectors→ **30-40 ps**

similar space resolution with reduced number of read-out channels (a factor of ~100 less)
smaller material budget

excellent time resolution

Space resolution with RSDs

FBK RSD2 (2021) best design: Swiss cross electrodes.
Position performance have been explored with laser and several test beams.

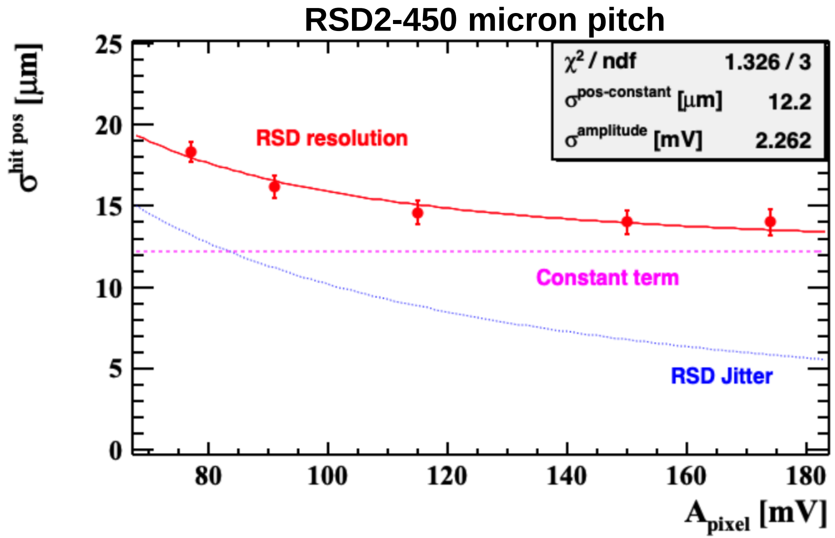
Results with electron testbeam (DESY)

RSD2-450, pixel 450 x 450 um^2 - 16 electrodes read out
16ch FAST2 Board (INFN Torino) + CAEN Digitizer

The constant term dominates the resolution $\sigma_{constant} \sim 13$ μm
It includes mis-alignment RSD-Tracker, sensor and electronics non uniformity, etc…

Resolution around **3%-4% of the pitch.**

L. Menzio et al, "First test beam measurement of the 4D resolution of an RSD 450 microns pitch pixel matrix connected to a FAST2 ASIC",)NIMA 1065 (2024), 169526

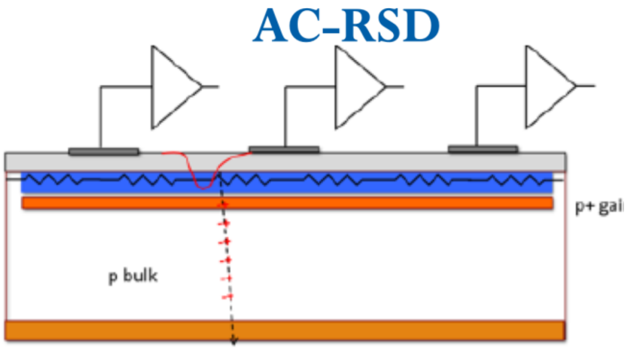


$$\sigma^{\text{hit pos}} = \sqrt{(\sigma^{\text{pos-constant}})^2 + (\frac{\sigma^{\text{amplitude}} \times \text{pitch}}{\Sigma_i^4 A_i})^2}.$$

Next evolution: DC-RSD

RSD sensors show **some non-ideal features**:

- Signal spread may involve a large (>4) and variable number of electrodes, leading to slight deterioration and a spatial resolution which is position-dependent
- Baseline fluctuations (leakage current collection only at the edge)
- The bipolar nature of the signals, with rather long tails during the discharge



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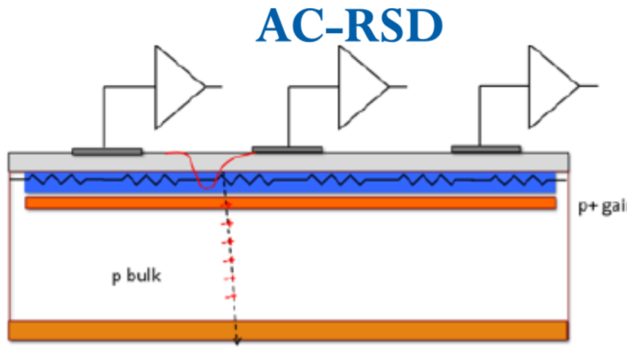
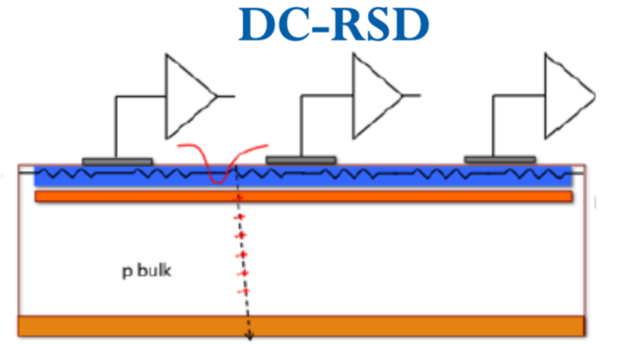
DC collection of signals, with low resistivity paths to readout pads + charge “containment” ⟹ DC-RSD design

- Signal is confined: charge sharing in a predetermined number of pads
- the leakage currents is removed locally at each electrodes
- No bipolar signal → 1-2 ns-long pulses

→ expected uniform performance and scalable to large devices

Extensive simulation studies performed to optimize design: resistive path, charge sharing, electrodes geometry, confinement method…





Status of DC-RSD production

DC-RSD development started in the framework of the **4DinSiDe** (PRIN, 2017) and is currently continuing with the **4DSHARE project** (INFN CSN5, PRIN 2022)

The first, **proof-of-concept**, production was completed @FBK in November: **DC-RSD1**

- The solution selected to achieve the charge containment: use of Isolating Trenches (like TI-LGADs or SiPM)

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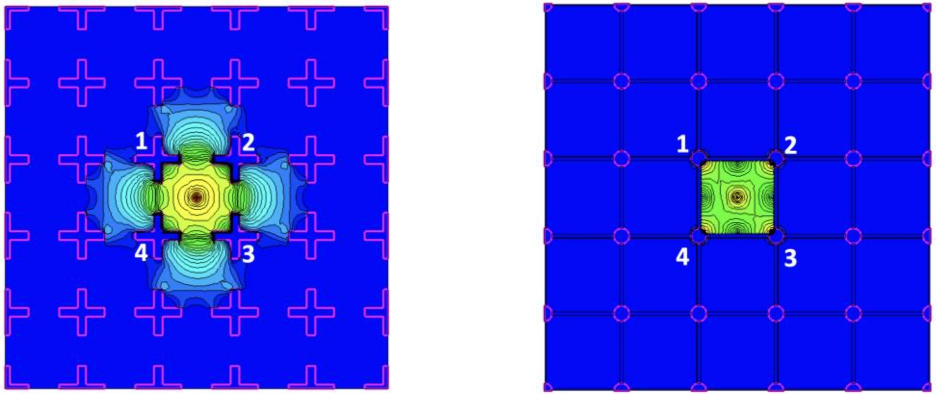
3D-TCAD simulation comparing
DC-RSD without (left) and with (right) isolating trenches



Current density over device surface, generated by a hit in the center of the sensor (3D-TCAD simulation), representing the expected **signal confinement** in a DC-RSD with cross-shaped metal electrodes (left), and with **dot-shaped electrodes** connected **with isolating trenches (right)**.

F. Moscatelli et al, https://www.sciencedirect.com/science/article/pii/S0168900224003061 (2024)

A. Fondacci's talk "Design and optimisation of radiation resistant AC- and DC-coupled resistive LGADs" (Pixel2024)

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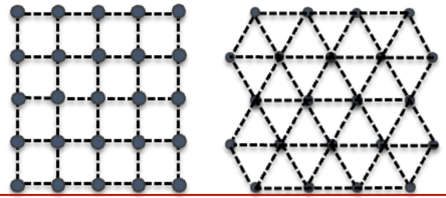
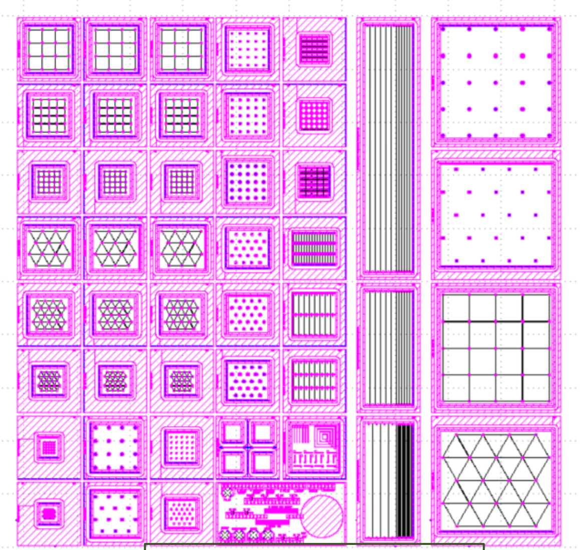
Several test structures implemented:

- devices with squared or hexagonal matrix of electrodes (dot-shaped), with and without isolating trenches, multiple pitch options
- strips with multiple pitch options and multiple length



squared or hexagonal matrix



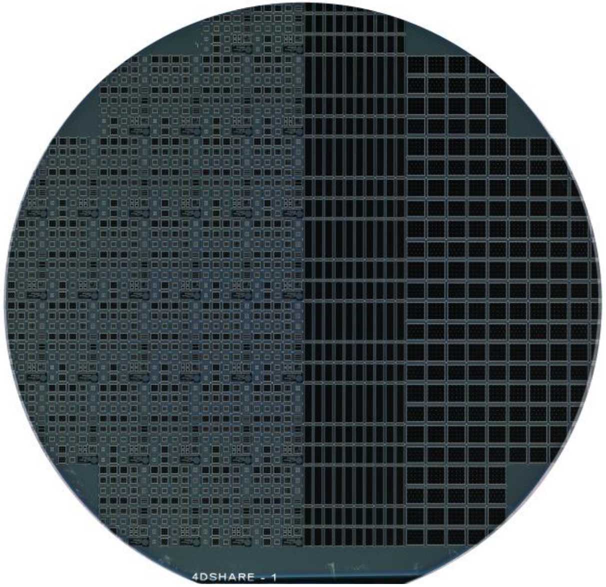
DC-RSD1 reticle

DC-RSD1: "split" table

diced

Wafer	NPLUS dose	CONHO IMP	Trench depth	Trench process	PGAIN dose	Thickness
1	0,25		D2	P2	1.02	55
2	0,25	Y	D2	P2	1.02	55
3	0,25	Y	D2	P2	1.06	55
4	0,25	Y	D2	P2	1.06	55
5	0,5		D2	P2	1.02	55
6	0,5		D2	P2	1.06	55
7	0,5	Y	D2	P2	1.06	55
8	0,5	Y	D2	P2	1.02	55
9	1		D2	P2	1.02	55
10	1		D2	P2	1.06	55
11	1	Y	D2	P2	1.02	55
12	1	Y	D2	P2	1.06	55
13	0,25	Y	D2	P2	1.06	55
14	0,5	Y	D2	P2	1.02	55
15	1	Y	D2	P2	1.06	55

- NPLUS sheet resistance
- Contact resistance Al-Si
- Gain dose

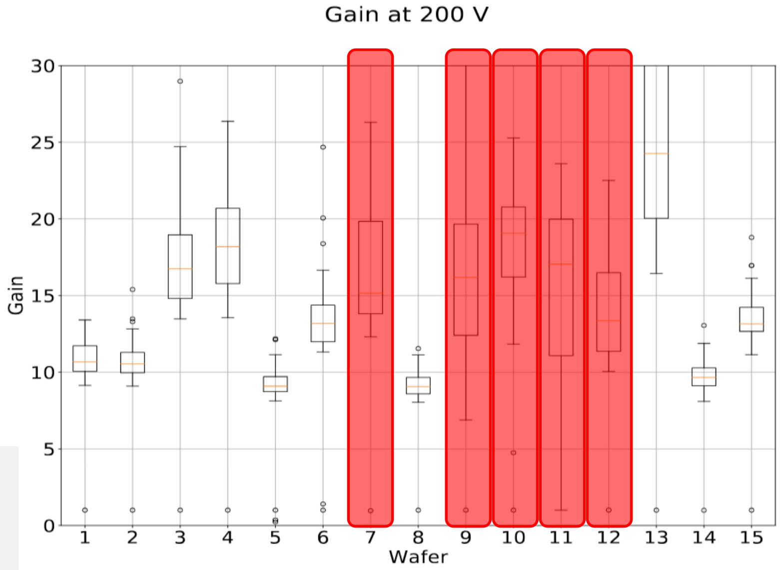


wafer layout (Photo from FBK)

DC-RSD1: gain, leakage current

Wafer	NPLUS dose	CONHO IMP	Trench depth	Trench process	PGAIN dose	Thickness
1	0,25		D2	P2	1.02	55
2	0,25	Y	D2	P2	1.02	55
3	0,25	Y	D2	P2	1.06	55
4	0,25	Y	D2	P2	1.06	55
5	0,5		D2	P2	1.02	55
6	0,5		D2	P2	1.06	55
7	0,5	Y	D2	P2	1.06	55
8	0,5	Y	D2	P2	1.02	55
9	1		D2	P2	1.02	55
10	1		D2	P2	1.06	55
11	1	Y	D2	P2	1.02	55
12	1	Y	D2	P2	1.06	55
13	0,25	Y	D2	P2	1.06	55
14	0,5	Y	D2	P2	1.02	55
15	1	Y	D2	P2	1.06	55

Gain on-wafer (median), **at 200 V**, using PIN and LGAD single pads. Gain computed comparing IV characteristics at dark and with LED light (λ= 950 nm)



Gain mean value and spread is as expected in most of the wafers, for the two pgain doses.

From IVs:

- **leakage current in range of operation in reverse bias condition is low** (for good substrate wafers)
- 5 wafers substrate have very high leakage current (high field defects) → discarded!
- Average breakdown: 280-300 V (high gain) and 330-350 V (low gain)

DC-RSD1: Al-Si contact resistence

Wafer	NPLUS dose	CONHO IMP	Trench depth	Trench process	PGAIN dose	Thickness
1	0,25		D2	P2	1.02	55
2	0,25	Y	D2	P2	1.02	55
3	0,25	Y	D2	P2	1.06	55
4	0,25	Y	D2	P2	1.06	55
5	0,5		D2	P2	1.02	55
6	0,5		D2	P2	1.06	55
7	0,5	Y	D2	P2	1.06	55
8	0,5	Y	D2	P2	1.02	55
9	1		D2	P2	1.02	55
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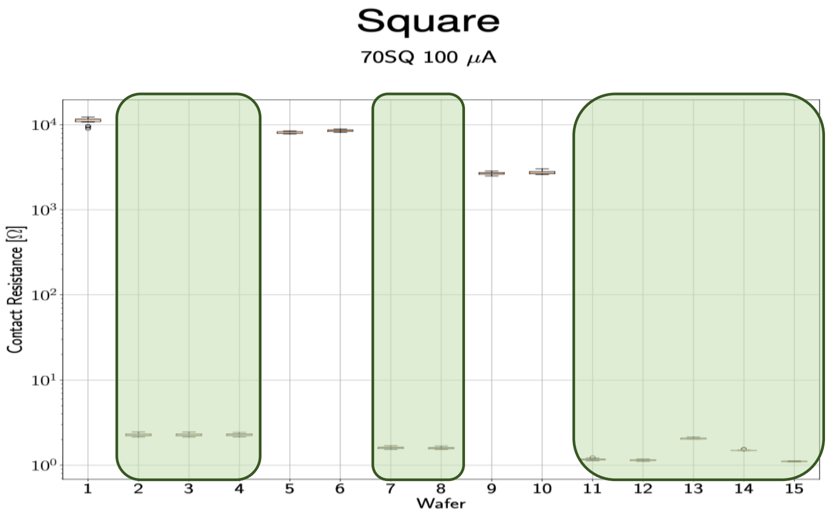
12	1	Y	D2	P2	1.06	55
13	0,25	Y	D2	P2	1.06	55
14	0,5	Y	D2	P2	1.02	55
15	1	Y	D2	P2	1.06	55

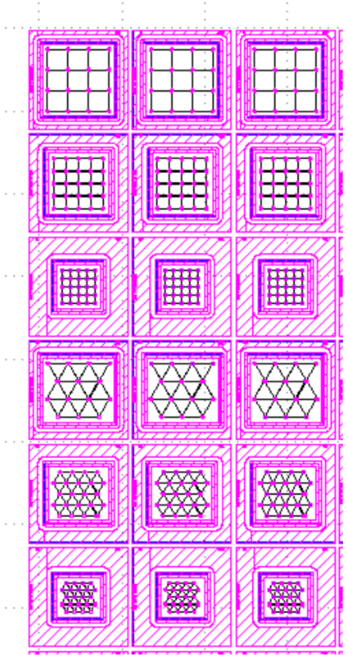
Study of the **Al-Si contact resistance** in the production, using **dedicated test structure** emulating the **various electrode designs**

11 wafers have an extra n++ implant below the metal contacts of each device (introduced predicting possible sub-optimal contact resistance between Al and n+ layer)

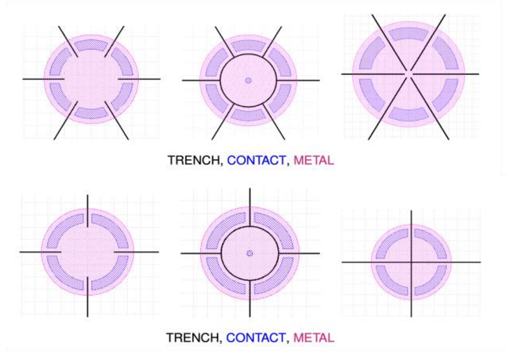


DC-RSD1: on-wafer characterization

IV characteristics on-wafer performed on all wafers, on a sub-set of device types in these two regions

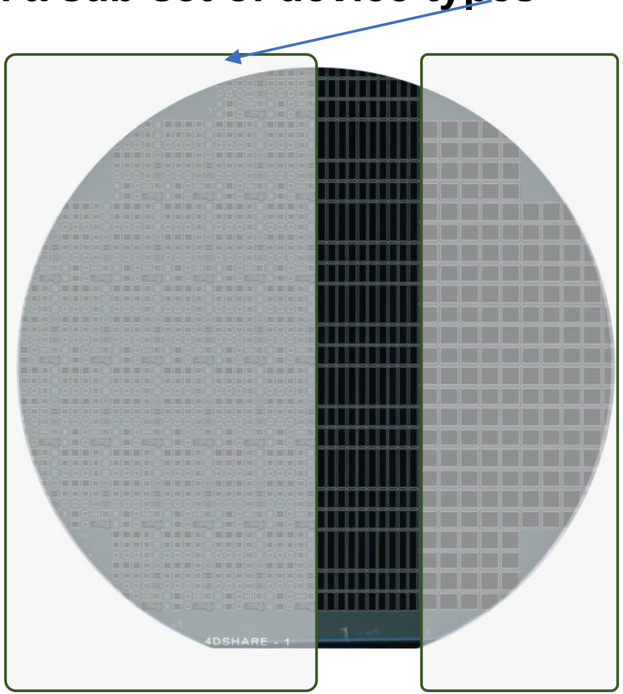


A B C



A B C

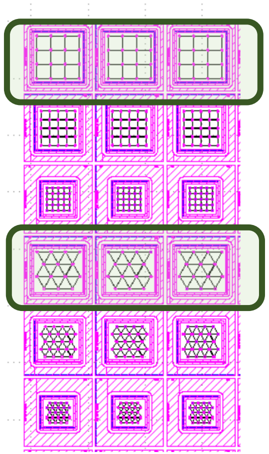
Three types of "trench crossing" under the electrode implemented



DC-RSD1: on-wafer characterization

IV characteristics for 5 shots on **wafer W3**

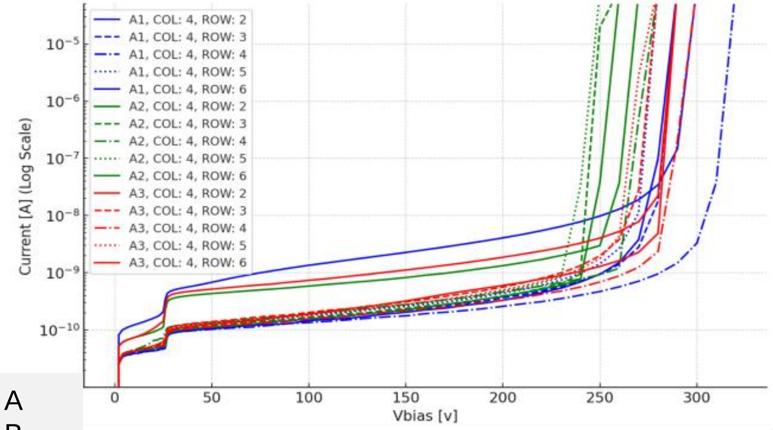
Comparison between the **three types of "trench crossing"** for:

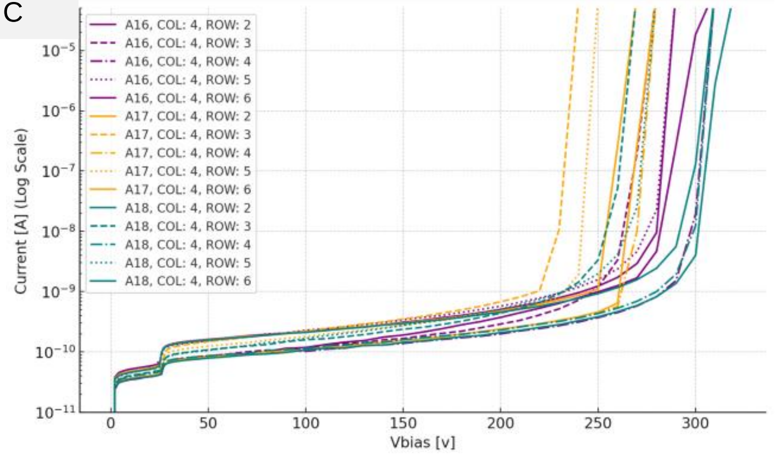


pixel matrix 3x3 squared 500 μm

exagonal matrix, 15 pixels, 500 μm

A1, A16 = type A
A2, A17 = type B
A3, A18 = type C





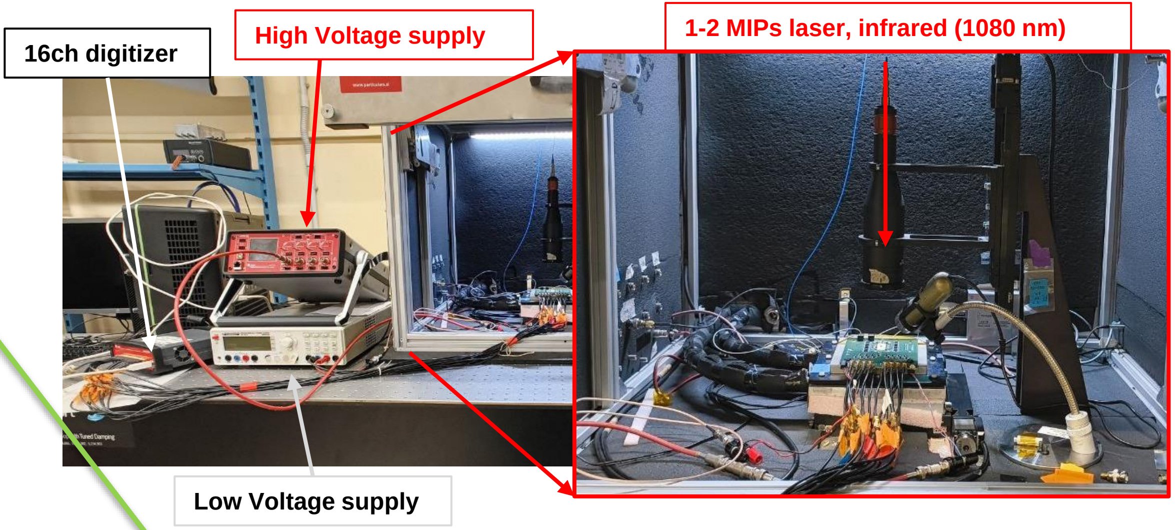
"Type B" devices show a slight early BD, either due to the design or to the testing method (single needle measurement). More measurements will follow.

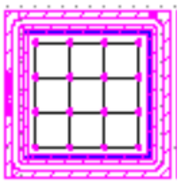
For the time being focussing on "Type A" devices

First characterization in LAB

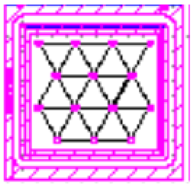
Diced sensors arrived 2 weeks ago in Torino (LISS)
Ongoing measurements:

- Quick scan at the **TCT** with **sensors wire-bonded to FNAL board**
- Acquisition with **beta** setup
- Scan on sensor surface with TCT setup

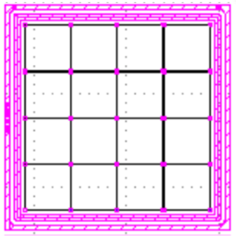




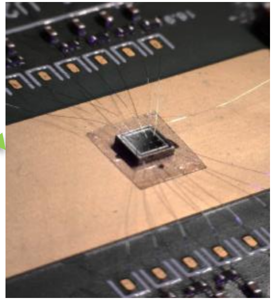
500 µm pitch, **Squares** (A1)



500 µm pitch, **Triangles** (A16)

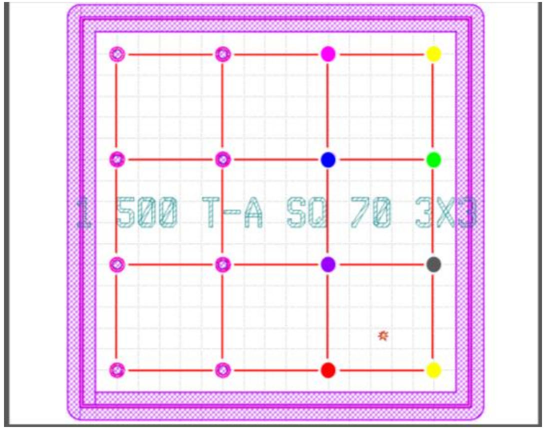


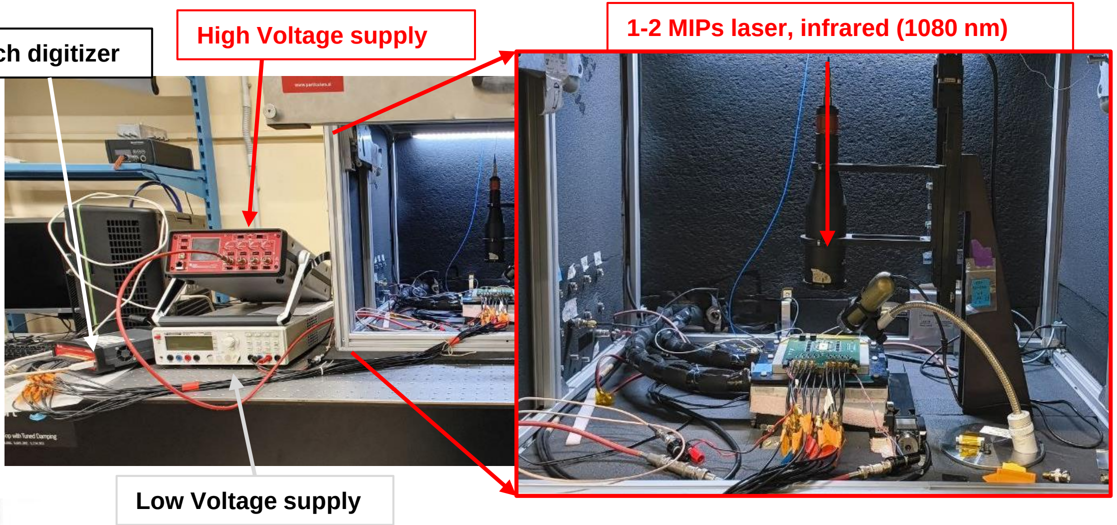
1000 µm pitch, **Squares** (C44)

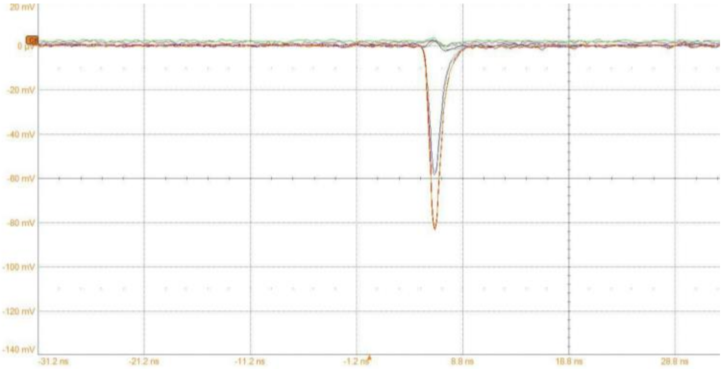


"FNAL board"
Fast pre-amplifier TIA developed at FNAL, discrete electronics
16 channels, ~25 ps jitter
Fixed gain G ≈ 70
Low input impedance ≈ 25 Ohm

First characterization in LAB



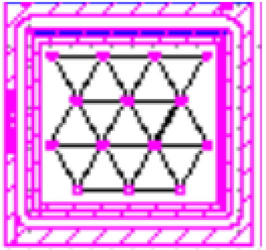




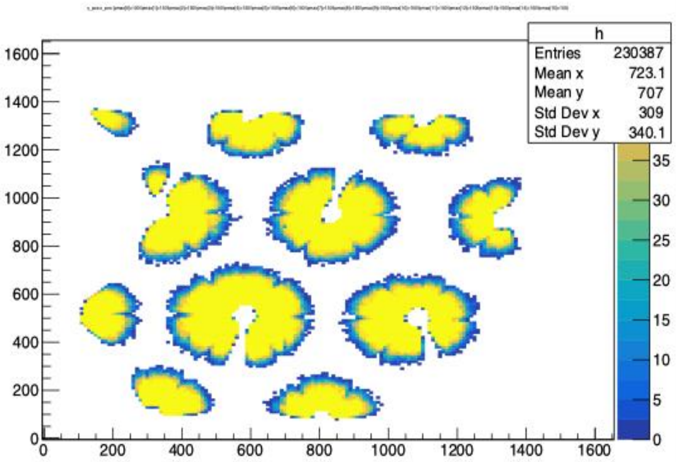
Very nice signals:

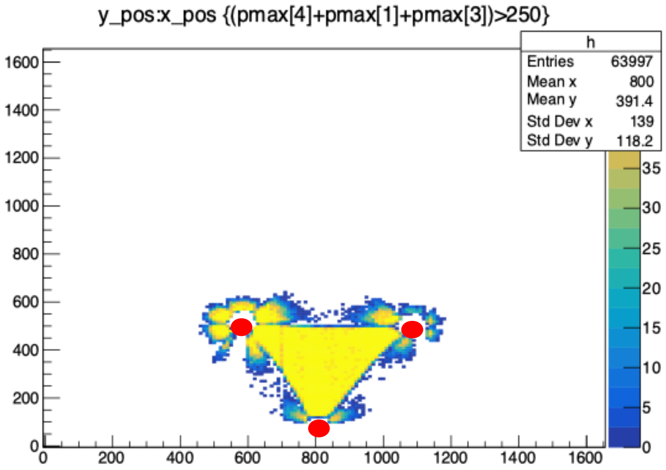
- **Fast**, about 2 ns in total (similar to standard LGADs)
- **High amplitude**, amplitude sum over one cell (4 electrodes) ~ 300 mV @ 20 V from breakdown

Preliminary TCT scans



500 µm pitch,
Triangles (A16)
gain layer only within trench matrix





Occupancy maps obtained with TCT data (scanning over device surface)

- Left: **x-y distribution of hits when the amplitude seen by any electrode is above 150 mV**
  - → **quick sanity check of electrodes signals and connections**
  - → visual representation of signal sharing

- Right: **x-y distribution of hits when the sum of the amplitudes seen by the 3 red electrodes (triangle corners) is above 250 mV**
  - → **representative of charge containment within a cell**

Outlook

The **first prototype run of DC-RSD has been completed** and it is currently under testing!

Initial measurements done @FBK on-wafer gave us very important feedback on the success (or problematic points) of the process flow

We are now **progressing with the characterization** of some **selected sensor types in the laboratory** (in Torino, and soon in Firenze and Perugia)

DC-coupled electrodes are alive, and charge is contained by the trenches

We are preparing for the first **DC-RSD Test Beam** in **DESY** (next week!), and for the full systematic studies of the production (months of work…)

Wish us good luck and Stay tuned!

Acknowledgements

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- INFN CSN5 through the 4DSHARE research project
- PRIN MIUR project 2017L2XKTJ '4DInSiDe'
- PRIN MIUR project 2022KLK4LB '4DSHARE'
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