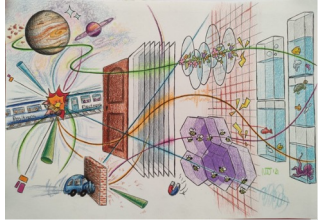
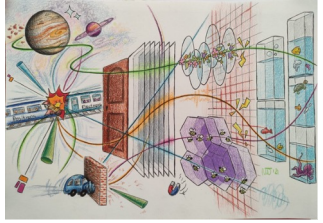


WG7 session - discussion on interconnects

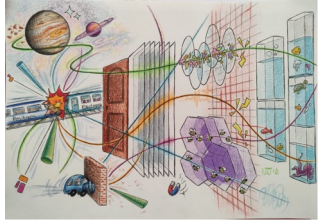
G. Calderini (LPNHE Paris), D. Dannheim (CERN), F. Huegging (Bonn)



June Expressions of Interest

DRD3

Group	Contact	Ongoing work / topics of interest	Maskless	classical processes	2.5D integr. / modules	3D integration	FTE
ANL	Jessica Metcalfe	technologies for large-scale tracking devices	☐	☐	☐	☐	
Bonn University*	Fabian Hügging, Jochen Dingfelder	fine-pitch (<50 um) bonding; W2W bonding; in-house hybridisation	☑	☑	☐	☑	1 Staff + 1 Stud./Postdoc/Techn.
CERN*	Dominik Dannheim	In-house plating and hybridisation; compact module studies (including silicon photonics integration)	☑	☐	☑	☐	2.5 Res. + 2 Stud.
FBK	Giovanni Paternoster	3d-integration and interconnection of BSI-SiPMs for NUV/VUV; mask and mask-less UBM; W2W temporary bonding; chip-level solder-ball bonding >50 um; wafer-level micro bumps/pillars <50 um; in-house maskless interconnects	☑	☑	☑	☑	1 Staff
Fraunhofer IZM*	Thomas Fritzsch	hybridisation with <=25 um pitch; W2W bonding; wafer-level packaging; single-chip bump bonding for R&D	☐	☑	☐	☑	1 Staff
Geneva University*	Mateus Vicente	In-house flip-chip bonding: gold studs, ACP/ACF, Cu pillars; chip-to-flex	☑	☐	☑	☐	
IMB-CNM-CSIC	Miguel Ullán	RDL, TSV, interposers	☐	☑	☑	☐	0.5 Res.
INFN Bari	Giovanni Francesco Ciani	interconnection between bent sensors; stacking of several CMOS sensors for full 3d tracking	☐	☐	☑	☐	0.5 Res. + 0.5 Stud.
INFN Cagliari	Adriano Lai	in-house single-die hybridisation with innovative bonding techniques such as ACF/ACP	☑	☐	☐	☐	
INFN Firenze	Giacomo Sguazzoni, Giovanni Passaleva	Novel interconnection techniques for future applications	☑	☐	☑	☐	0.5 Res. + 0.5 Stud.
INFN Milano	Gianluca Alimonti	Indium bump bonding; in-house die-to-die and die-to-PCB bonding; hybridisation of RSD; multi-chip systems on PCB/bus tape	☑	☑	☑	☐	
INFN Trieste	Giacomo Contin	interconnects for bent and ultrathin chips (ALICE ITS3); aerosol jet printing for RDL and contactless interconnects; TSV and wafer-to-wafer for 3D stacking	☐	☐	☐	☑	3 Res. + 1 Stud.
IPHC Strasbourg	Maciej Kachel	3D integration; small pitch (<10 um) interconnection	☐	☑	☐	☑	0.1 Staff
IP2I Lyon	Didier Contardo	wafer-to-wafer interconnect demonstrator	☐	☐	☐	☑	0.6 Physicist + 2.8 Tech
KIT Karlsruhe	Michele Caselle	in-house flip chip, gold studs, TSV processing, RDL	☑	☐	☑	☐	0.5 Staff + 1 Stud.
LPNHE Paris	Giovanni Calderini	interconnects: ACF, ACP, gold studs; characterisation techniques and devices; reliability testing; new interconnection techniques / scalability	☑	☐	☐	☐	1.5 Res. + 1 Stud. + 1 Techn.
MPG Halbleiterlabor*	Ladislav Andricek, Jelena Ninkovic	direct wafer bonding; 3D/2.5D systems with micro-channel cooling; W2W/C2W bonding	☐	☑	☑	☑	1 Staff + 2 Stud./Postdoc/Techn.
NIKHEF	Martin Fransen	high-frequency ASIC to module integration (RDL, TSV), wire bonding	☐	☐	☑	☐	0.2 Staff
ORNL	Mathieu Benoit	in-house interconnect for hybridisation and module building: single-chip bumping, UBM, bonding; gold studs, ACP/ACF, Cu pillars; chip-to-flex, chip-to-interposer; interposer fabrication	☑	☐	☑	☐	1 Staff + 1 Stud./Postdoc/Techn.
*groups presenting at DRD3 workshop June 2024							**~30 FTE in total**



Points for discussion

- Originally received 18 EoIs for interconnect activities, ~30 FTE
  - 35 groups had expressed interest in initial questionnaire

- Several institutes already pursue interconnect activities
  - 4 institutes presented ongoing activities at June Collaboration meeting
  - Mostly linked to various ongoing / approved projects (also large overlap with AIDAinnova WP6)
  - 2 additional subjects presented today

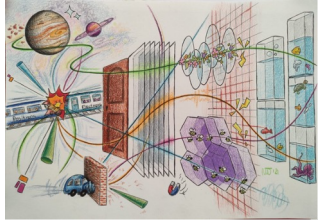
- Call for projects ongoing
  - 1(+1+1?) Project proposal in a more advanced shape (linked to what in the proposal was RG 7.1 / 7.2 / 7.3)

    - Development of in-house plating, hybridization and module integration technologies for pixel detectors (CERN, Fondazione Bruno Kessler, LPNHE Paris, Univ. Geneva)
  - 1 Project has solid proposal but still at the beginning of the editorial part RG 7.4

    - Ultrathin hybrid pixel detectors using wafer-to-wafer bonding (U. Bonn, IZM)
  - 2 Project proposals at the interface with DRD7 for which groups had expressed interest (ongoing) RG 7.2 / 7.5

    - Improving classical bump-bonding process
    - Module 2.5D integration

7.1 Yield consolidation for fast interconnection technologies
7.2 Demonstration of in-house process for single dies and pixel interconnections for a range of pitches (down to < 30 µm)
7.3 Development of post-processing for classical bumping interconnection
7.4 Development of wafer-to-wafer interconnections
7.5 Development of VIAS in multi-tier sensor/front-end assemblies



Project 1: Development of in-house plating, hybridization and module integration technologies for pixel detectors

DRD3

7.1.1 Description

This project develops innovative and scalable plating, hybridisation and module-integration concepts. Short-term applications include in-house single-die processing for pixel-detector R&D projects, as well as low-temperature hybridisation for irradiated sensors. The long-term goals concern scalability to large-area hybrid-pixel-detector systems for future collider detectors.

Most interconnect processes require specific surface properties and topologies of the bonding pads. An in-house Electroless Nickel Gold (ENIG) plating process is therefore under development, which is performed on single-die level and can be adapted to a large range of pad geometries and bonding techniques. The plating is performed in a chemical laboratory at CERN, using dedicated test devices, as well as functional ASICs and sensors from various projects.

The in-house flip-chip hybridisation and module-integration processes under study include bonding with anisotropic conductive adhesives (ACA) available from industry, gold-stud bonding with glue underfill, and nano wires. A flip-chip bonding machine at UNIGE is currently used for all flip-chip assemblies. The produced assemblies are tested at CERN, LPNHE and in the collaborating projects.

Novel low-mass flip-chip-capable module-flex printed circuit boards (PCBs) are under development within the project, to enable compact packaging through the direct attachment of chip connection pads to the flex.

The design and production of dedicated chain-device test structures for plating and interconnect process optimisation is part of the project scope, and the structures will be produced by FBK. Reliability tests for thermo-mechanical stress and radiation exposure will be performed at CERN and LPNHE.

The project foresees to collaborate with hybrid- and monolithic-pixel-detector projects in DRD3 WG1, WG2 and WG6, by receiving samples and providing hybrid assemblies and modules that are then characterised in the participating projects.

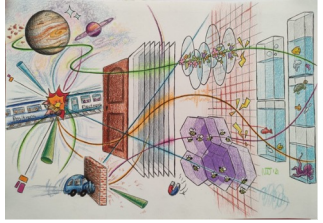
Country	Collaborating Institution	Town	Institution Code	Contact
France	Laboratoire de Physique Nucléaire et des Hautes Energies, Paris	Paris	LPNHE	G. Calderini
Italy	Fondazione Bruno Kessler	Trento	FBK	M. Boscardin
Switzerland	CERN	Geneva	CERN	D. Dannheim
Switzerland	University of Geneva	Geneva	UNIGE	M. Vicente

7.1.3 Start And End Date, Deliverables and Time Scale

The Work Package has started at the beginning of 2024 with an initial duration of 4 years (until end of 2027), with potential for a further prolongation.

The deliverables, time scales and contributing institutions are indicated in the table below.

Number	Title	Description	Start date	End date	Institutions
Di.1	Interconnect test structures	Design and production of test devices for plating and interconnect process optimisations.	Q1 2025	Q2 2026	CERN, FBK, LPNHE, UNIGE
Di.2	Plating process	Development and optimisation of in-house ENIG plating process for high yield and uniformity.	Q1 2024	Q4 2026	CERN
Di.3	Hybridisation process	Development of single-die hybridisation processes, for pixel pitches from ~1 mm^2 down to 25 µm and up to ~2 cm^2 bonding areas.	Q1 2024	Q4 2027	CERN, LPNHE, UNIGE
Di.4	Module flex	Development of flip-chip capable low-mass flexible PCB.	Q1 2024	Q4 2027	CERN, UNIGE
Di.5	Reliability testing	Validation of the robustness of the developed interconnect processes against thermo-mechanical and radiation-induced stress.	Q1 2025	Q4 2027	CERN, LPNHE



General remarks

DRD3

- As already noticed in yesterday's discussion many FAs are still hesitant to take official engagements
  - Finalization of MoU still ongoing
  - Long-term financial and HR engagement

- Structure of projects still not completely frozen in terms of organization
  - Still DRD3 discussions in the way projects should be presented in terms of WP, deliverables
  - The way projects should/might be grouped is not completely clear yet

  -> presently aiming for a few projects covering relevant activities to 2027, short list of deliverables, all institutes contributing to at least one deliverable, no resource commitment required as of today

- Some more homework needed in the definition of the interfaces within DRD3 and also to DRD7
  - Some project still presenting developments in both Collaboration; in some case, groups might have limited resources and they are hesitant to pursue dedicated interconnection R&D in WG7 in addition to their core activity

- These conditions are slowing down a bit the building of the structure of WG7 projects

Please don't feel shy, express your interest in present and new projects and tell us how WG7 can support your research