

Development of in-house plating and hybridisation technologies for pixel detectors



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Introduction

- Development of an in-house module hybridization technique in two main steps:
- 1. Bumping: creation of bumps on the pads of Sensor and ASIC with ENIG plating, gold studs...
- 2. Flip-chip assembly with an anisotropic conductive layer or non-conductive layer between the chips

Advantages:

- Single die processing
- Adaptable to the application
- Low temperature process
- Maskless
- In-house (short turnaround time, quick adjustments)



- ACF: Anisotropic Conductive Film
- ACP: Anisotropic Conductive Paste
- NCP: Non-Conductive Paste



1) Chips bumping with ENIG plating



Introduction

3 main steps for Electroless Nickel Immersion Gold (ENIG) plating:

- 1. Pre-treatment and zincation of the aluminium pad (electroless)
- 2. Electroless Nickel deposition (creation of the bump)
 - Self-catalytic reaction on pad surface, bump height controlled by immersion time
- 3. Immersion Gold
 - Corrosion protection, bondable surface, very thin layer (< 1 μ m)





FIB cross-section of an ENIG bump on an aluminium pad



Sample preparation improvements

Samples preparation:

- Gluing the chip on holder
- Protection of bonding pads





R&D

Challenges for the preparation of small-sized chips (handling, gluing, protection of bonding pads)



Development of a microdispenser for small chips gluing



Probe station micromanipulator



3D printed adaptor







2.4 mm



Pre-treatment setup

Pre-treatment: ultrasound + manual movements





Nickel Plating setup and gold plating



Setup for nickel plating

Temperature probe

R&D



Setup for gold plating



Cyanide based solution



TimeSpot ASIC <u>Functional chip</u> 55µm pitch, <u>19µm</u> <u>pads</u>

Excellent ENIG results:

- 100% of pads correctly plated (1184 pads)
- No overplating
- Bumps height: 10 μm (+/-0.5 μm) 1h deposition

Collaboration with INFN Cagliari (Angelo LOI, Adriano LAI) https://web.infn.it/timespot/

Before plating, optical microscope



0028 30.0kV 21.5mm x350 UVD 100Pa 05/16/2024 100

After 1h plating, optical microscope





TimeSpot ASIC





KEK AC-LGAD Sensors and ASICs

Functional chips 100 µm pitch, 40 µm diameter pads

Excellent ENIG results:

- 100% of pads correctly plated (100 pads)
- No overplating
- Bumps height: 8.5 μm (± 0.6 μm)

Collaboration with KEK (Koji NAKAMURA) and University of Geneva (Lorenzo PAOLOZZI)

Tomoka Imamura, Sayuka Kita, Koji Nakamura, and Kazuhiko Hara, "Development of HPK Capacitive Coupled LGAD (AC-LGAD) detectors", PoS, vol. VERTEX2023, pp. 032, 2024

After plating, SEM





1.3 mm

Optical microscope, 61° tilt

ColorPix2 <u>Functional</u> <u>chips</u> 70 µm pitch, 40 µm pads

Excellent ENIG results:

- 100% of pads correctly plated (1156 pads)
- No overplating
- Bumps height: 11 μm (± 0.5 μm) 1h deposition

"Color imaging of Xrays", FNSPE CTU in Prague

https://indico.cern.ch/event/829863/co ntributions/5053901/attachments/256 7463/4426692/PIXEL2022_poster.pdf



After plating, SEM



Optical microscopy after ENIG plating



mm

တ



Conclusion for ENIG plating

Optimised ENIG plating:

- Reproducibility
- No skipped pads
- No overplating
- Uniformity

Tested on different configurations:

- High pad density (20 μm pitch) and small pads (10 μm)
- Low pad density (1.3 mm pitch) and large pads (90 μm)
- Successful plating of functional chips TimeSpot, ColorPix, KEK AC-LGAD ASICs and sensors, and LGAD sensors for ALTIROC3

	Pad size	Pitch	ENIG height	Chip size
"Timepix3" daisy-chain test structures	12-22 µm	55 µm	10 µm	14x14 mm
"Small pitch" daisy-chain test structures	10x8 µm² (rectangular)	20 µm	4.5 μm	3.2x3.2 mm
TimeSpot ASIC	19 µm	55 µm	10 µm	2.4x2.7 mm
ATLAS HGTD LGAD sensors	90 µm	1.3 mm	8.5 µm	20x22 mm
KEK AC-LGAD Sensor and ASIC	40 µm	100 µm	8.5 µm	ASIC 1.3x2.9 mm Sensor 1.9x1.9 mm
ColorPix2	40 µm	70 µm	11 µm	3x4.9 mm



2) Flip-chip hybridisation



Hybridisation with flip-chip

Bonding done at Geneva University using semi-automatic flip-chip bonder

- Precise temperature, pressure and alignment control
- Heating up to 400 ℃ and force applied up to 100 kgf
- Available for bonding with Anisotropic Conductive and Non-conductive Film/Paste ACF/ACP or NCF/NCP

ACF bonding has two steps: lamination and bonding

- ACF lamination at 80°C, ≈ 5 kg/cm2
- Bonding at 150° C, ≈ 50 kg/cm²



ACP bonding has three steps:

- Mixing the micro-particles with the liquid adhesive
- Dispensing the mix on the bottom chip
- Flip-chip bonding



Operator = Anite Pere



Top chip

Conductive

particle

ACF

Bottom chip-

WD = 5.1 mm

Mag = 2.00 K X

Characterisation of daisy-chain test structures





Hybridisation and characterisation of functional chips

ENIG plated TimeSpot chip

Si 3D trench sensor TimeSpot chip TimeSpot chip Si 3D trench 8 0 0 0 sensor 6 6 6 6 6 6 to one one one on Before ENIG o o o o o o o o o o o o variations of o o o o o o o o o o o o o bump sizes 0000000000000 0000000000000

TimeSpot:

One hybrid realised with not optimised ENIG plating (first plating, before optimisation)

- 32x32 pixels, 55 µm pitch
- Si 3D trench sensor
 - ACF 18 µm thick
 - >85% connection yield (Characterised by Angelo Loi INFN Cagliari)



3) Hybridisation with gold studs



Gold-stud hybridisation of ALTIROC3/A and LGAD sensors

- Using ALTIROC3/A ASICs and LGAD sensors from ATLAS High-Granularity Timing Detector (HGTD) to develop new in-house bonding process for sensor and ASIC qualification
- Single and stacked double gold studs used for the connections between the chips, epoxy underfill for bonding
- Used for radiation-hardness qualification of LGAD sensors
- Low temperature process (60°C) to avoid uncontrolled annealing



Gold studs are deposited one by one https://www.youtube.com/watch?v=ICRDBpmev4o&t=42s&ab_channel=TPT-Wirebonder



Stacked Gold studs

Preferred this solution to increase the gap between ASIC and sensor from 20 µm to 35 µm and thereby decrease coupling between them



Test-beam occupancy map of ALTIROC with double gold studs + irradiated LGAD sensor



- High connection yield, reproducibility, low temperature process
- Only for large pitch (>100µm), large pads (>80µm) chips





• Optimised ENIG plating tested on many different configurations

• Functional chips, with different pad size, pitch, chip size...

• Different approaches studied for hybridisation

- ACF, ACP, NCP, Gold Studs
- Successful flipchip bonding of different chips with different sizes
 - Optimisation of bonding parameters (pressure, time, temperature)
- Reliability tests in climate chamber (ongoing)
 - Good results for both the ACF and the ACP





ENIG plating results on test structures

Timepix3 type daisy-chain test structures, 22x22 µm pads and 55 µm pitch



Timepix 3 type daisy-chain device test structure (14x14mm)

Excellent ENIG results:

- Good bump homogeneity
- >99% of 65536 pads correctly plated
- Bumps height: 10 μm (± 0.5 μm) 55min deposition





Small pitch/small pads test structures, <u>20 µm pitch</u>, <u>10x8 µm rectangular pad</u> <u>size</u> (High connection density)



Small pitch/small pads test structures test structures (3.2x3.2mm)

Excellent ENIG results:

- Good bump homogeneity
- >99% of 16384 pads correctly plated
- Bumps height: 4.5 μm (± 0.2 μm) 25min deposition







ATLAS HGTD LGAD sensors <u>Functional chips</u> 1.3mm pitch, 90 µm diameter pads

Good ENIG results:

- Homogeneity of bumps achieved with no overplating
- 100% of pads correctly plated (225 pads)
- Bumps height: 8.5 μm (± 0.7 μm) (1h deposition)

Optical microscope, 62° tilt





Optical profilometry after ENIG plating







4000

2000

1789







Test dedicated daisy-chain chips on glass wafer







Daisy chain devices produced at FBK

Designed to validate interconnect yield, electrical resistance, thermo-mechanical stress

- 6" glass wafers, 625 µm thick
- Varying Bonding area, pad size and pitch, matching different target applications

https://zenodo.org/records/7310324



Challenges of initial platings





ENIG plating on high connection density chips (ex: CLICpix2, 12µm pads; 25µm pitch) !!



Characterisation of ENIG plating



EP R&D

Process flow documentation





		Computing this:	
Given Data	3. Observed Proportion of Good Groups	ppprox 0.968	
• Total number of samples: 65, 536.	From the test results, 29 out of 72 groups are good.	Thus, the probability that a single sample is good is approximately 96.8% .	
• Samples are grouped into 72 groups of 28 samples each.	Therefore, the observed proportion of good groups is:		
Out of these 72 groups:	$\hat{P}(\mathrm{group\ good}) = rac{29}{72} pprox 0.4028$		
• 29 groups are good.	Since the observed proportion of good groups is an estimate of $P(\mathrm{group}\ \mathrm{good})$, we have:	5. Estimating the Total Number of Good Samples	
• 43 groups are bad.	$P(ext{group good}) = p^{28} = \hat{P}(ext{group good})$	To estimate the total number of good samples among the $65,536$ samples, multiply p by the total	
	Substituting the observed proportion:	number of samples:	
. Probability That a Group is Good group of 28 samples in that group are good.	$p^{28} = rac{29}{72}$	$N_{ m good} = p imes 65,536$ Substituting $p pprox 0.968$:	
et p represent the probability that a single sample is good. he probability that a group of 28 samples is good is then given by:		$N_{ m good}pprox 0.968 imes 65,536pprox 63,442$	
$P({\rm group}\;{\rm good})=p^{28}$	4. Solving for p To find p , take the 28 th root of $\frac{29}{\pi_2}$:	Final Results:	
onversely, the probability that a group is bad is:	$\sqrt{20}$	1. Probability that a single sample is good: $ppprox 0.968$ (96.8%).	
$P({\rm group} \ {\rm bad}) = 1-p^{28}$	$p=\left(rac{29}{72} ight)^{23}$	2. Estimated number of good samples: $N_{ m good}pprox 63,442.$	
		This means that approximately $63,442$ samples out of $65,536$ are good, based on the group test results.	



Setup:

Setup

- DUT: Timespot-1 Hybrid on Tspot-1 board
- Clock generator
- FPGA and dedicated mezzanine.
- IIC interface

Device exposed to Sr90 source





Approach

Mutiple acquisition runs performed

Method:

- Distribution of the Time Over Threshold analysed
 - TOT proportional to released charge
 - Set a cut below 3 ns which is considered mostly noise contribution
- Hit map generated after setting the threshold on the TOT



15

25

30

Channel X [#N]



Time over threshold

Bonding efficiency

Due to intrinsic design flaws of the hybrid it's not possible to determine exactly the bonding efficiency

TCT has been considered but the already very thick support wafer still attached on the active you volume absorbs most of the NIR radiation

Bonding efficiency estimated by applying an increasing threshold on the counted events pe channel

- Above 5 counts per channel, trend is more constant.
 - We conclude that efficiency estimation is at the lowest 85.5 %

Bonding Efficiency based on counts per channel



