

Caribou: A versatile data acquisition system for silicon pixel detector prototyping

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Caribou is a versatile data acquisition system used in multiple collaborative frameworks (CERN EP R&D, DRD3, AIDAInnova, Tangerine) for laboratory and test-beam qualification of novel silicon pixel detector prototypes. The system is built around a common hardware, firmware and software stack shared across different projects, thereby drastically reducing the development effort and cost. It consists of a custom Control and Readout (CaR) board and a commercial Xilinx Zynq System-on-Chip (SoC) platform. The SoC platform runs a full Petalinux distribution integrating the custom software framework (Peary) and a device-specific build of the common FPGA firmware (Boreal) or any other custom firmware. The CaR board provides a hardware environment featuring various services such as powering, slow-control, and high-speed data links for the target detector prototype. Boreal and Peary, in turn, offer firmware and software architectures that enable seamless integration of control and readout for new devices. While the first version of the system used a SoC platform based on the ZC706 evaluation board, migration to a Zynq UltraScale+ architecture is progressing towards the support of the ZCU102 board and the ultimate objective of integrating the SoC functionality directly into the CaR board, eliminating the need for separate evaluation boards. This talk describes the Caribou system, focusing on the latest project developments and showcasing progress across its hardware, firmware, and software components.

Type of presentation (in-person/online)

in-person presentation

Type of presentation (I. scientific results or II. project proposal)

I. Presentation on scientific results

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