Contribution ID: **79** Type: **WG1 - Monolithic Sensors**

Performance studies of the CE-65v2 MAPS prototype structure

Thursday 5 December 2024 16:00 (20 minutes)

With the next upgrade of the ALICE inner tracking system (ITS3) as its primary focus, a set of small MAPS test chips have been developed in the 65 nm TPSCo CMOS process. The Circuit Exploratoire 65 nm (CE-65) focuses on the important characterisation of the analogue charge collection properties of this technology. The latest iteration of sensor design in this line of development is CE-65v2, which was produced in different processes (standard, with a low-dose n-type blanket, and blanket with gap between pixel) and pixel pitches (15, 18, 22.5μm). The comparatively large pixel array size of 48×24 pixels in CE-65v2 allows, among other benefits, to study the uniformity of the pixel response.
This year, the CE-65v2 chip was characterised in a test beam at the CERN SPS. A first analysis showed that hit efficiencies of $\geq 99\%$ and spatial resolution better than 5μm can be achieved for all pitches and process variants. For the standard process, with a pitch of 15μm, spatial resolutions below 3μm are achieved, thanks to larger charge sharing between the pixels, in line with the requirements of FCC-ee vertex detectors.
This contribution further investigates the data collected at the SPS test beam. The large amount of statistics collected, thanks to the large sensor size and efficient data taking, allow for detailed in-pixel studies to see the efficiency and spatial resolution as a function of the hit position within the pixels, again comparing different pitches and process variants.

Type of presentation (in-person/online)

in-person presentation

Type of presentation (I. scientific results or II. project proposal)

I. Presentation on scientific results

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Session Classification: WG1 - CMOS technologies