



# Development of next generation particle beam telescope using OBELIX chips

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On behalf of OBELIX VTX Group

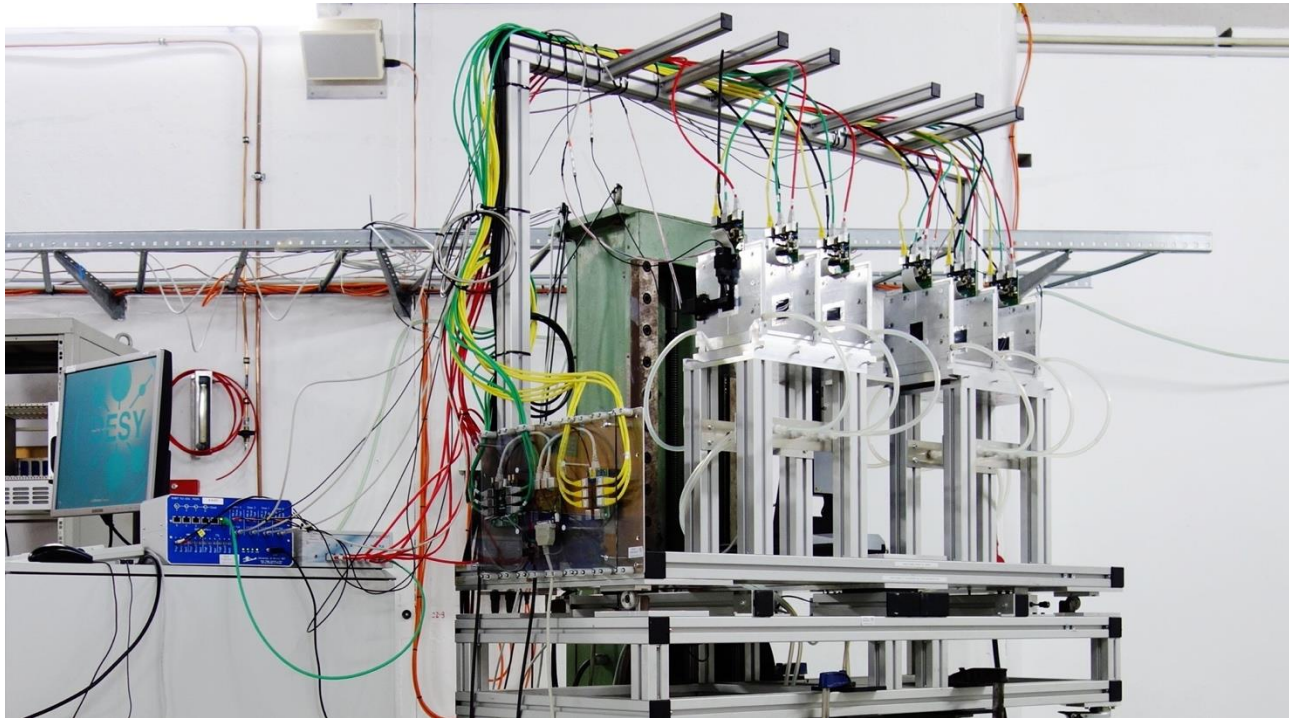
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# OBELIX-based Telescope

Intelligent, thin, fine-pitch vertex detector prototype in the context of a *full*  $e^+e^-$  tracker demonstrator design

→ In other words: A large area (multi-chip assemblies) DMAPS particle beam telescope



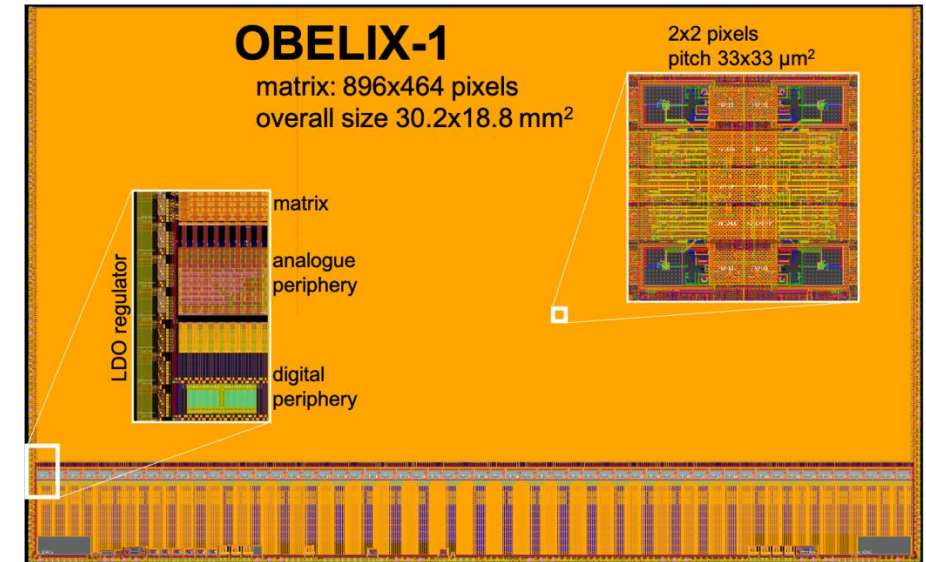
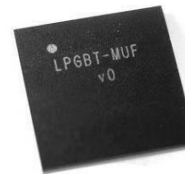
Bring the existing infrastructure to the next level, together with a number of international partners:

- 6 large area high-resolution detector planes
- DAQ and TRG
- Compact integration
- Software, monitoring, interlocks, ...

Plan to request a permanent location at CERN SPS H6 line and a copy for the new test beam line at KEK. DESY test beam infrastructure for development and commissioning.

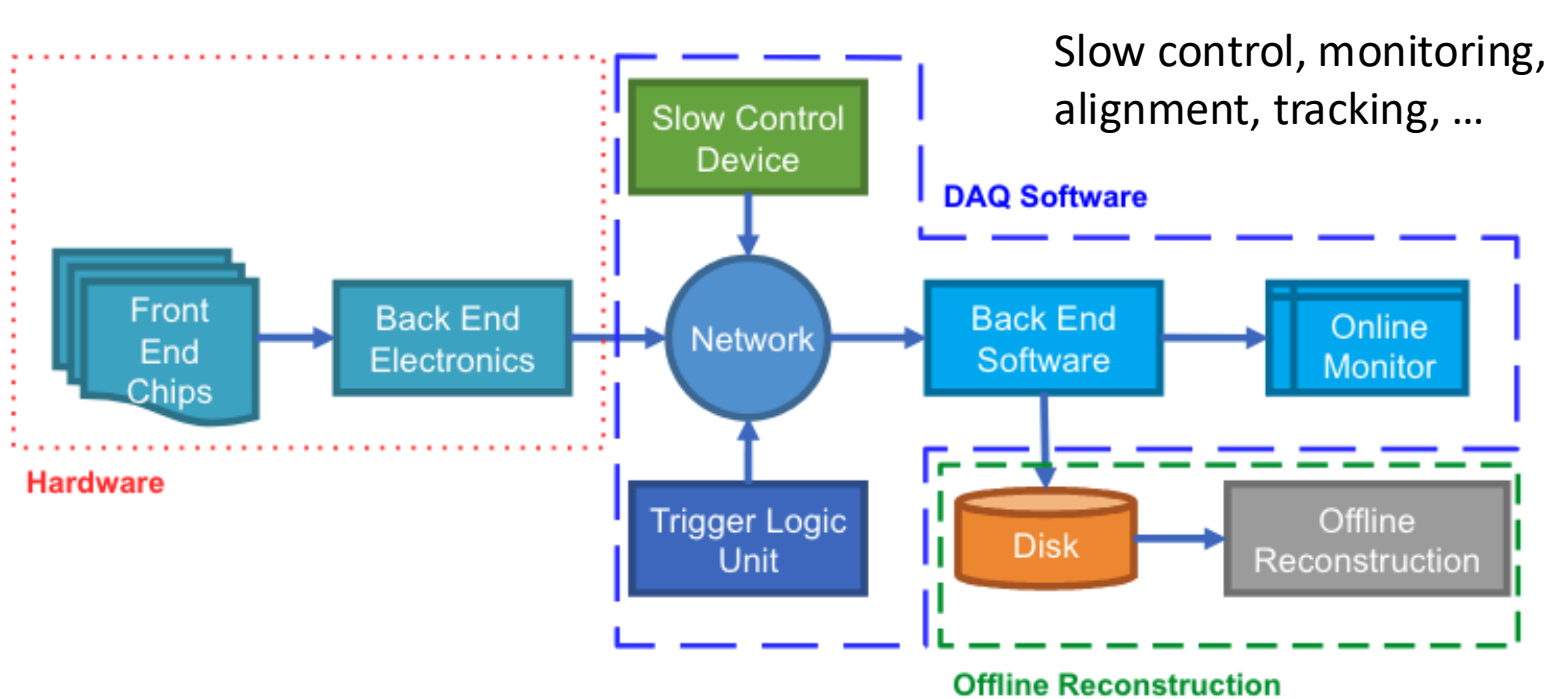
# System Configuration – Some choices (TBD)

- Sensors: OBELIX -1 – Versatile tracker matrix (2x3 cm<sup>2</sup>)
  - 33x33 μm<sup>2</sup> pitch, 50 μm thick, 100 ns time stamps
  - Trigger handling 30 kHz, 120 MHz/cm<sup>2</sup>
  - Precision timing module (5 ns for < 10 MHz/cm<sup>2</sup>)
  - Low granularity hit information for track trigger
- Transceiver: IpGBT, GBTX,...
- (Timing: Scintillators, SiPM, LGADs, PicoPix, ...)
- DAQ: PCIe40 miniDAQ
  - Real time event reconstruction
  - System to handle large heterogeneous detectors
- Synchronization: AIDA TLU
- Power supplies, cooling ,...

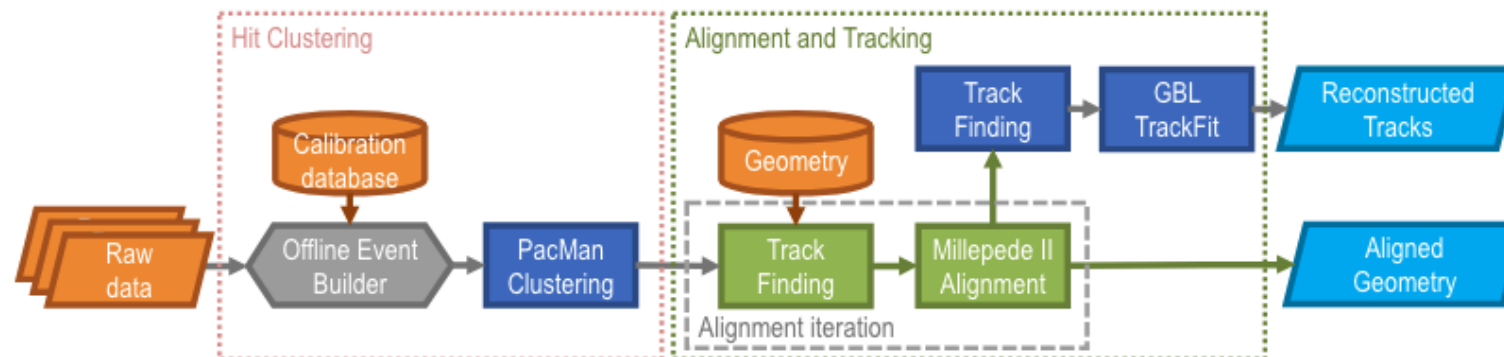




# System Configuration – Much more than hardware



Reuse as much as possible  
 Run control  
 Data collector  
 Producers



# Schedule and Milestones

Identify critical components and secure them as soon as possible (IpGBT, PCIe40, TLU)

	H1	H2	H3	H4	H5	H6	H7	H8
Verification OBELIX (test beams, irradiations)	█	█						
Integration IpGBT on miniDAQ	█	█						
OBELIX full chain		█	█					
Multiple OBELIX chip readout				█	█			
Synchronization TLU (TRG, busy/data)			█	█	█			
Slow Control and Monitoring	█	█	█					
Mechanics (module and overall)		█	█	█				
Integration (Laser, beam)						█	█	
Including DUT								█

→ Need to think in long term maintenance and support after delivery and commissioning

# Summary

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OBELIX-based telescope is a natural step forward in the DMAPS family to equip our test beam lines  
→ Interesting added value wrt available systems. Large area, fast, handling complete detector systems.

Case for DRD3 Common Project, linking with AIDAInnova activities

DRD3 groups working on OBELIX are interested in pursuing this development. First informal contacts with:  
France, UK, Germany, Austria, Italy, Japan, Spain, China

Call for kick-off meeting will happen soon to start defining concrete action plan. Get in touch if interested.

OBELIX Telescope Working Groups:

WG1: Sensor characterization

WG2: Interfaces

WG3: DAQ

WG4: Integration

WG5: Mechanics and cooling

WG6: Software (configuration, slow control, ...)

WG7: Alignment and Tracking

**WG8: Long term operation and support**

# TJ-Monopix Family

### DMAPS in TJ 180 nm: Concept

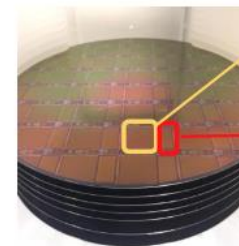
- **Small sensor capacitance ( $C_d$ )**
  - Key for low power/low noise
- **Radiation tolerance challenges**
  - Modified process
  - Small pixel size
- **Design challenges**
  - Compact, low power FE
  - Compact, efficient R/O

W. Snoeys et al. <https://doi.org/10.1016/j.nima.2017.07.046>

$C_d \leq 3fF$

$P \approx \frac{S}{N} \approx \frac{Q}{C_d}$

## Large scale demonstrator chip development



TJ-Investigator characterization	TJ-Monopix1 & MALTA Design	TJ-Monopix1 & MALTA Submission	Mini-MALTA sub. with process fixes	TJ-Monopix1 resub. process fixes & Cz	TJ-Monopix2 & MALTA2 Design	TJ-Monopix2 & MALTA2 Submission	TJ-Monopix2 Characterization	"OBELIX" Design
Q2 2016	Q4/2016	Q3/2017	Q3/2018	Q2/2019	Q2/2019	Q3/2020	Present	- Future plans -

Full scale System-ready: LDO, CDR, memory etc.

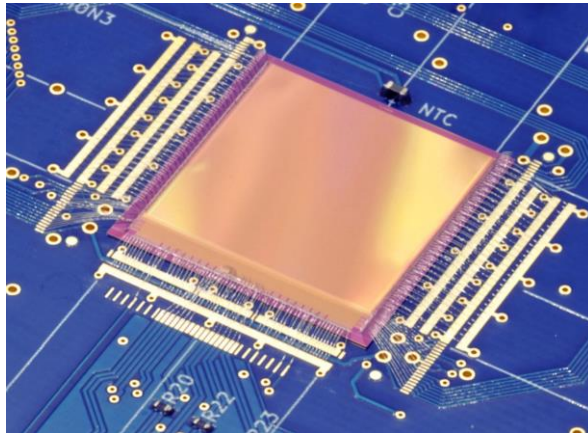
Present





# Increasing Complexity

From single reticles to all-silicon ladders



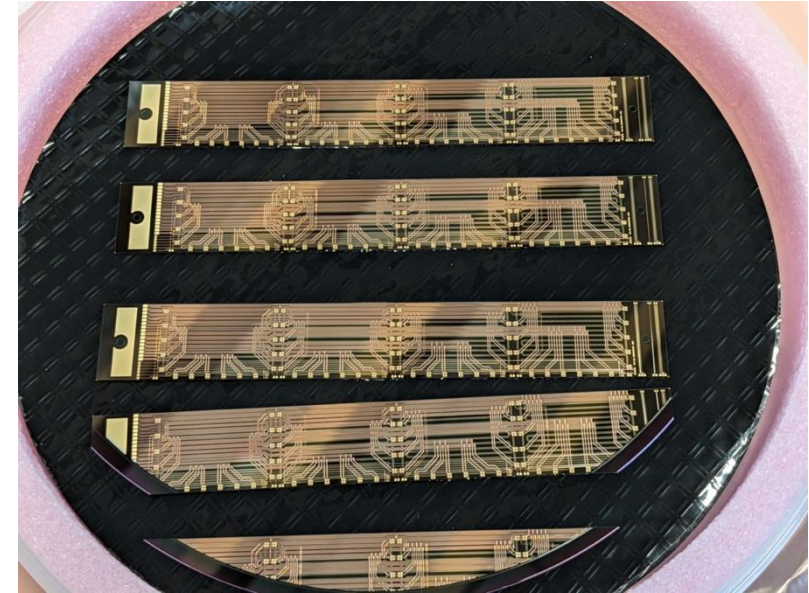
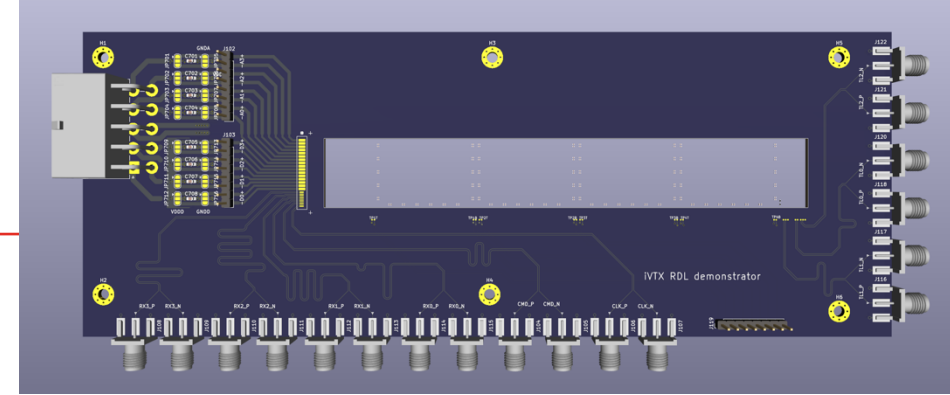
TJ-Monopix2 single chip → OBELIX1 (TowerJazz 180 nm)

Size: 3x2 cm<sup>2</sup>

Pitch: 30x30 μm<sup>2</sup>

Time: 25-100 ns

Resolution, efficiency, charge collection properties,  
radiation hardness



Multi-reticle ladder

Size: 12x2 cm<sup>2</sup> (4x chips interconnected)

Full front and backside processing

Impedance, continuity of the RDL, integrity data lines

Selective etching



# VTX Readout Concept

