

Extra flip-chip bonding results

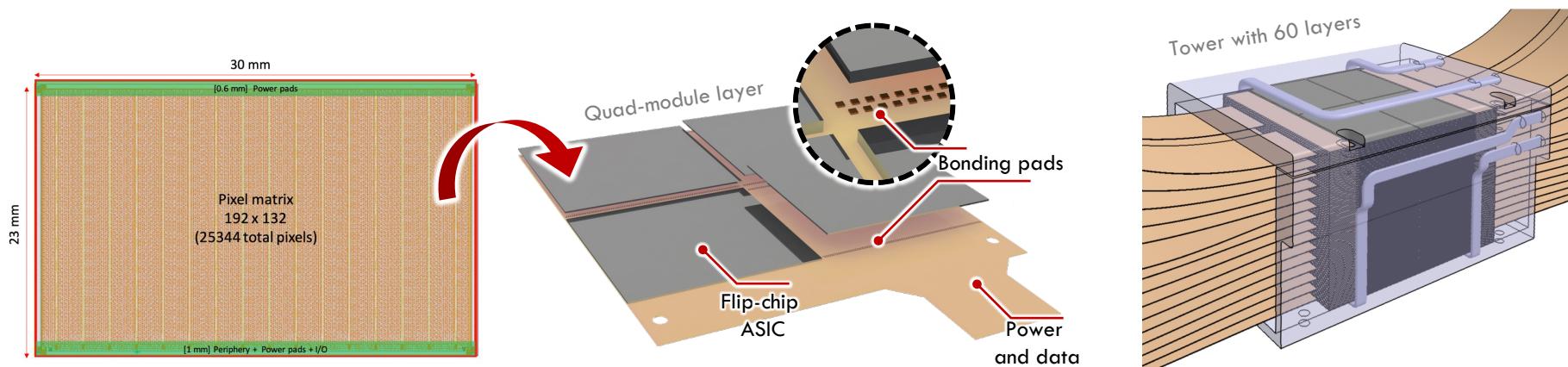
The 100 μ PET scanner

ASIC, module/layer, tower

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□ Multi-layer stack of CMOS imaging sensors

- **100 μ PET MAPS:** 130 nm SiGe BiCMOS; **2.3 x 3 cm²**; **150 μ m pixel pitch**; **270 μ m thick**; **4 kOhm*cm p-substrate**; **~0.5W power**
 - Designed foreseeing flip-chip bonding, the size and pitch of the bonding pads allows integration with standard PCB/FPC production
- Single silicon detection layer composed by **2x2 ASICs** flip-chip to a flex printed circuit, covering **24 cm²**
 - In addition to the thin MAPS, a 50 μ m thick layer of Bismuth is added above the MAPS to increase the photon conversion rate
- **60 detection layers + cooling block compose each scanner **tower****, with 4 towers per scanner (for a grand total of **960 chips!**)



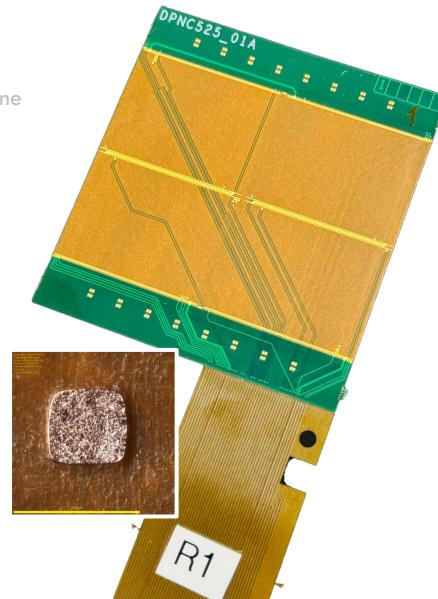
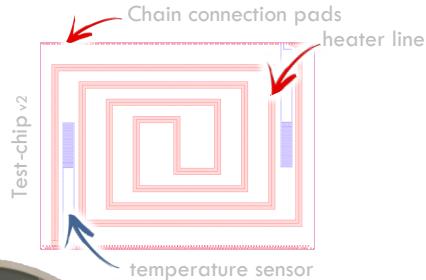
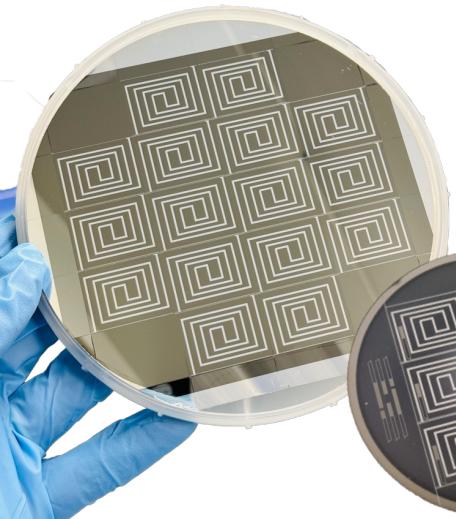
100 μ PET module demonstrator

Design and production

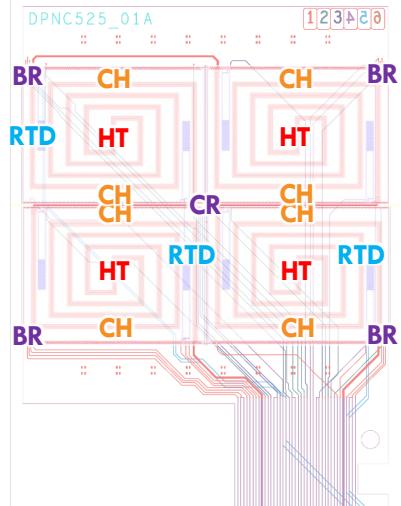
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- **240x** 300 μ m thick test chips:
 - 4x 4-wire single-bond resistance, 1x resistive heater (1 μ m thick Al), 2 RTDs (PT1000-ish), 1x 162-pads chain and 1x 82-pads chain
 - 4x 4-inch wafers produced at NMP-FCBG and 15x 6-inch wafers from CMI (no RTDs)
- **60x** test flex (+ 2x beck-end prototype system)



3x Resistive Temperature Detectors
5x Bond Resistance (4-wires)
4x Heaters in series
8x Chains (4x w/ 162 pads, 4x w/ 82)



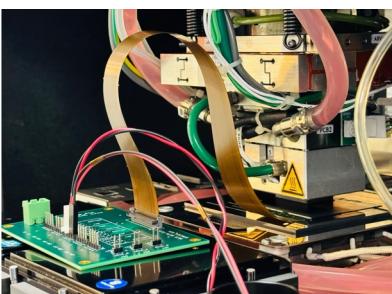
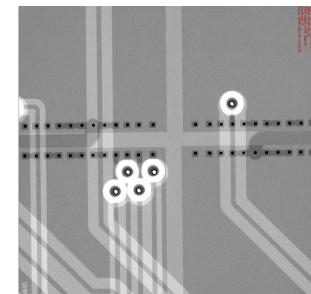
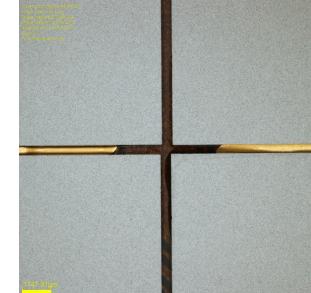
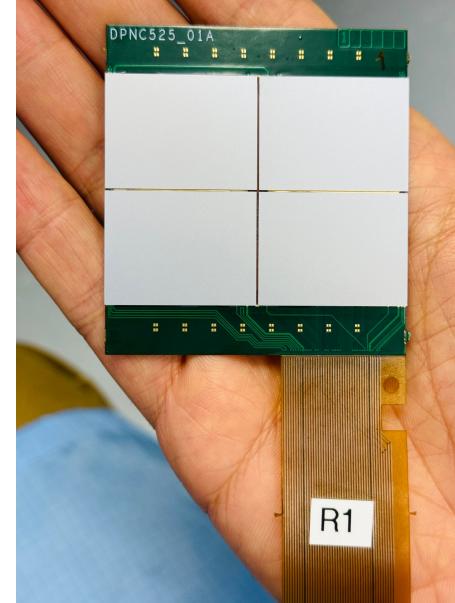
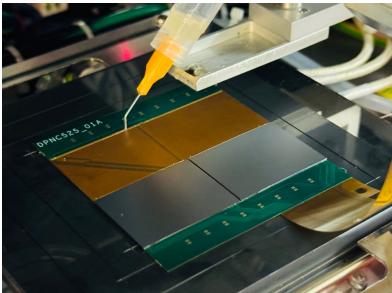
100 μ PET module demonstrator

Reference module

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- Bonding reference module with flip-chip machine
 - We are putting in place the data-base tracking, handling the temporary storage, module quality control tests and etc



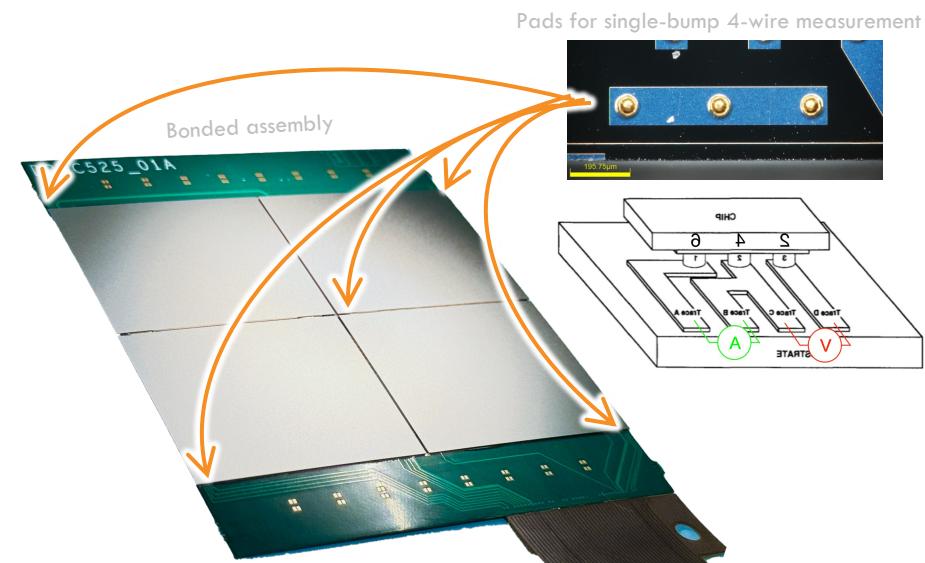
100 μ PET module demonstrator

Reference module characterization

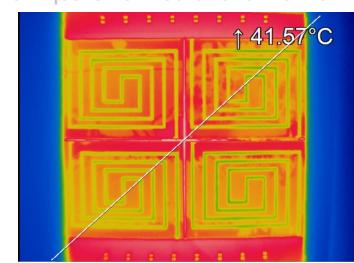
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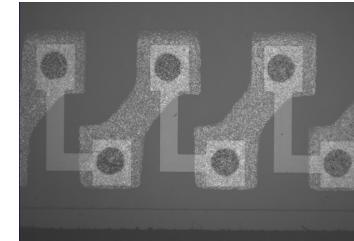
- Bond resistance of $\sim 10 \text{ mOhm}$ and uniform over module's 4 corners and center
- Chains of pads indicating no open connection in ~ 1000 pads (**bonding yield >99.9%**)
- Heater system is working as expected, with 8°C increase in temperature at nominal module power (2W)
- New assembly jig for simultaneous 4-chip bonding (we need 240 4-chip modules in total!)



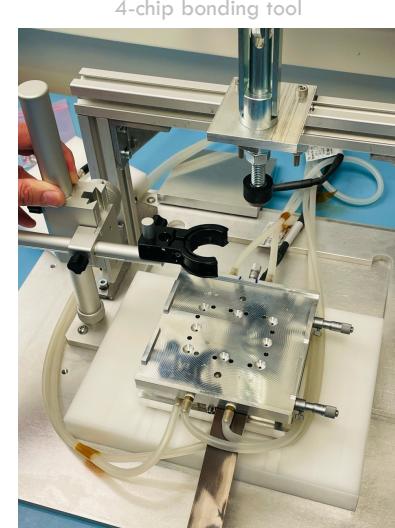
Pads for single-bump 4-wire measurement



Power injection on heater and thermal image



Pads for chain continuity test

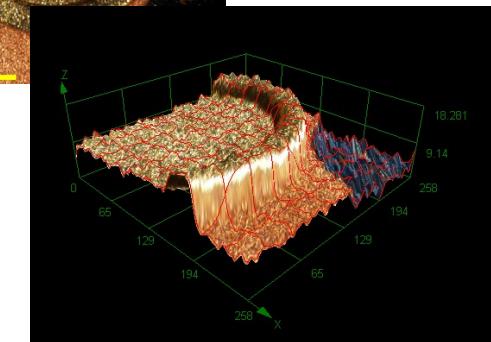
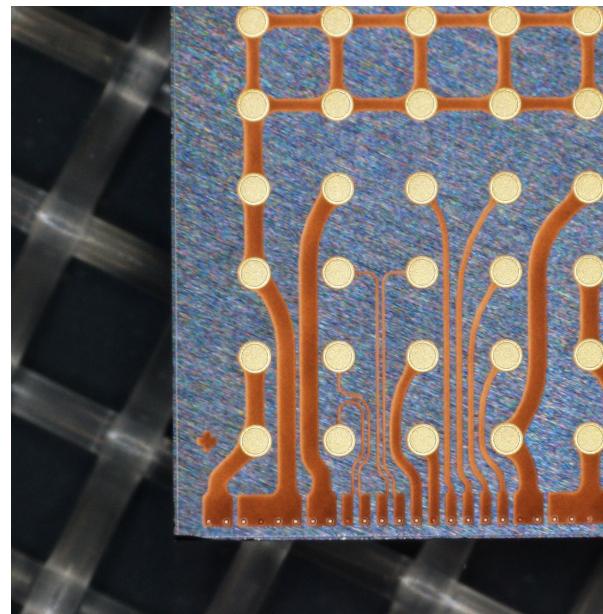
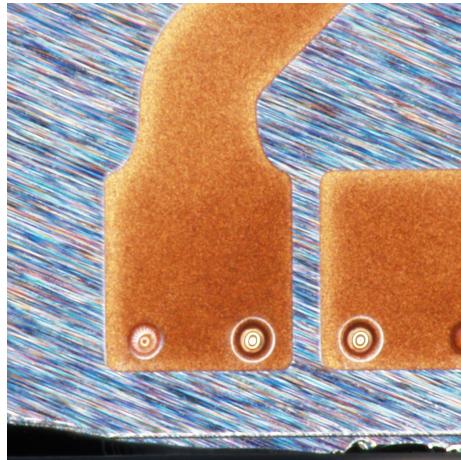


4-chip bonding tool

Timepix4 TSV bonding with ACP

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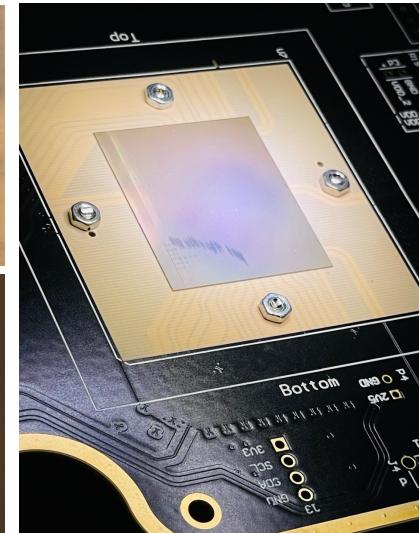
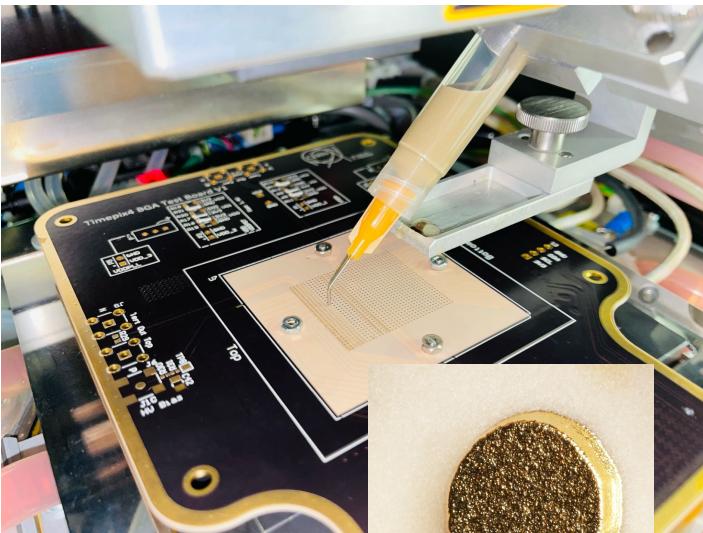
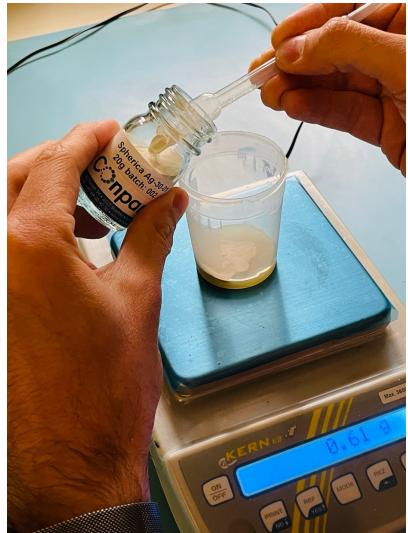
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Timepix4 TSV bonding with ACP

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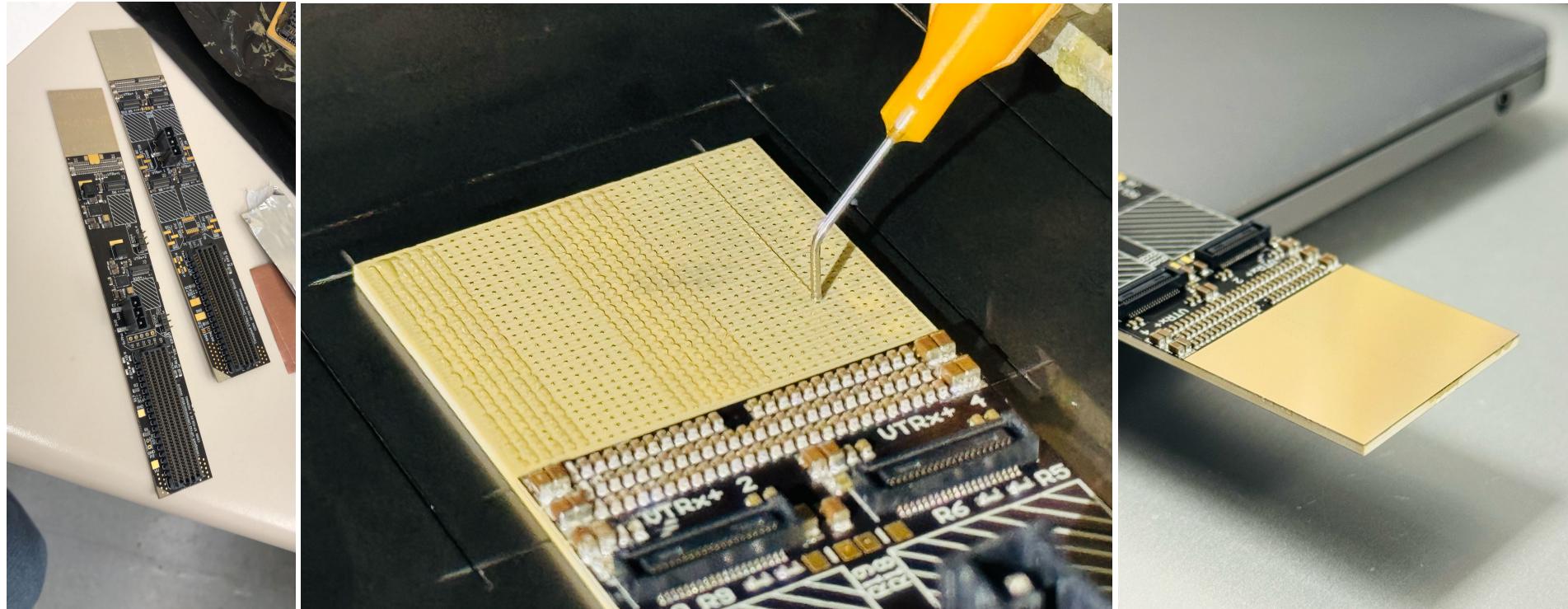
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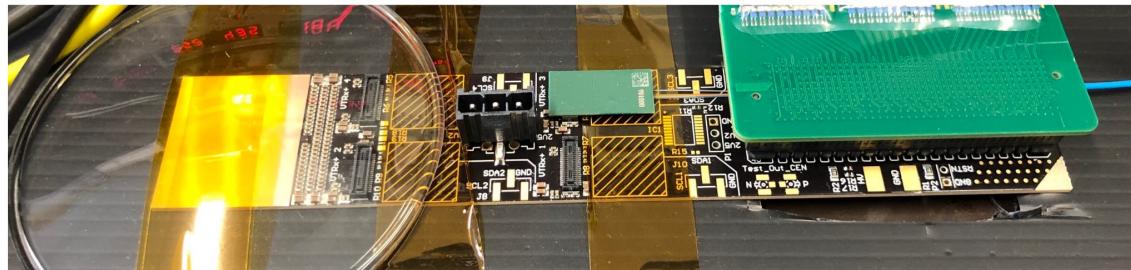


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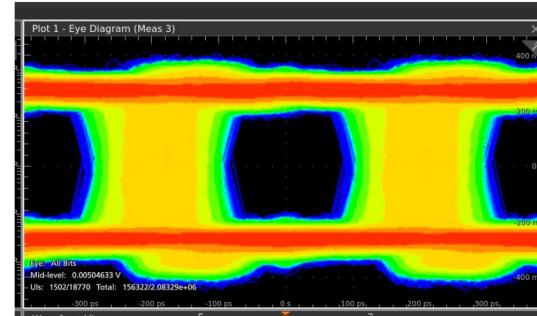
5. First Results and Future Work



Opto-demonstrator module

Timepix4.1 TSV, bonded with ACP glue

- Eye diagram through **optical fiber** at 2.56Gbps.
- This version of the chip has **problems with jitter**.
- Waiting for TSV processing of Timepix4 V3



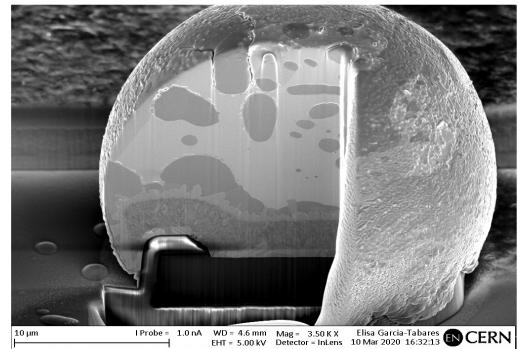
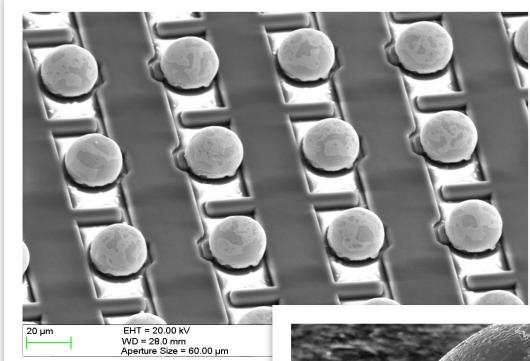
Timepix4 Hybridization with Cu pillars

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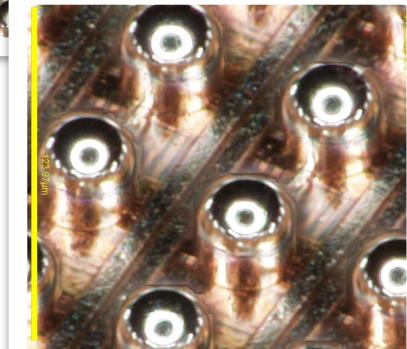
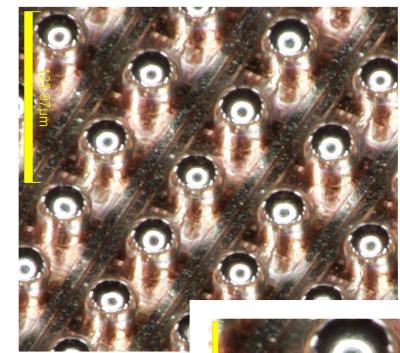
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Hybridization pads/bumps

Standard (SnPb) bump-bonds



**“New” copper pillars
(with Sn1.8Ag caps)**

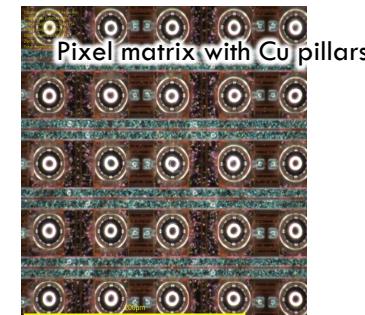
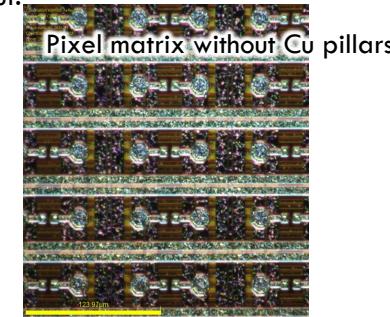
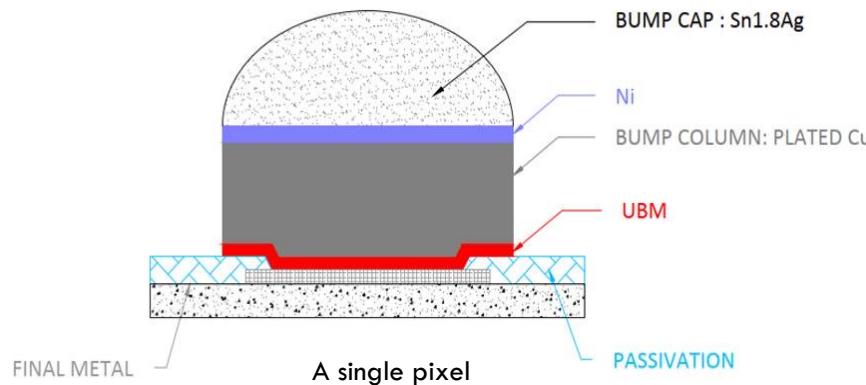
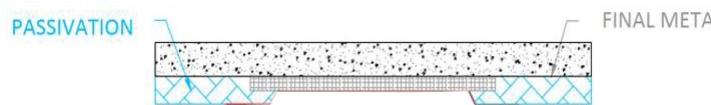


Timepix4 Hybridization with Cu pillars

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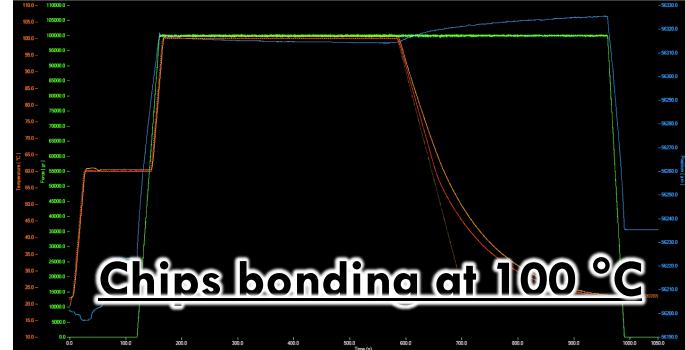
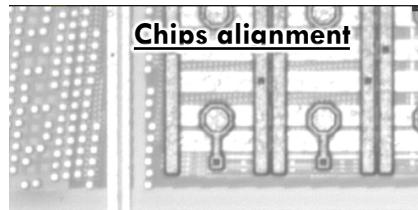
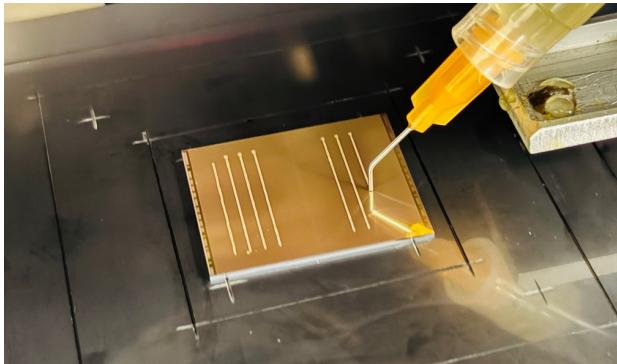
The plan: Bonding two Timepix4, one with Cu pillars and the other without.



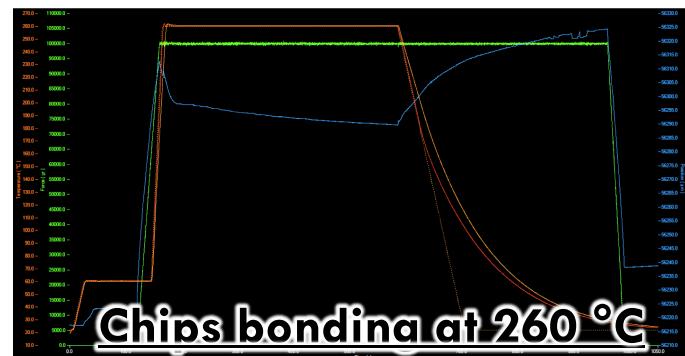
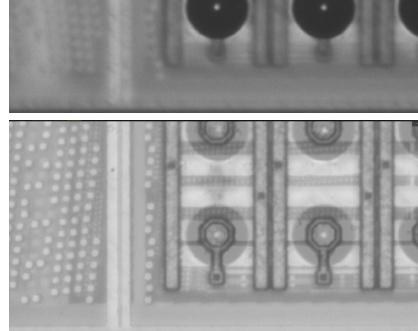
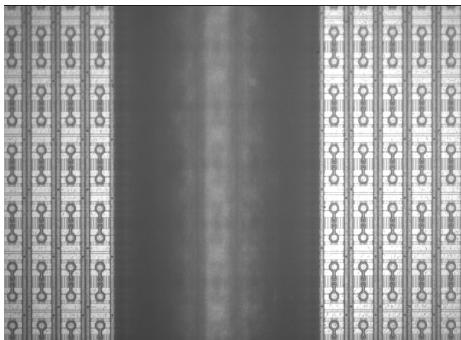
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Chips bonding at 100 °C

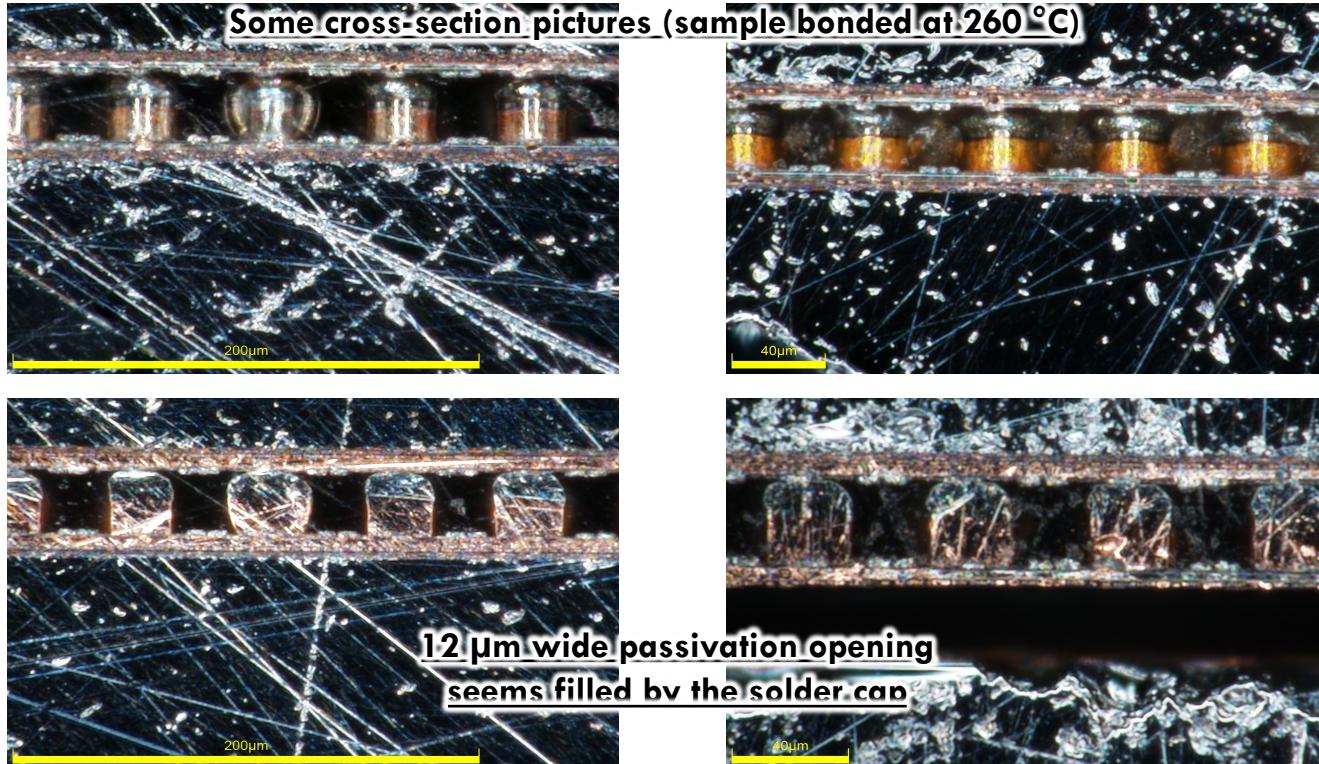


Chips bonding at 260 °C

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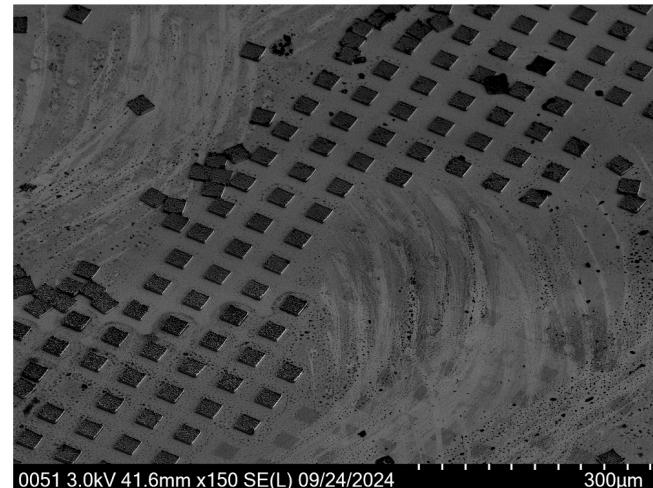
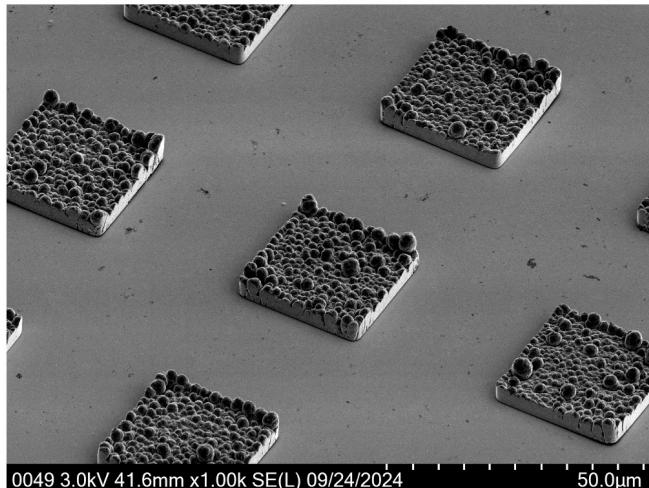
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Targeting 10µm

- Comments:
 - Correct Height
 - poor Adhesion



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Time calculation and observation

20 minutes process gives approximately $20\mu\text{m}$

- Comments:
 - The pillars grew higher than the pattern because of a too long process time
 - Non-uniform coating
 - Weak adhesion

