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Evaluation of OpenPDKs and OpenSource Design Tools for DMAPS

A WP1 proposal?

Or rather a WG1 proposal/common project

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OpenSource? OpenPDKs?

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Issue:

- We use “large” and somewhat exotic process nodes that are constantly in danger of becoming unavailable (change of ownership, foundry oversubscribed or going bankrupt)
- Due to proprietary processes and PDKs, we cannot just transfer our designs to alternative processes/ foundries and partially not even discuss about details with collaborators thanks to NDAs

Google + skywater TECHNOLOGY

FOSS 130nm Production PDK
github.com/google/skywater-pdk

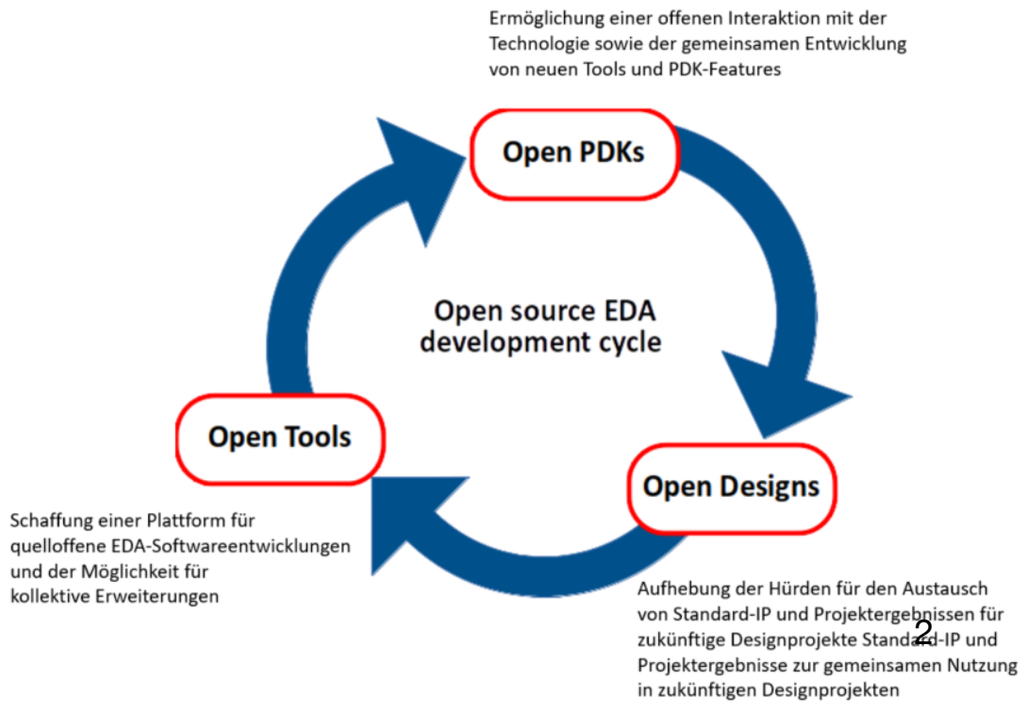
IHP-GmbH/**IHP-Open-PDK**

130nm BiCMOS Open Source PDK, dedicated for Analog, Mixed Signal and RF Design

12 Contributors · 23 Issues · 4 Discussions · 317 Stars · 43 Forks

Solution/Proposal:

- Use OpenSource!
  - If the PDK (and ideally the process) is OpenSource, other foundries could step in and offer to process our ASICs
  - The usage of OpenSource chip design tools would save cost and allow for commercial spin-offs without Cadence license fees



OpenSource!

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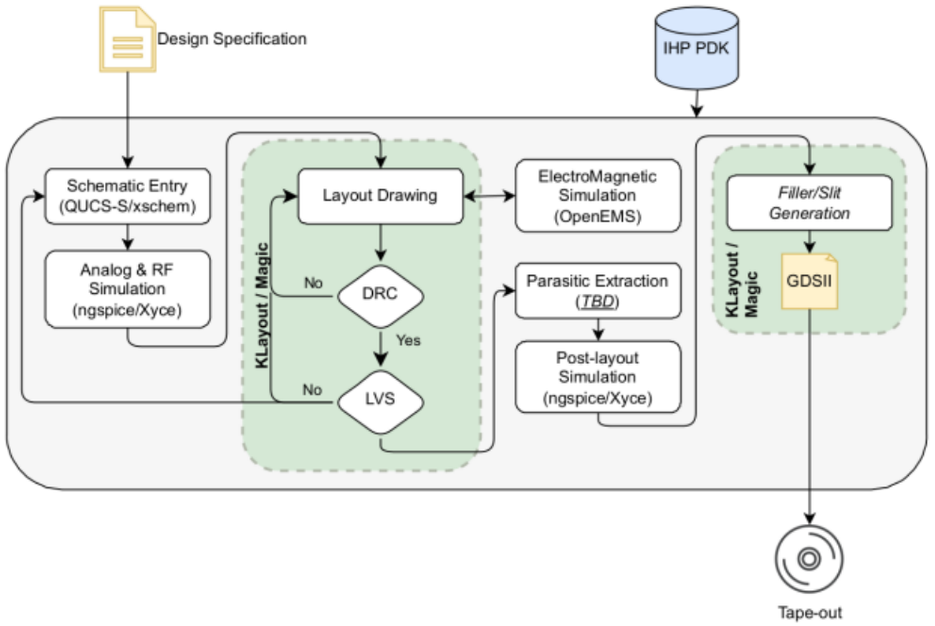
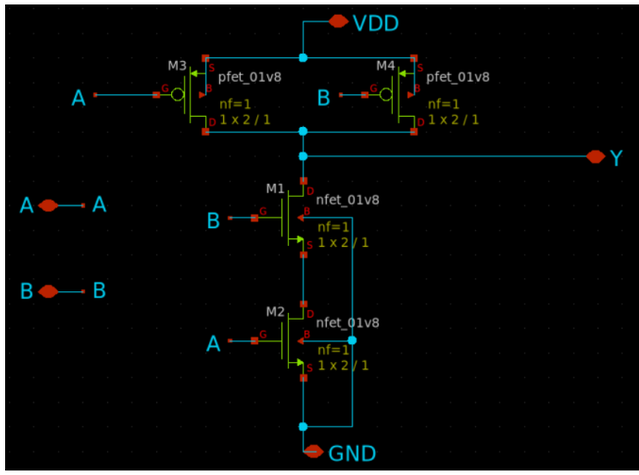
How to start?

- Evaluate OpenPDKs: Are the OpenPDKs (and the underlying processes) actually equal to their proprietary counterparts?
  - SkyWater 130nm
  - IHP 130nm SiGe
  - ...
- Evaluate Open-Source-EDA Tools
  - How to replace Cadence for Mixed Signal chips? Is this desirable?

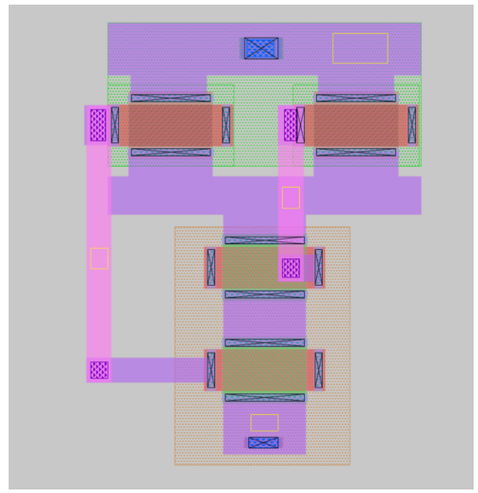


- First steps:
  - Design a simple analogue test chip, submit it via MPW/ tiny tapeout, see whether it works
  - Re-submit a known chip with the OpenPDK and see whether it works

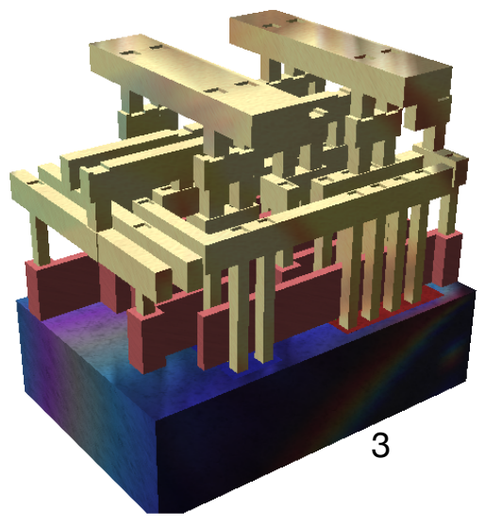
Schematic



Layout



Tapeout



Why am I here (again) today?

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- Is this a WP1 proposal?
  - Does not really match the strategic research goals set out in the research proposal
  - But addresses one of the processes mentioned and might also relate to RG1.5?
  - Is just “evaluate” too small as a project?
- Rather a WG1/common project proposal?
  - Would be more than happy to not pursue this alone
  - Project is probably “cheap” (no software cost, tiny tapeout already paid for), but DRD3 approval and common fund contribution would help with PCBs and applying for national funding for (re-)submission of a larger chip
- Please reach out to me if you might be interested in joining the effort!

DRD3 - Solid State Detectors
- Research Proposal (Version 3.1) -

DRD3 Proposal Team

May 27, 2024

WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: $\leq$3 μm position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRad
RG 1.5	Low-cost large-area CMOS sensors

D1.1	Several MPW1.1 submissions in the identified technology processes (TJ/TSI 180 nm, LF 110/150 nm and IHP 130 nm in 2024, and TJ 65 nm in 2025)
D1.2	Several MPW1.2 submissions in the identified technology processes (TJ/TSI 180 nm, LF 110/150 nm and IHP 130 nm in 2026, and TJ 65 nm in 2027)