# FCC-SEED
# A vertex detector concept for FCCee

## Expression Of Interest for a Vertex Detector at FCCee :

FCC Snail-shape vErtEx Detector (FCC-SEED)

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[5]laboratoire AstroParticule et Cosmologie, France

General Expression of Interests, not yet attached to a specific detector concept

# Introduction and context

- In2p3 (France) has a long standing expertise in the R&D, sensor designs and construction of pixel/vertex detectors.
  - Strong contributions in ATLAS/CMS upgrades but also STAR-HFT (MIMOSA-28) , ALICE ITS-2 (ALPIDE), ITS-3 (MOSAIX), CBM-MVD (MIMOSIS), Belle-II VTX upgrade (OBELIX), etc.

- We want to participate to the creation of vertex detector concept for FCCee based on CMOS-MAPS sensors, with contributions to the following topics :
  - R&D for MAPS sensors, within the DRD3,
  - A new approach for detector geometry design, based on curved sensors,
  - Mechanics and integration,
  - Sensor simulations and detector full-simulation for evaluation of performances.

- This is a national effort, meant also to structure our community. But international collaboration is of course absolutely mandatory !

# Vertex detector requirements reminder

FCCee

$$\sigma_{d_0} = a \oplus \frac{b}{p\sin^{3/2}\theta}$$

$a \simeq 5\,\mu m$; $b \simeq 15\,\mu m\,GeV$

$b \sim r_0\sqrt{material}$

$a \sim \sqrt{r_0}$

- Challenge:
  - How to reach the targeted resolution with an adapted read-out architecture while fulfilling all the other requirements ?
  - How to propose a robust but ambitious VTX concept ?
- Side remarks
  - The Vertex detector has to be integrated in the whole tracker concept
  - Some considerations depend on the main tracker choice (e.g. timing capabilities, low pT track reconstruction, etc.)

| | | |
|---|---|---|
| Spatial resolution per layer | $\simeq 3$ | $\mu m$ |
| Pixel pitch | 14-20 | $\mu m$ [1] |
| read-out time | $\simeq 500$ | $ns$ [2] |
| Power dissipation | $\simeq 20 - 50$ | $mW/cm^2$ |
| Sensor thickness | $40 - 50$ | $\mu m$ [3] |
| Safety factor on particle rate | 3 | [4] |
| Maximum Hit rate | 75 / 25 | $MHz/cm^2$ [5] |
| Maximum Hit rate | $22.5 \times 10^{-3}$ / $7.5 \times 10^{-3}$ | $hits/mm^2/BX$ [5] |
| Assumed cluster multiplicity | 5 | |
| Fired pixel rate | 375 / 125 | $MHz/cm^2$ [5] |
| Fired pixel rate | 0.33 / 0.11 | $fired\ pixels/mm^2/BX$ [5] |
| Occupancy/pixel/read-out | $3.45 \times 10^{-3}$ / $1.15 \times 10^{-3}$ | $/pixel/readout$ [5] |
| Ionising radiation ($1^{st}$ layer) | 30 / 10 | $MRad/year$ [5] [6] |
| Corresponding Fluence | $\simeq 1.8 \times 10^{14}$ / $6 \times 10^{13}$ | $n_{eq(1\ MeV)}/year$ [5] [7] |

[1] Depending on charge sharing/encoding
[2] Compromise between power dissipation and pile-up at $\sqrt{s} = 91\ GeV$
[3] To allow bending
[4] due to beam background uncertainties estimates
[5] With / without safety factor
[6] assuming beam running 180 days/year, and average incident angle of $\simeq 70^o$.
[7] assuming NIEL factor of $5 \times 10^{-2}$

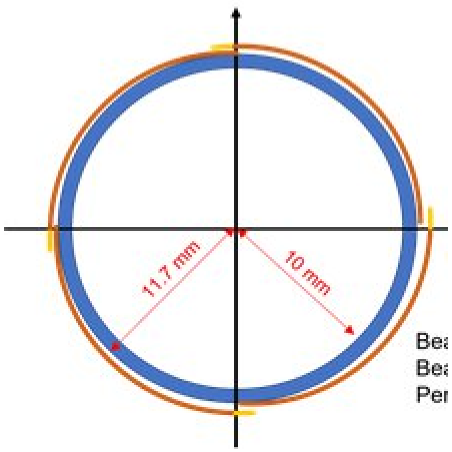
| | thickness ($mm$) | Mat. Budget ($X/X_0$ %) |
|---|---|---|
| Beam pipe[1] | | |
| Au | 0.005 | 0.16% |
| AlBeMet162[2] | 0.35 | 0.14% |
| Paraffin | 1.0 | 0.18% |
| AlBeMet162[2] | 0.35 | 0.14% |
| Total beam pipe | 1.705 | 0.61% |
| Single layer | | |
| Silicon sensor | 0.050 | 0.05% |
| Cables, flex and support | | $\simeq 0.10\%$ |
| Material per layer | | $\simeq 0.15\%$ |

[1] described in [6]
[2] 62% Be and 38% Al alloy
[3] from [7]

# FCC-SEED in a nutshell

- Starting point:
  - Historical approach (CLD, ILD): 3 double ladder + discs: Robust but not optimized for material budget
  - À la ALICE ITS-3 : 3/4 layers with stitched half cylinders
    - Fill factor not 100% per layer
    - Stitching mandatory (impact on design) Pitch ? Power ? Yield ? Fill factor ? Bent radius ?
    - Very competitive for mat. budget but limitations (acceptance, resolution, radius ?)
  - Alternative Proposal: Seed concept = bent ladders
    - Competitive for mat. Budget. AND full azimuthal acceptance

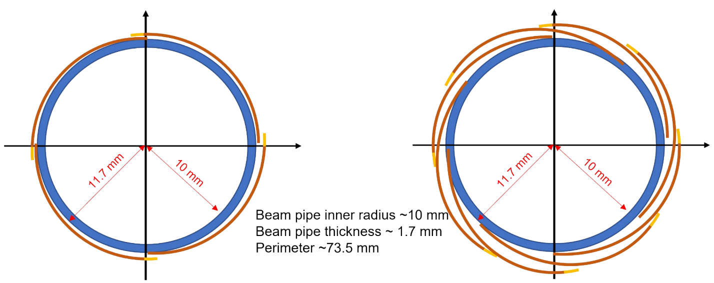
- Concept based on large size curved sensors (DRD8)
  - Smallest possible radius, first hits as close as possible to the collision point,
  - Minimization of the material budget.
- Dedicated R&D for maps (participating to the Octopus project, DRD3-7).
  - Allows to define mid-term milestones (optimizing the spatial resolution first)




- **Coherent developments of sensors, mechanic, integration and simulation.**

# FCC-SEED : geometry concept

- Overlaps to avoid cracks in the acceptance in phi.

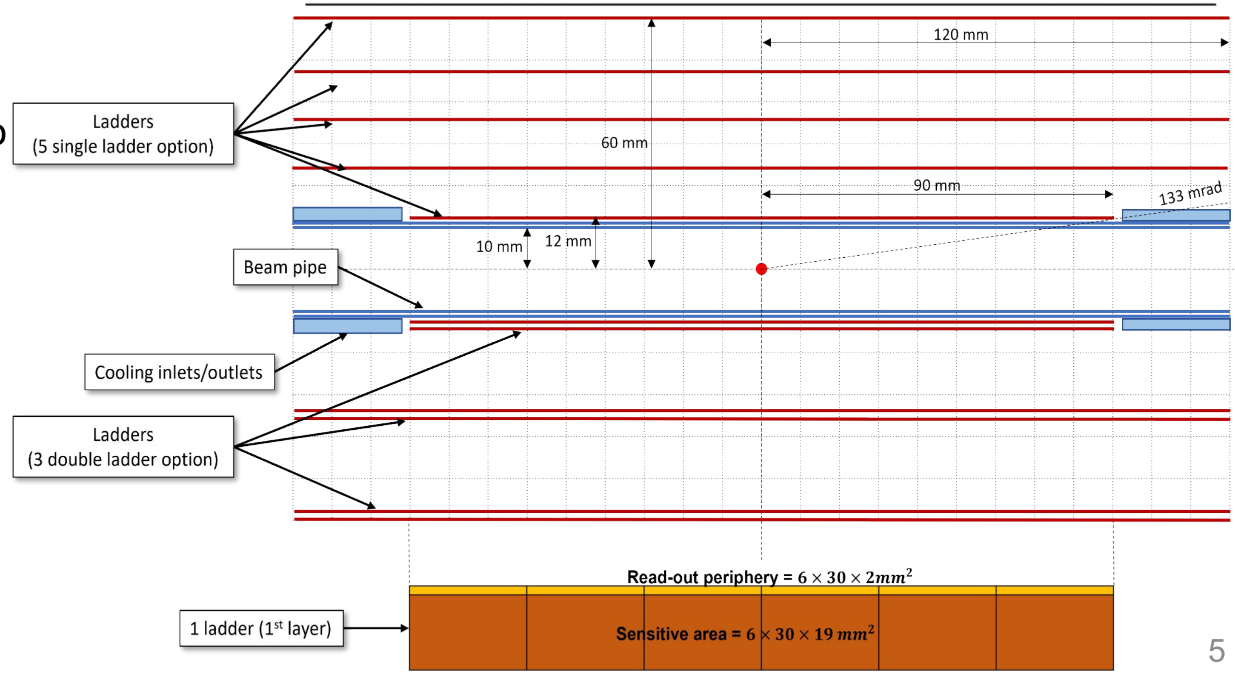



- Ladders: bonding performed along the longitudinal (z) axis.
- Stay flexible
  - Focused on (long) barrel, to be completed by disks.
  - Options to be explored :
    - Possibility of stitching,
    - Double sided vs single sided layers,
    - Layers radius and numbers of layers are free parameters
    - Cooling options (air cooling preferred)

| Layer | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| Radius (mm) | 12-13 | 24 | 36 | 48 | 60 |
| Zmax (mm) | 90 | 120 | 120 | 120 | 120 |
| Perimeter (mm) | 75 | 151 | 226 | 302 | 377 |
| # Chips per ladder | 6 | 8 | 8 | 8 | 8 |
| # ladders | 4 | 8 | 12 | 16 | 20 |

| Layer | 1-2 | 3-4 | 5-6 |
|---|---|---|---|
| Radius (mm) | 12-13 | 35-36 | 59-60 |
| Zmax (mm) | 90 | 120 | 120 |
| Max perimeter (mm) | 82 | 226 | 377 |
| # Chips per ladder | 6 | 8 | 8 |
| # ladders | 4 | 12 | 20 |

| | |
|---|---|
| Single chip dimension | $30 \times 22.2\ mm^2$ |
| Sensitive area chip dimension | $30 \times 19.2\ mm^2$ |



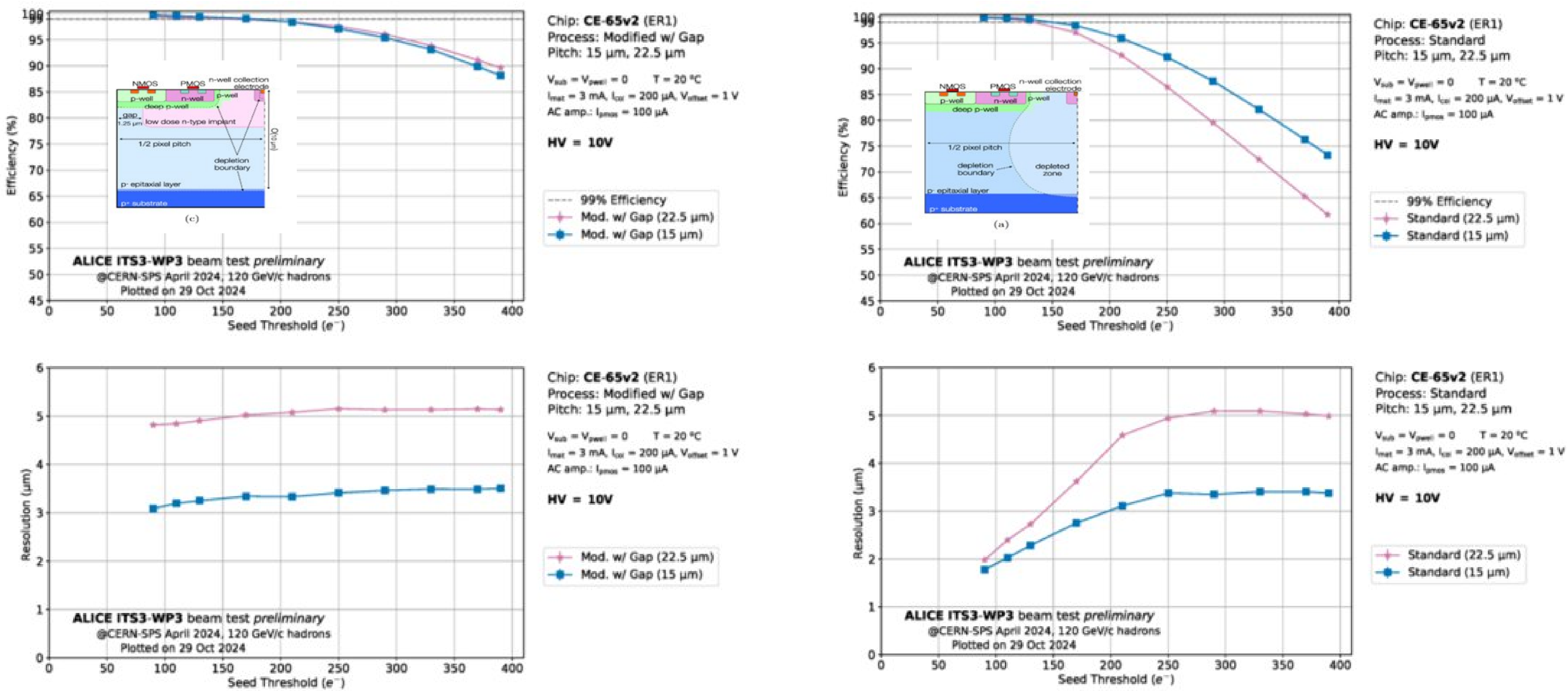
# CMOS-MAPS Sensors R&D

- Long History of CMOS-MAPS R&D inside IN2P3 labs
- Today :
  - IN2p3 involved in full scale sensors : ITS-3 (MOSAIX), CBM-MVD (MIMOSIS), Belle-II VTX upgrade (OBELIX),
  - IN2p3 groups partipate to the TPSCo 65 nm R&D (initiated by CERN and ALICE ITS-3)
- To be pursued inside DRD3/DRD7 trought the OCTOPUS project targeting fine resolution full size prototypes
  - adapted to beam telescope
  - and adressing Higgs factories requirements


## OCTOPUS project

| Institute | Contact | Main areas of contribution |
|---|---|---|
| APC Paris | M. Bomben | Simulations, testing |
| Bonn University | J. Dingfelder | ASIC design, testing |
| CERN | D. Dannheim | Testing, DAQ, ASIC design support (through DRD7) |
| DESY | S. Spannagel | ASIC design, testing, DAQ, simulations |
| ETH Zurich | M. Backhaus | ASIC design, testing |
| FNSPE Prague | P. Svihra | ASIC design, DAQ, testing |
| GSI Darmstadt | M. Deveaux | Simulations, testing |
| HEPHY Vienna | T. Bergauer | DAQ, testing, ASIC design |
| IPHC Strasbourg | A. Besson | ASIC design, testing |
| Oxford University | D. Bortoletto | Powering, integration, testing |
| Zurich University | A. Macchiolo | Testing, DAQ, simulations |

# TPSCo 65nm : spatial resolution




First proposed by W. Snoeys et al.
H. Pernegger et al., 2017 JINST 12 P06008

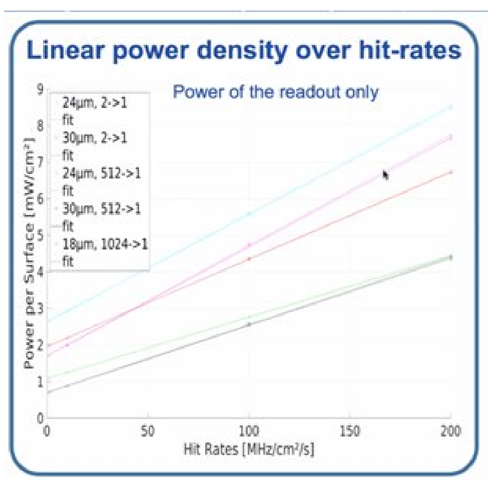
PIXEL2024 :
https://indico.in2p3.fr/event/32425/contributions/142771/

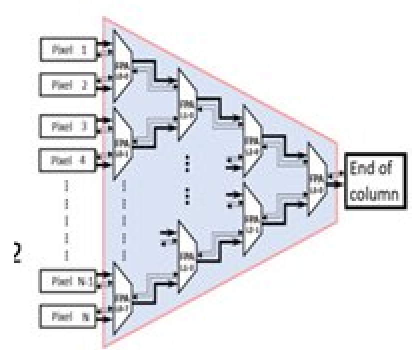
Key message: Spatial resolution ≤ 3 µm reachable if:

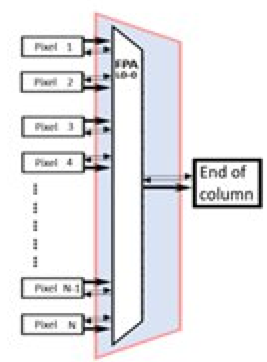
- Pitch below ~ 15 µm (no charge sharing, binary output)
- Pitch below ~ 20-25 µm (charge sharing AND charge encoding on fews bits)

# TPSCo 65nm : Readout architecture

- Small pitch is conflicting with the footprint of the readout architecture
  - Idea: decouple the relationship pitch - resolution with charge sharing AND charge encoding (few bits ADC) Keep seed S/N high enough but improve resolution
- Proposal : Asynchronous (clockless) matrix readout
  - Based on Fixed Priority Arbiters (FPA)
  - Versatile architecture (Power, hit rate)
  - SPARC Prototype to be sumitted in ER2 (2025) (In2p3 and IRFU)




NIMA-A : 10.1016/j.nima.2024.169663

https://indi.to/tWgw2

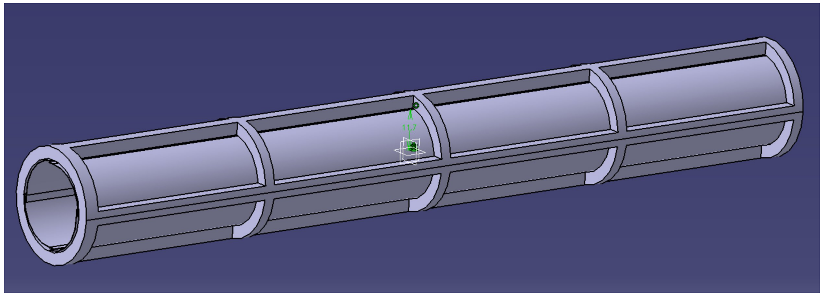
# Mechanics, cooling and integration

- Several challenges ahead.

- We need to master sensor bending (see next slide).

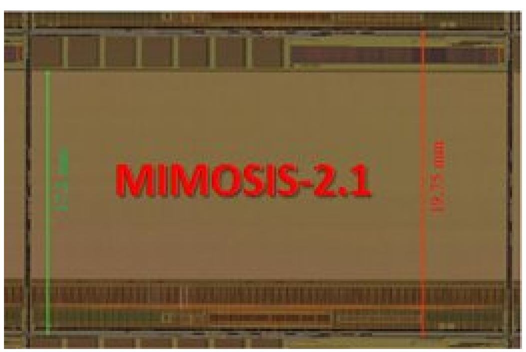
- Design light and precise mechanical supports
  - Determine light material, allowing for a precise geometry,
  - Imagine a robust and “simple” assembly procedure, including integration and cable/fibre routings,
  - Allowing for an efficient (air) cooling, while other options can be explored too.

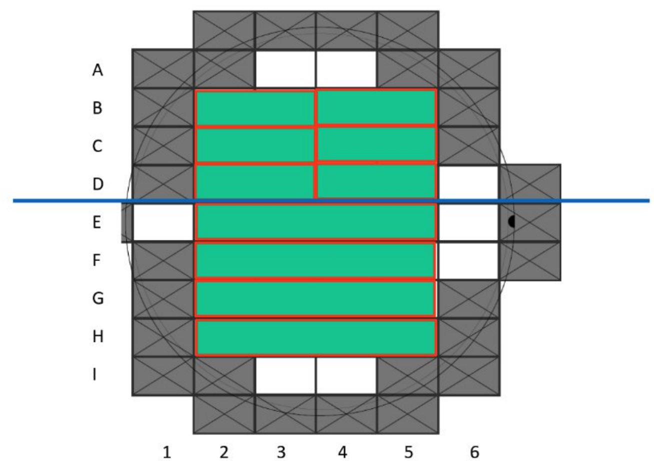
- Short/midterm plan :
  - Start the design effort,
  - Design first geometry to play with,
  - Implement it into a full simulation.



# Curved sensors

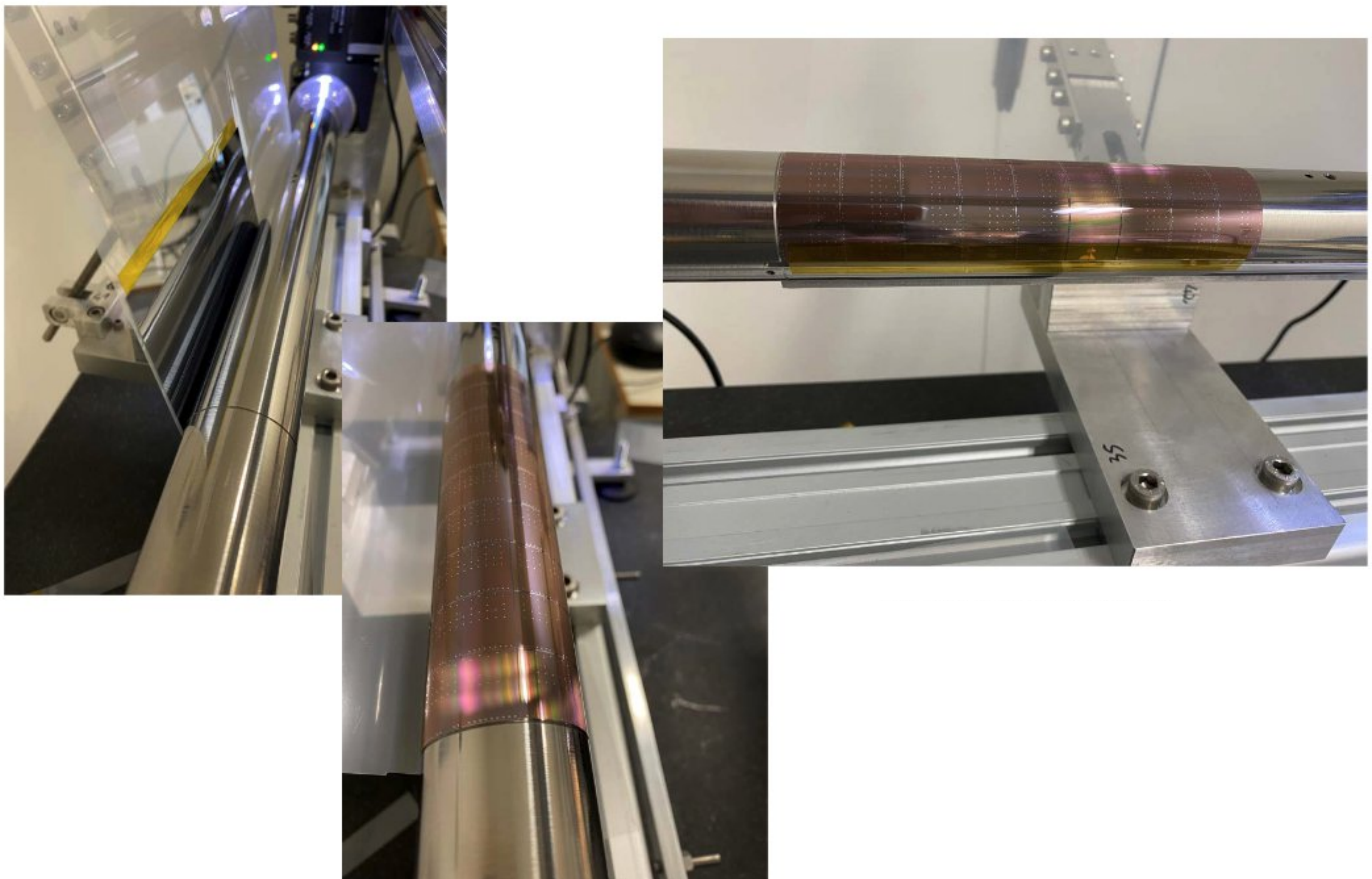
- Working plan :
  - Prepare and install sensor bending bench, with different radius options (12-15mm), and different sensor thickness (30-50 microns).
  - Practice bending with dummy sensors, then real functional on single sensors (Mimosis), perform connectivity and setup DAQ, and tests.
  - Bending of a wafer slice (Mimosis), connectivity and tests,
  - Move toward a larger scale demonstrator of the 1st Layer in a few years from now.
  - Mimosis : large size sensor (6 $cm^2$), with specs close to FCCee needs.



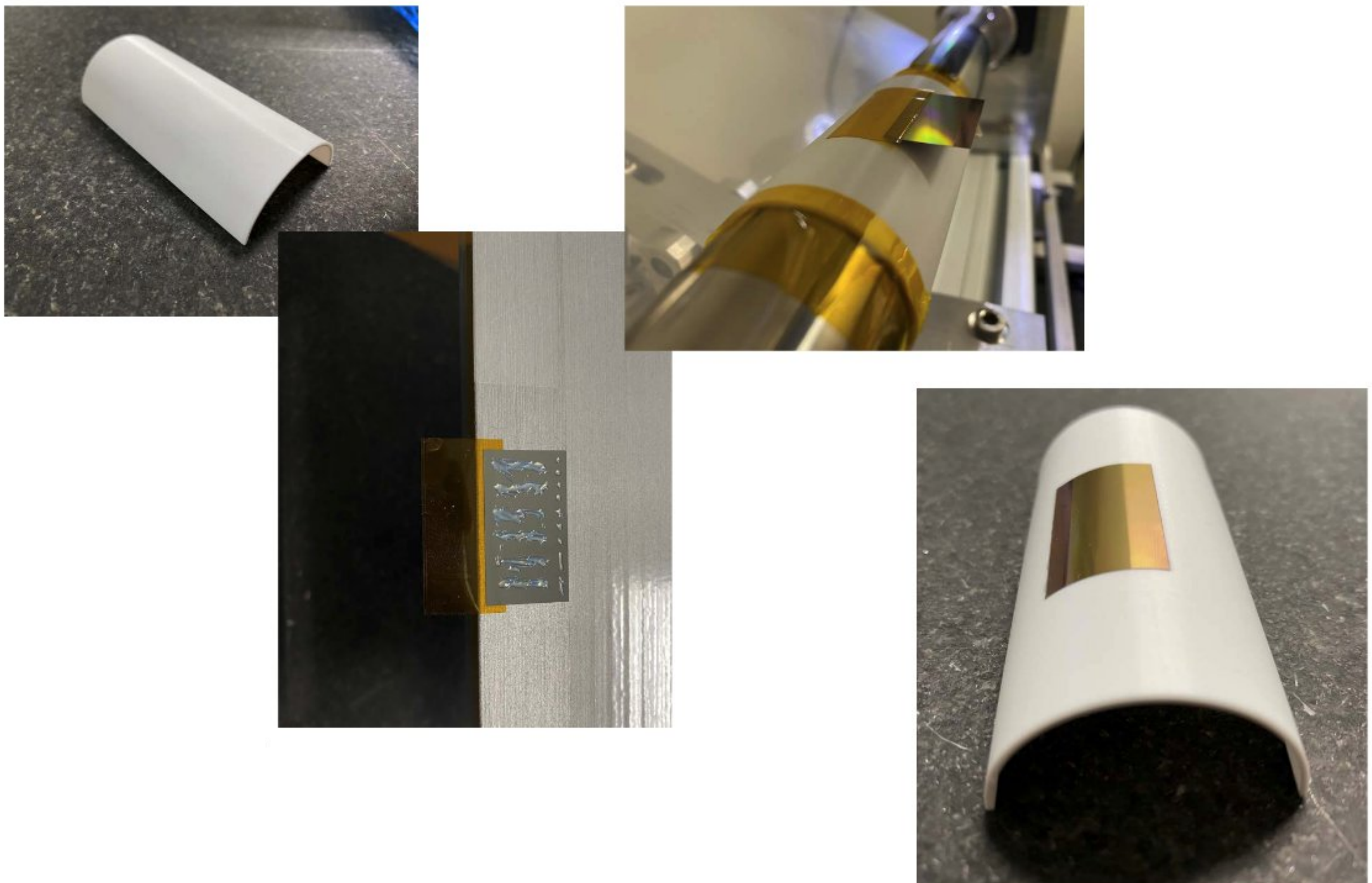
# Curved sensors (2)

Bending bench highly inspired from Alice ITS3.
Bending test of super-Alpide pad, 130x50mm, thickness of 40 microns.
Radius: 18 mm



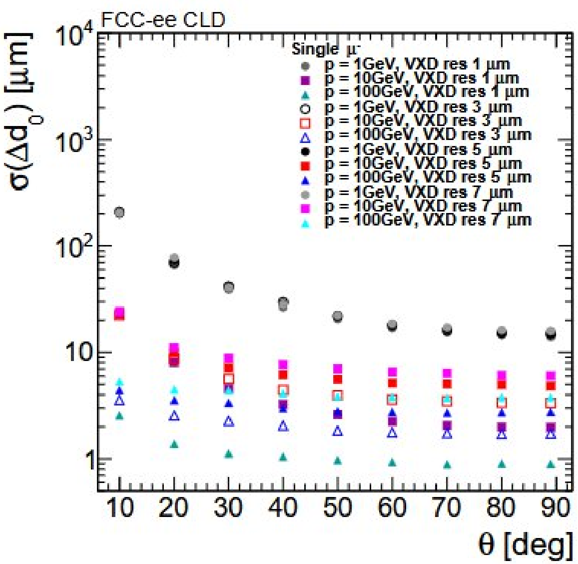
# Curved sensors (3)

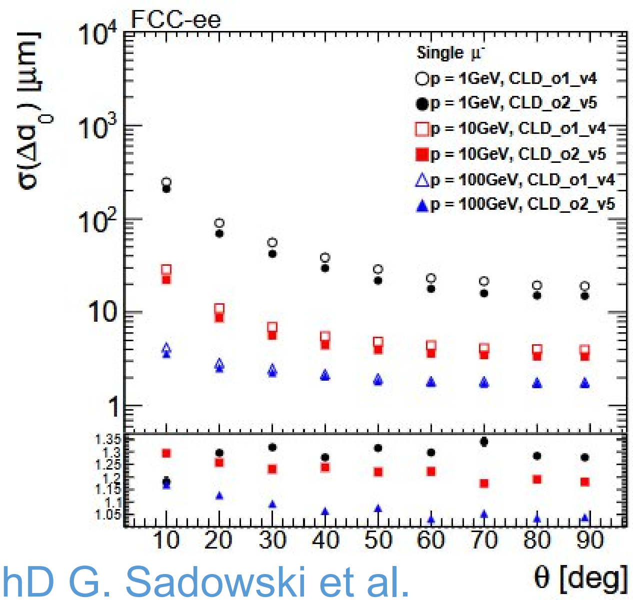
Bending tests of Mimosis 2.1 (31x17mm), thickness of 40-50 microns.
Radius: 18 and 15 mm.
Successful (no breaking)



# Detector simulations

- Preliminary studies where performed, using the CLD full simulation.
- Impact of the sensor design (single point resolution), geometry, and material budget on the track resolutions / impact parameter




PhD G. Sadowski et al.

**CLD_o1_v04** (nominal geometry)

- Beam Pipe **radius**: 15 mm
- Beam Pipe **material**: Beryllium
- Beam Pipe **thickness**: 1.2 mm + 5 μm gold
- **X/X0** = 0.45 %

**CLD_o2_v05**

- Beam Pipe **radius**: 10 mm
- Beam Pipe **material**: AlBeMet 0.35 mm + paraffin 1 mm + AlBeMet 0.35 mm
- Beam Pipe **thickness**: 1.7 mm + 5 μm gold
- **X/X0** = 0.61 % ⇒ **+ 33 % material budget**

- Similar studies (including physics performance) have to be performed after :
  - Implementation of the digitisation,
  - Implementation of the new geometries into the full simulation.

# FCC-SEED : Conclusion and plan

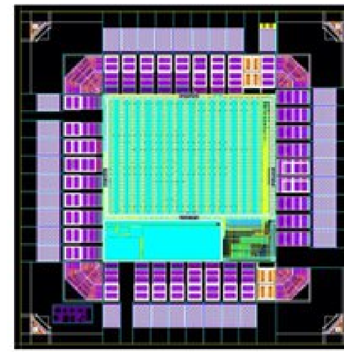
- Starting efforts for the design of a Vertex detector concept for FCCee
  - Based on dedicated maps-sensors R&D <= long standing expertise in French labs,
  - Curved sensors, mechanics and integration <= bending being practiced currently, involvements of micro-technical and mechanical engineers,
  - Include simulation studies <= test impact of design choices on physics performances,
  - Global and coherent approach.

- A detailed program is being constructed, with the scope of preparing a standalone Expression of Interest in preparation with French institutes (open to collaborations).
  - draft of EoI
  - More details in a future public document (available on request)

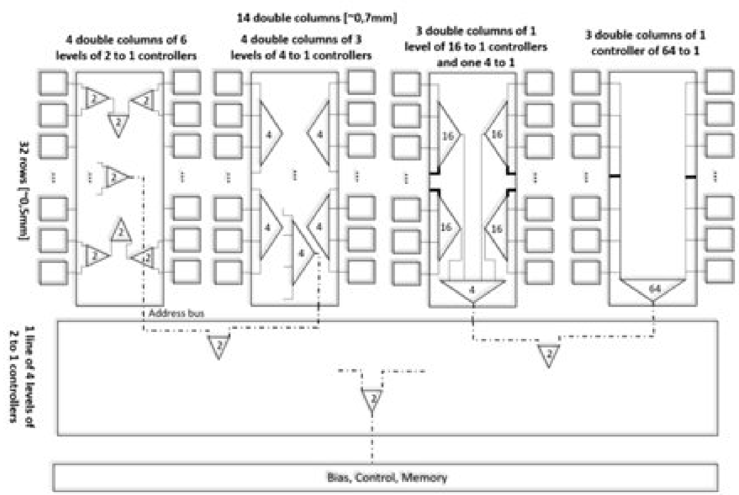
# backup

# SPARC : first prototype with asynchronous readout

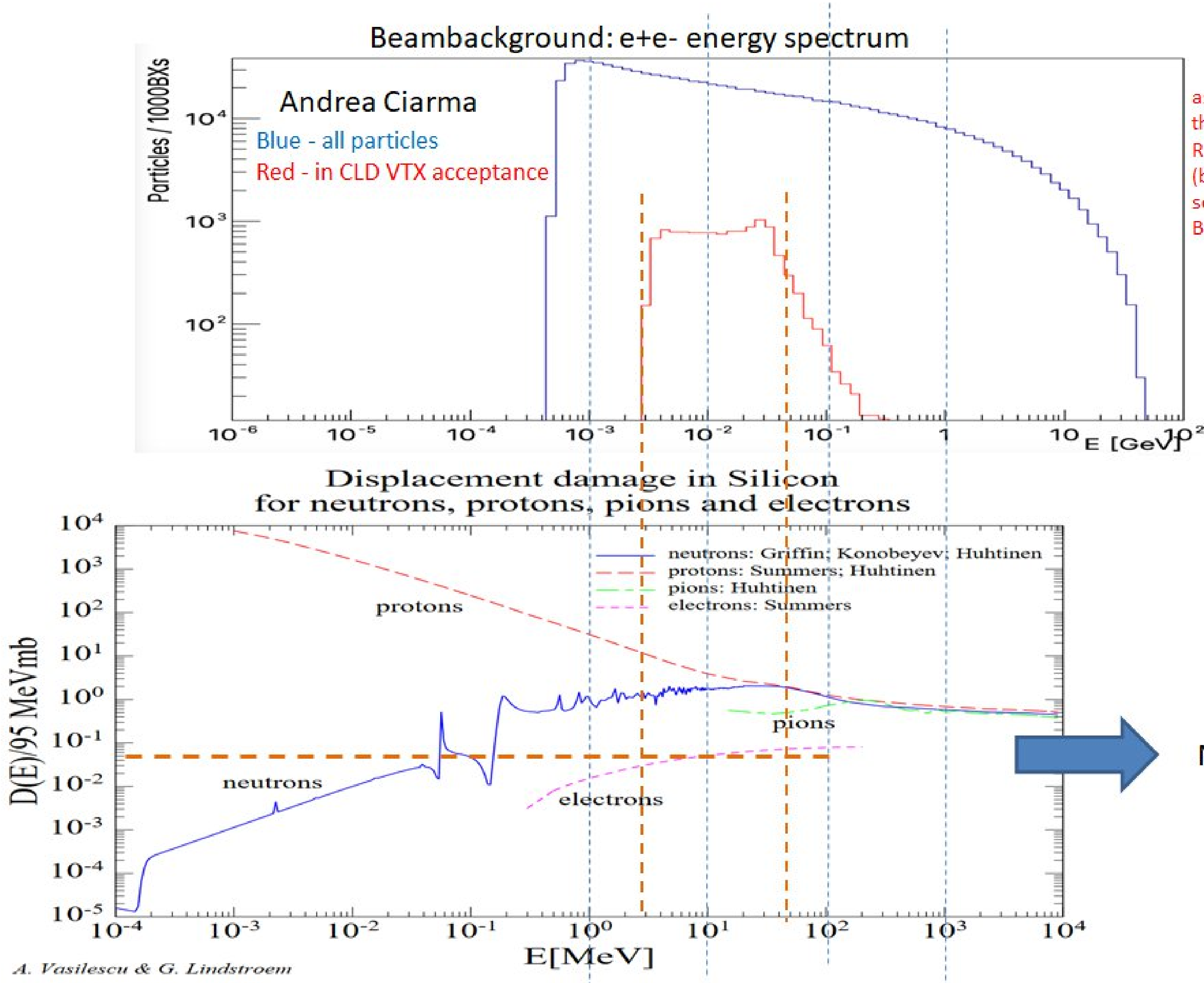
- Pixel pitch: $24 \times 16\ \mu m^2$
- Pixel matrix: $32 \times 28$
- Pixel front-end: DPTS (CERN)
- FPA tree types: 2:1, 4:1, 16:1, 64:1
- Power dissipation: $5\ mW/cm^2$
- Mean readout time: 6.3 ns
- Developed by IPHC and IRFU
- To be submitted early 2025 in ER2
- Test system in preparation for summer 2025



$1.5 \times 1.5\ mm^2$



# Fluence @ FCCee




assumptions:
theta > 100mrad ;
R > 10mm ;
(beampipe radius to account for scattering/secondaries) ;
B = 2T —> pT > 3MeV

NIEL factor ~ 5 x $10^{-2}$