universität freiburg

# Large Area CMOS Silicon Detectors for the FCC

Ulrich Parzefall, University of Freiburg

14 January 2025, 8th FCC Physics Workshop

universität freiburg

# Silicon for the FCC - Setting the Scene

- Silicon sensors are core tracking element in HEP
- At present, vast majority of (large) experiments use (or install) passive silicon in dedicated technology, often from single source
- Mostly Hybrid Technology (sensor and separate FE ASIC)
- Area of silicon is constantly increasing
- Presently running Si trackers provide 3D space points
- “Fast timing” to be used e.g. in Phase-2 LHC upgrades

- FCC poses a number of challenges: position resolution, low mass, radiation doses (for FCC-hh)
- FCC detectors will likely also have silicon-based trackers! If we would need to start building in 5 or 10 years, this would be monolithic CMOS… possibly like ALICE ITS3
- Most CMOS projects are pixels – also strip examples
- My FCC Requirements: ~**3 µm** single-point resolution, ~**5 ns** time resolution, average power consumption below **~50 mW/cm2, low mass (thin, low inactive area)**
- Small highly biased CMOS selection presented today

# Silicon for the FCC - Setting the Scene

- Silicon sensors are core tracking element for in HEP
- At present, vast majority of (large) experiments use (or install) passive silicon in dedicated technology, often from single source
- Mostly Hybrid Technology (sensor and separate FE ASIC)
- Area of silicon is constantly increasing
- Presently running Si trackers provide 3D space points.
- “Fast timing” to be used e.g. in Phase-2 LHC upgrades

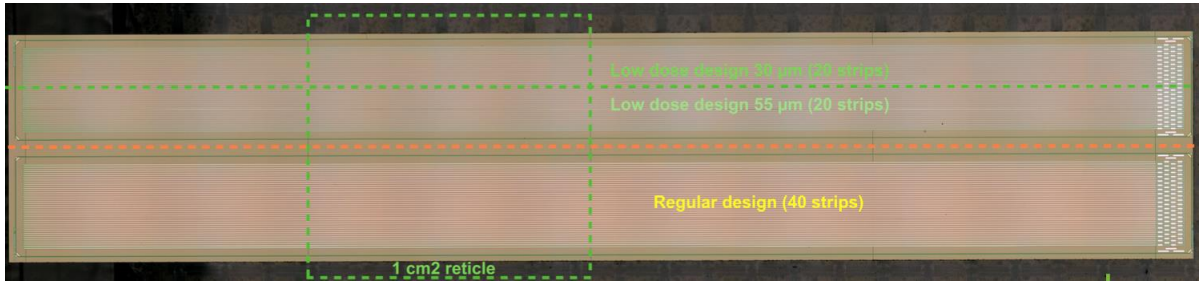
- FCC poses a number of challenges: position resolution, low mass, radiation doses (for FCC-hh)
- FCC detectors will likely also have silicon-based trackers! If we would need to start building in 5 or 10 years, this would be monolithic CMOS… possibly like ALICE ITS3
- Most CMOS projects are pixels – also strip examples
- My FCC Requirements: ~**3 µm** single-point resolution, ~**5 ns** time resolution, average power consumption below **~50 mW/cm2, low mass (thin, low inactive area)**
- Small highly biased CMOS selection presented today

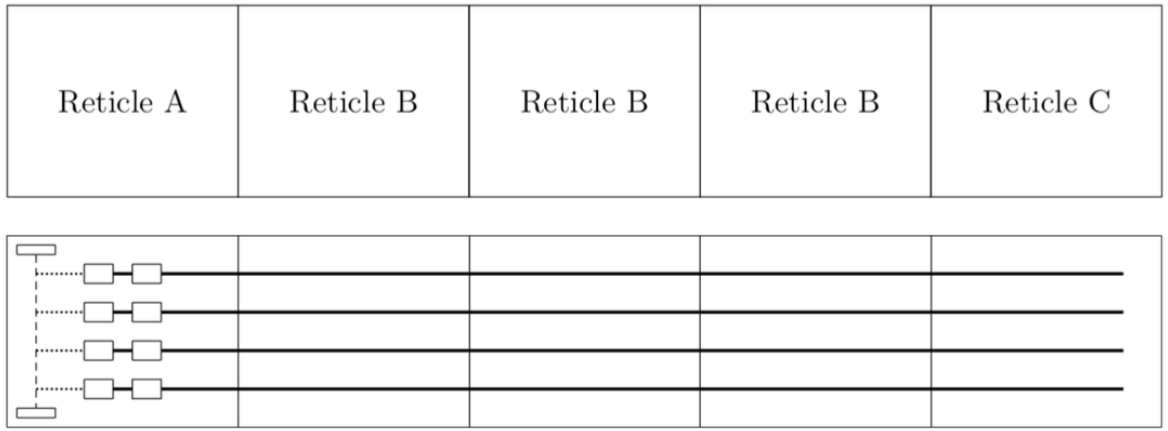
| WG1 research goals <2027 | |
|---|---|
| | **Description** |
| RG1 | Spatial resolution: ≤3 µm position resolution |
| RG2 | Timing resolution: towards 20 ps timing precision |
| RG3 | Readout architectures: towards 100 MHz/cm$^2$, 1 GHz/cm$^2$ with 3D stacked monolithic sensors, and on-chip reconfigurability |
| RG4 | Radiation tolerance: towards $10^{16}$ $n_{eq}$/cm$^2$ NIEL and 500 MRad |
| RG5 | Low-cost large-area CMOS sensors |

# Example: Passive CMOS Strips

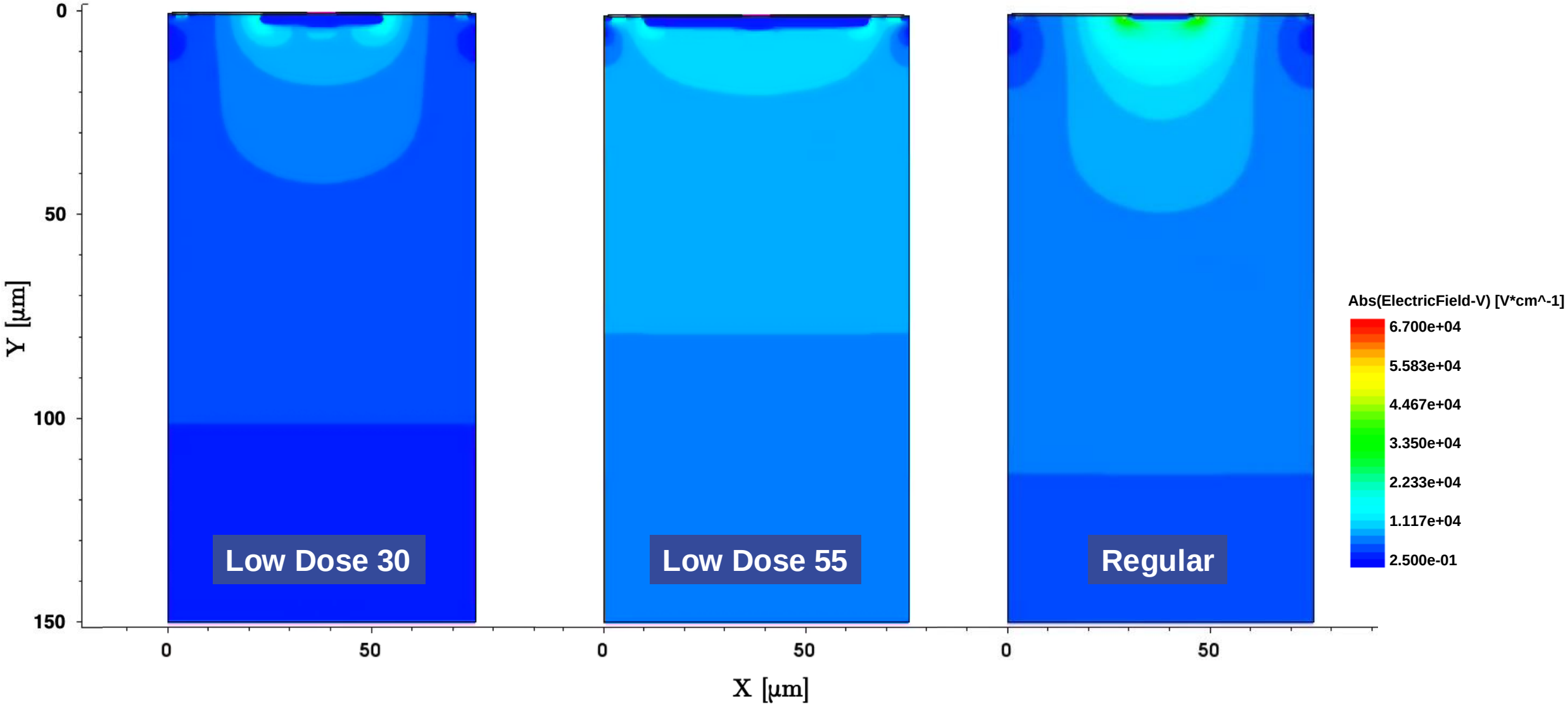
- **Sensors: 150nm LFoundry, 150 µm thick, passive** (Bonn, TU Dortmund, DESY, Freiburg)
- **Two lengths of strips: 2.1 and 4.1 cm**
  - **1 cm$^2$ reticle used → stitching needed (max 5).**
- **Three different designs**
  - **Regular** – similar to the ATLAS ITk strip design
  - **Low dose 30 & 55** – low dose implant and NIM capacitor

  **Sensors simulated, studied in lab and test beam measurements**



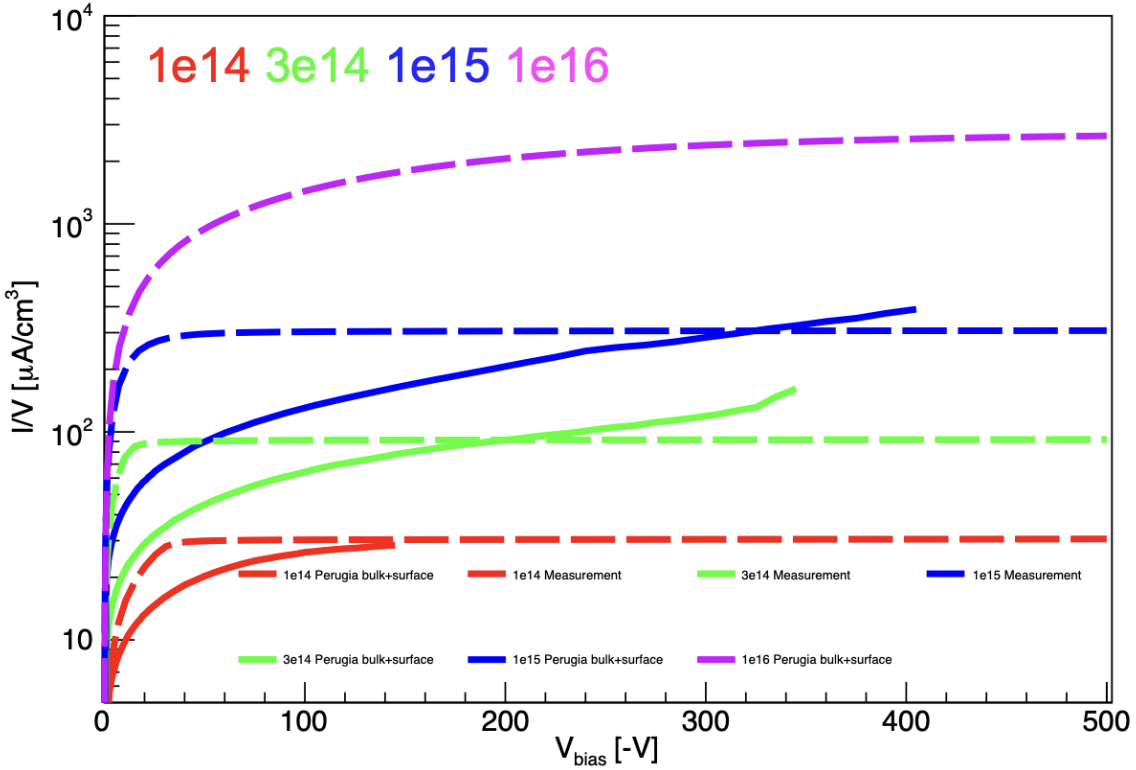



# **Passive CMOS Strips:** Electric Field simulation at 100 V

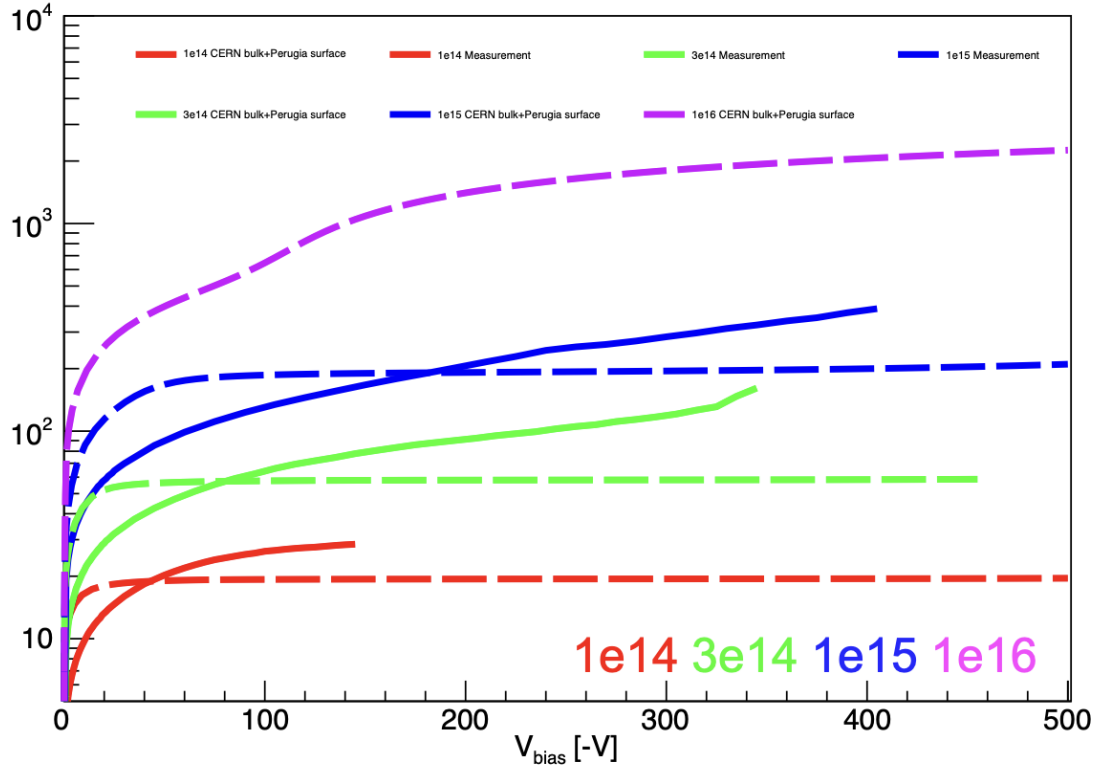


# Passive CMOS Strips:
## Leakage Current Post-Irradiation: Measured and Simulated

**Perugia Bulk+Surface Model**




**CERN Bulk+Perguia Surface Model**

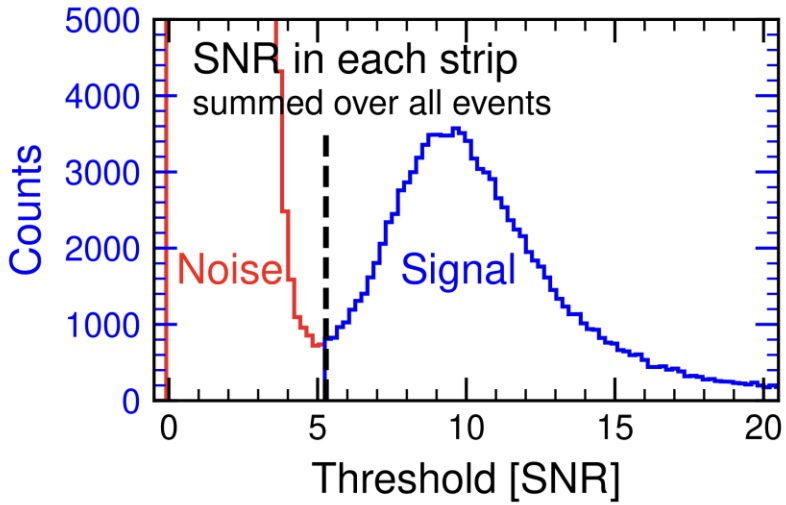



Dashed line: simulation
Solid line: measurement

Proton and neutron irradiated,
all fluences NIEL, T = -30 °C

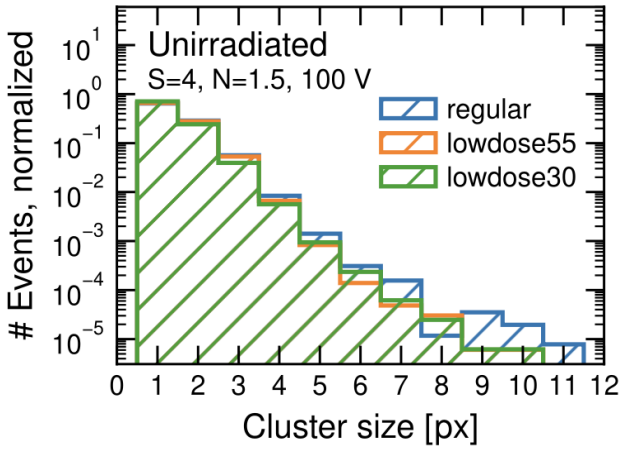
# **Passive CMOS Strips:** Test Beam Measurements

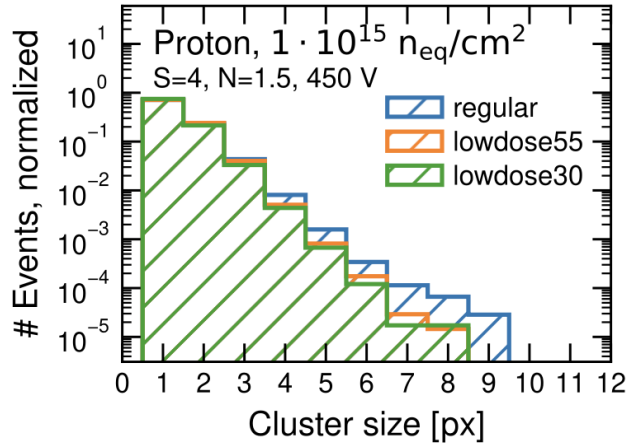
- Measured at DESY-II test beam facility
- Telescope consists of 6 ALPIDE Pixel sensors
- Device Under Test (DUT) read out with ALiBaVA system (analogue, Beetle ASIC (LHCb))
- Several DUTs : from unirradiated to proton and neutron doses up to 3x$10^{15}$ $n_{eq}/cm^2$ (NIEL)

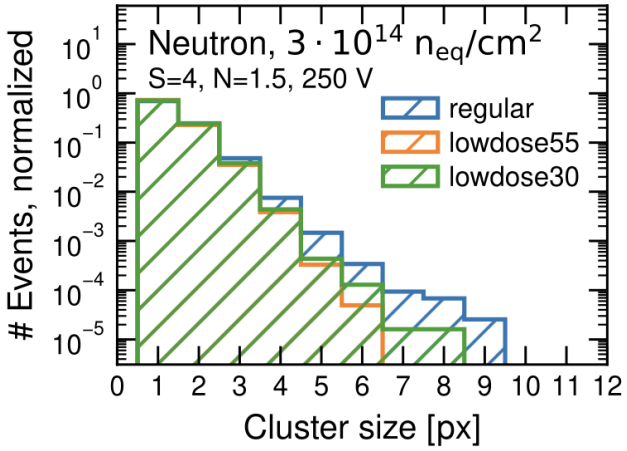


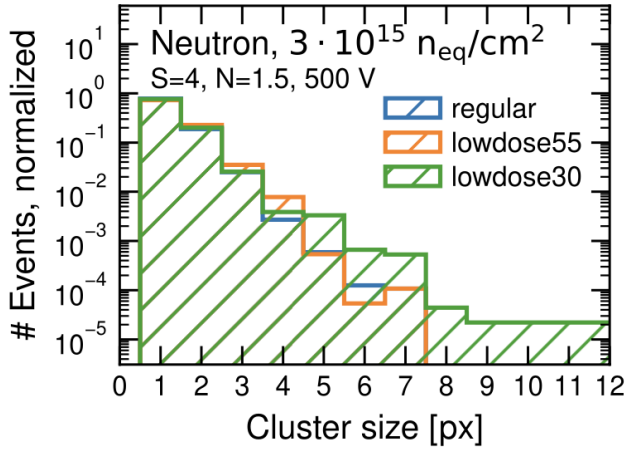

Dashed line: expected binary resolution

- Calculate SNR (Signal to noise ratio) in each strip
- Identify real hits and create clusters of hit strips by applying a cut in SNR (Seed or Neighbour cut)
- Measure cluster size



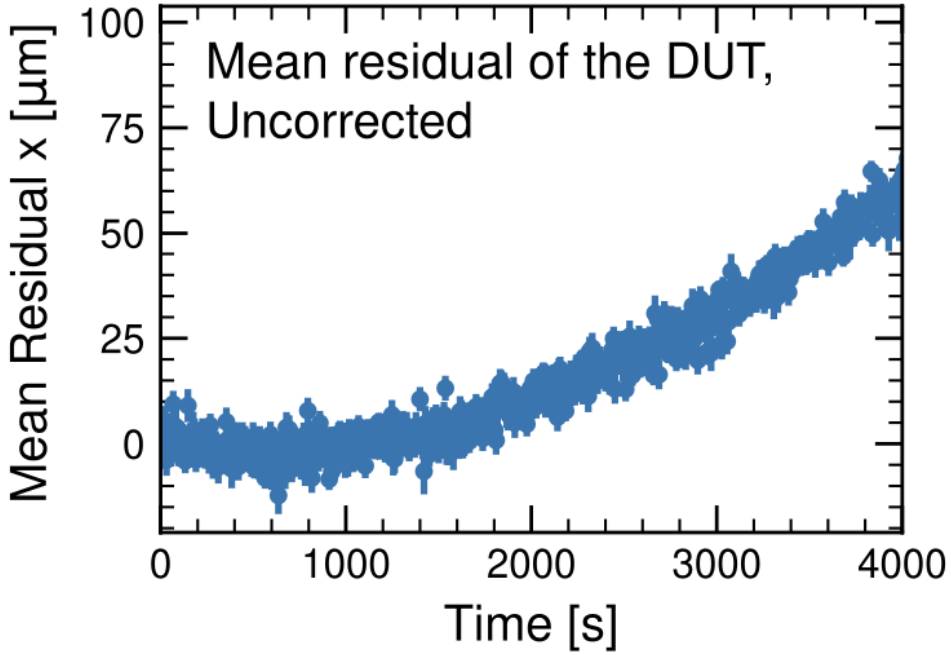



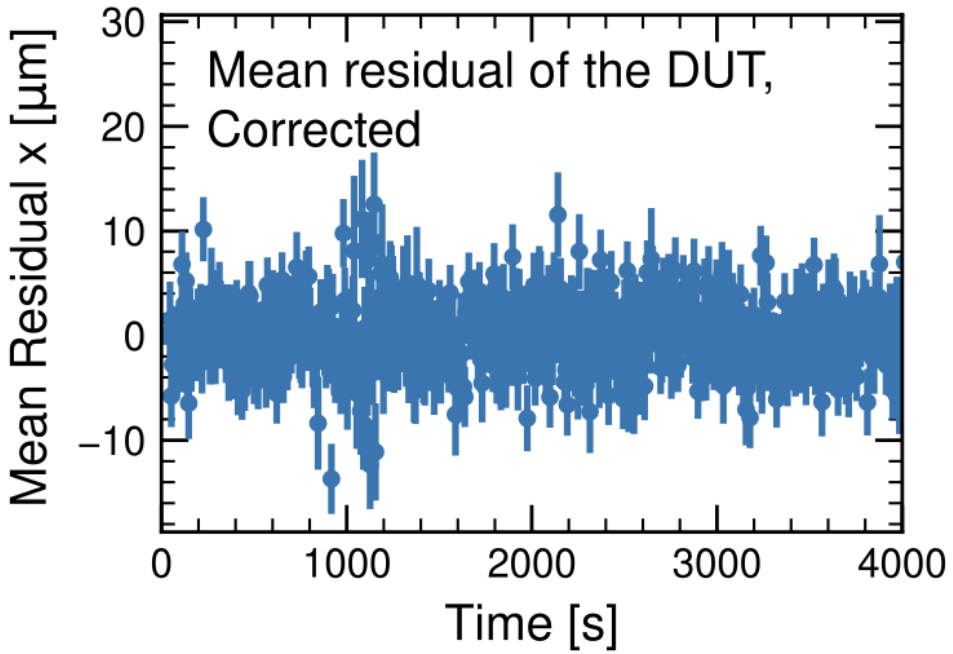



# **Passive CMOS Strips:** Resolution

- Residual: Distance between cluster position on DUT and reconstructed track intercept at DUT
- DUT resolution obtained by subtracting known telescope resolution
- Initially, resolution was time-dependent, requiring time-dependent alignment and correction

- Effect is caused by details of cooling system….
- E.g. ATLAS IBL also experienced time-dependent position drifts and needs time-dependent alignment….

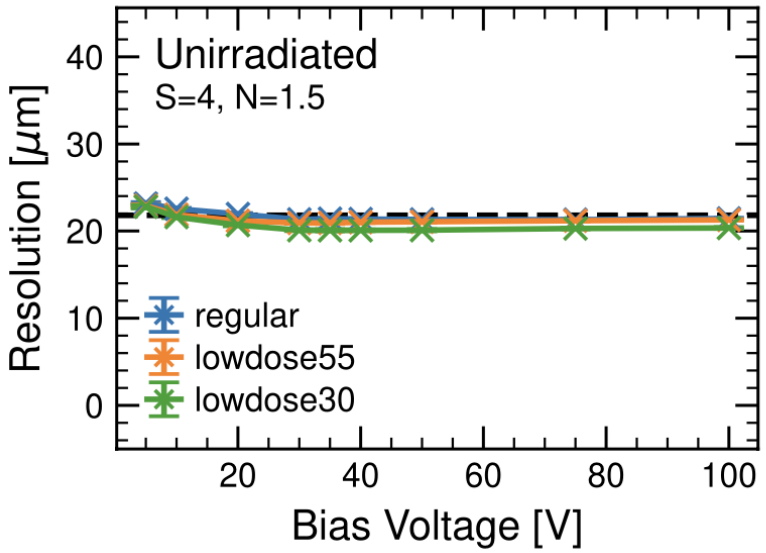


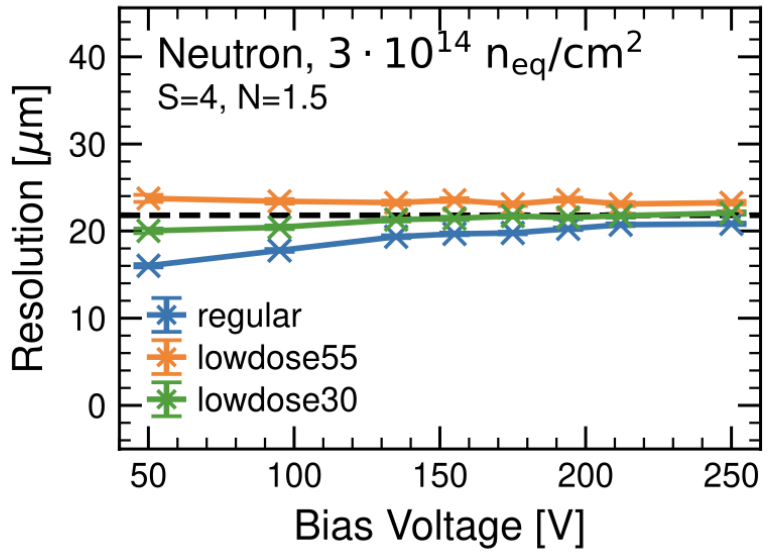



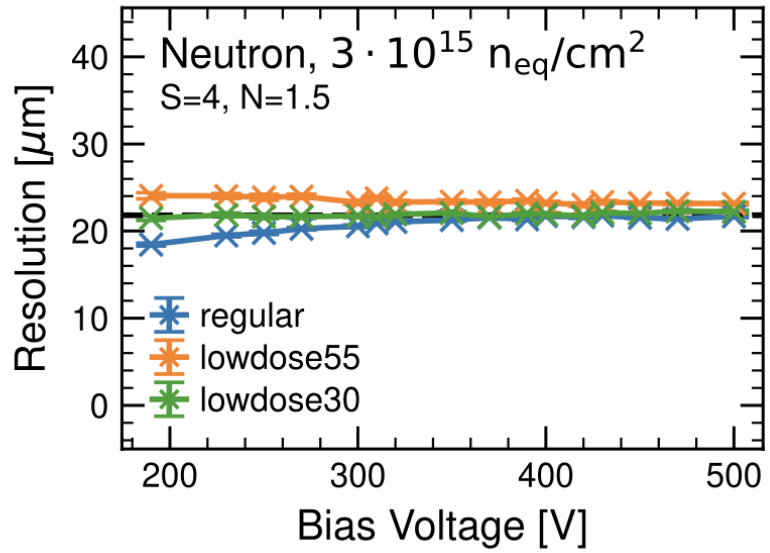
# **Passive CMOS Strips:** Resolution

- Expected binary resolution is reached
- Resolution remains constant up to 3x10$^{15}$ $n_{eq}$/cm$^2$
- Resolution improves slightly with voltage for unirradiated sensor, same resolution for all 3 designs
- Irradiated sensors show different resolutions for the designs and a slighlty degrading resolution with voltage

- Resolution reaches constant value around full depletion (efficiency plots give similar message)
- Resolution of LD30 and Regular design comparable, LD55 worse



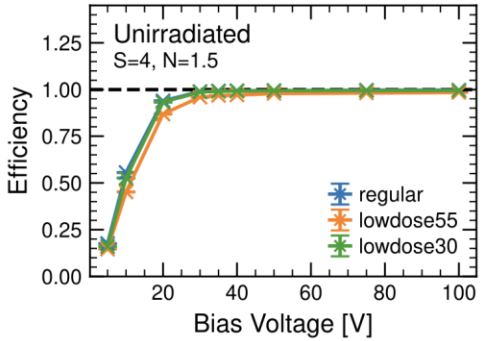



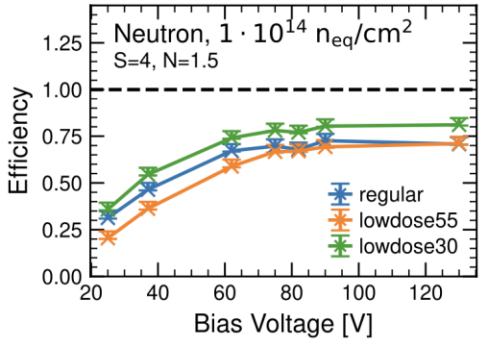

Dashed line: expected binary resolution

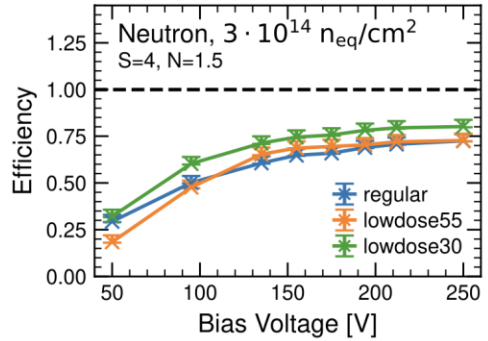
# Passive CMOS Strips: Efficiency

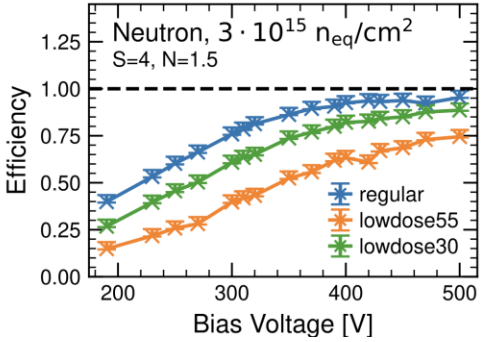
- Efficiency measured by search window around telescope track, extrapolated to DUT
- Efficiency increases with voltage, as depletion progresses trough the sensor

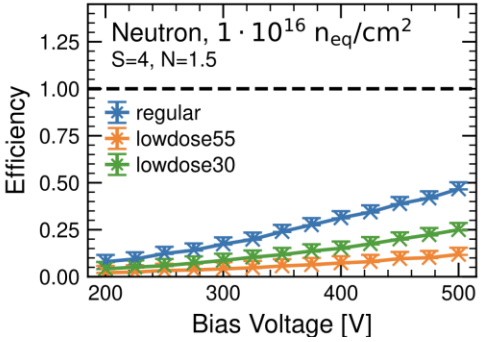
- Irradiated sensors have reduced efficiency with increasing dose (need higher bias to become efficient)
- Regular design largely performs best
- Lowdose55 design disfavoured



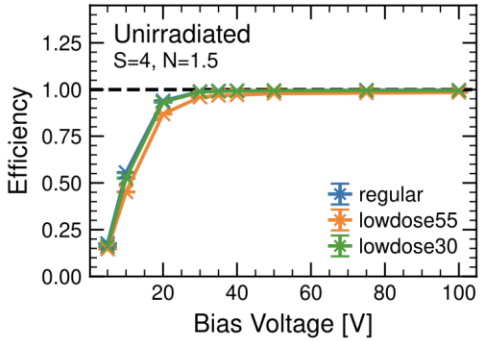



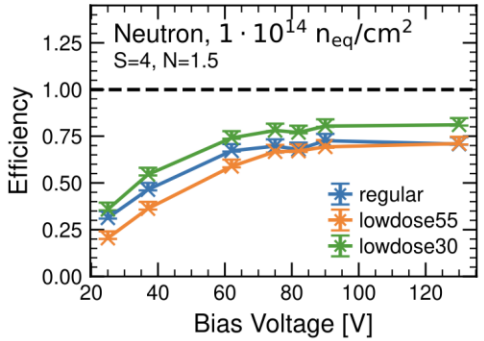



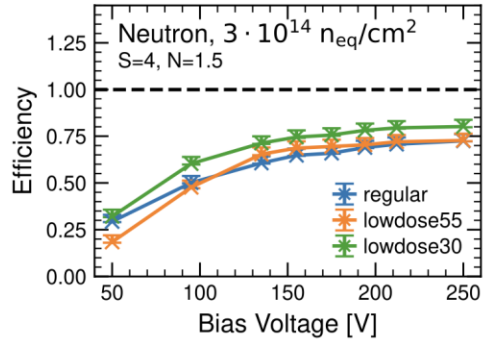
# Passive CMOS Strips: Efficiency

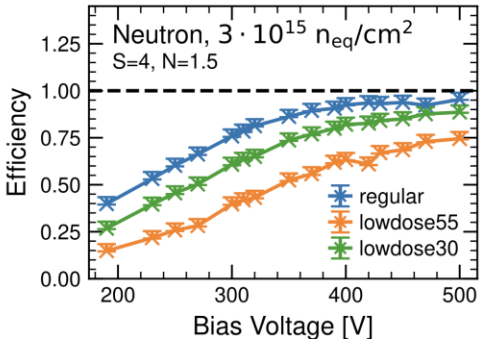
- Efficiency measured by search window around telescope track, extrapolated to DUT
- Efficiency increases with voltage, as depletion progresses trough the sensor

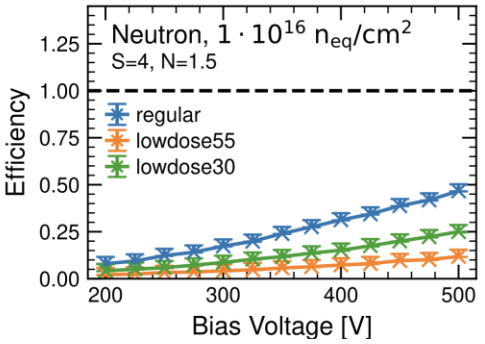
- Irradiated sensors have reduced efficiency with increasing dose (need higher bias to become efficient)
- Regular design largely performs best
- Lowdose55 design disfavoured



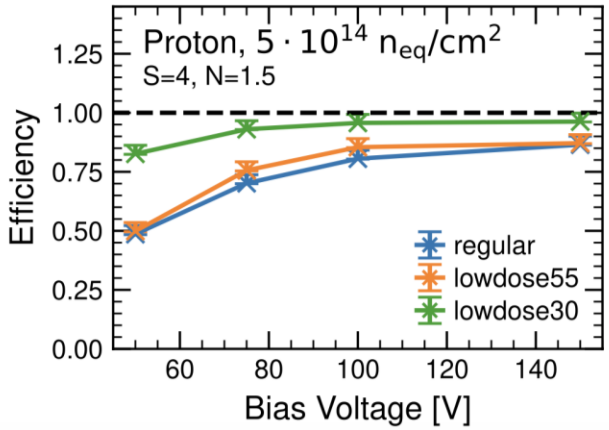



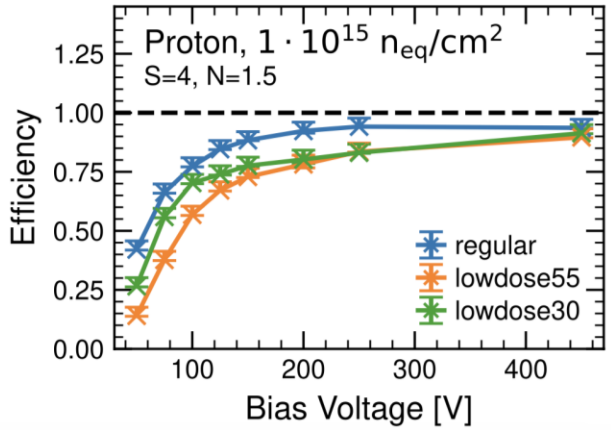




- Neutron and Proton irradiations have somewhat different effects on designs in terms of efficiency
- Several possible explanations, but not yet fully understood

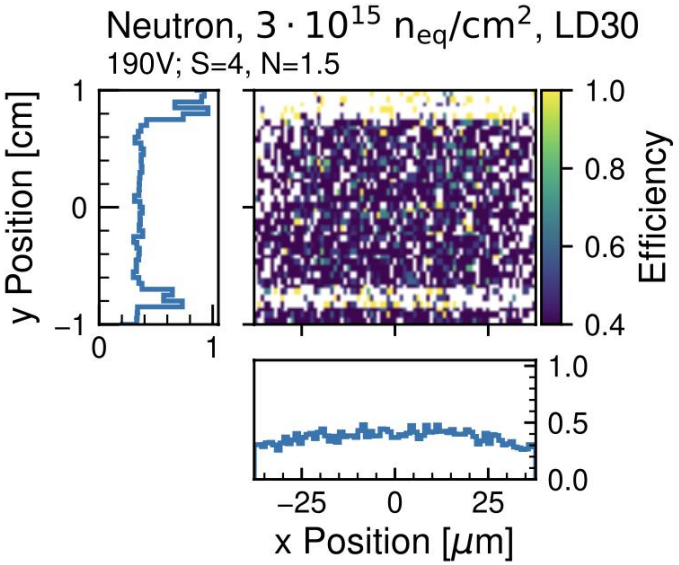


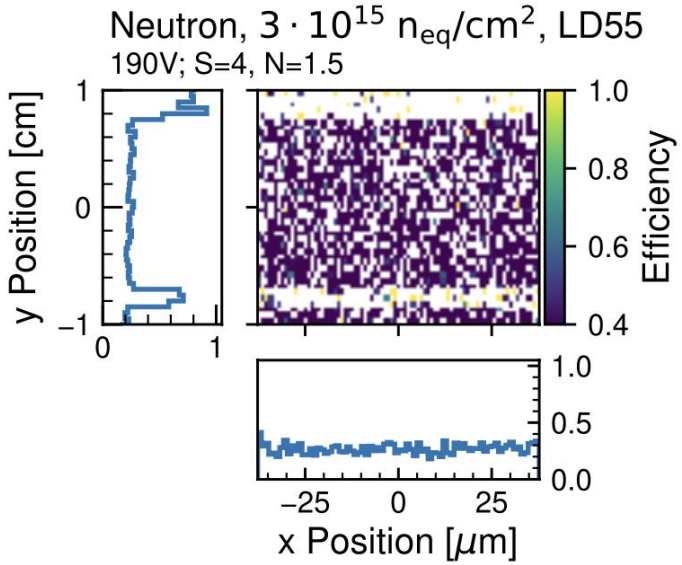



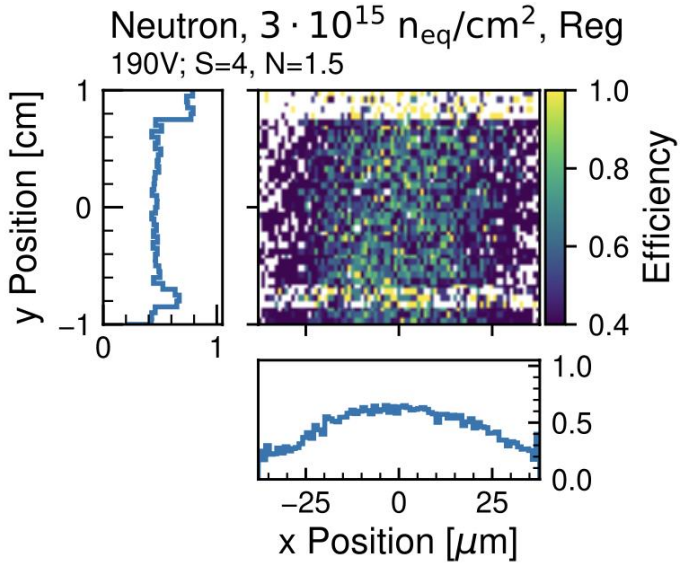
# **Passive CMOS Strips:** Efficiency Maps (“In-Strip Efficiency”)

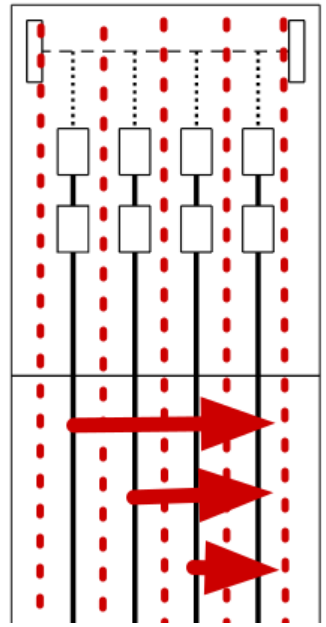
- In-Strip plots: folding all strips onto a single one (unit cell) to increase statistics (see picture to right)
- Plots show 2D effciency map of unit cell, and projections parallel (x) & orthogonal (y) to strip direction
- Example: sensors irradiated to $3x10^{15}$ $n_{eq}/cm^2$ (all 3 designs)

- Following slides will be stepping up bias from where hits are seen to max bias voltage



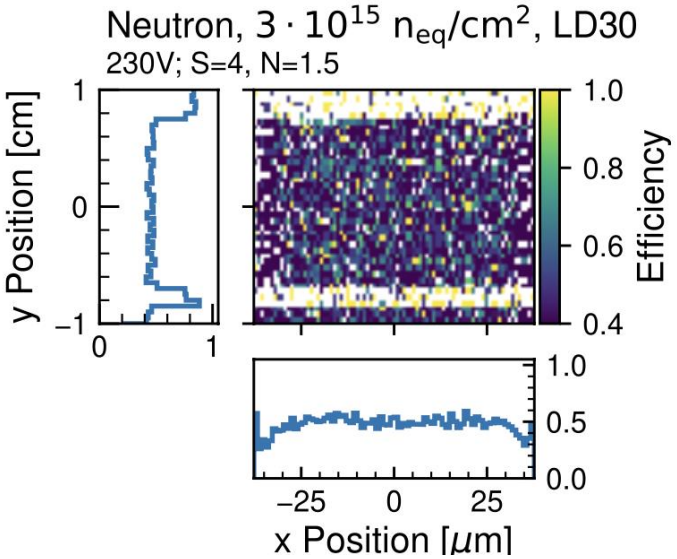



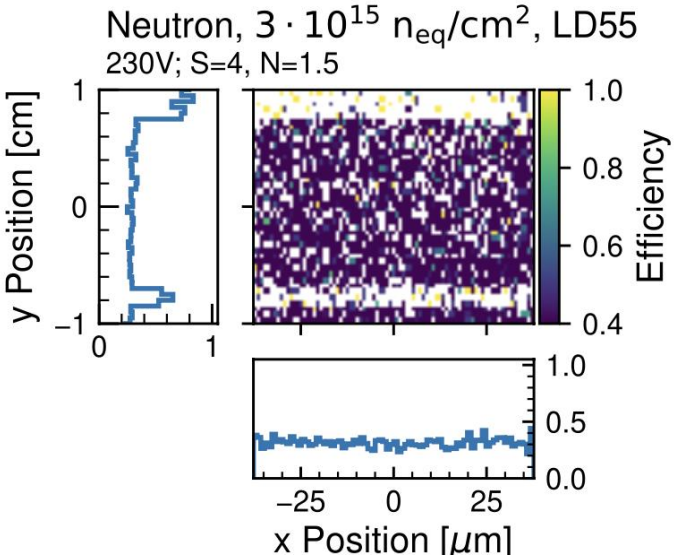



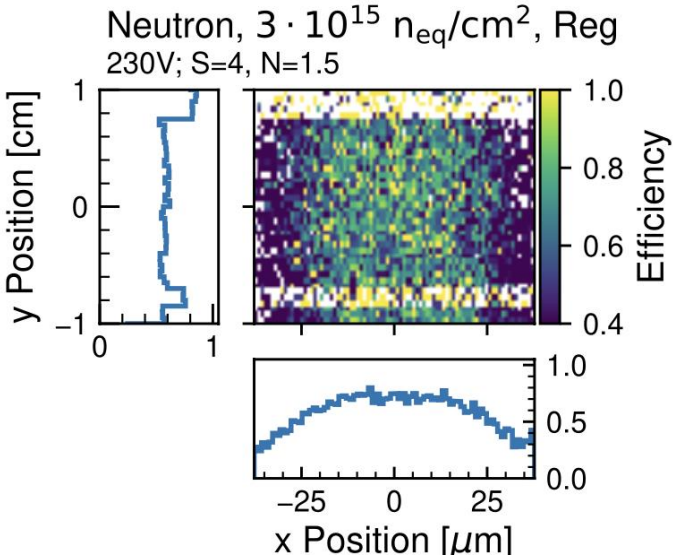
Folding onto unit cell

# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

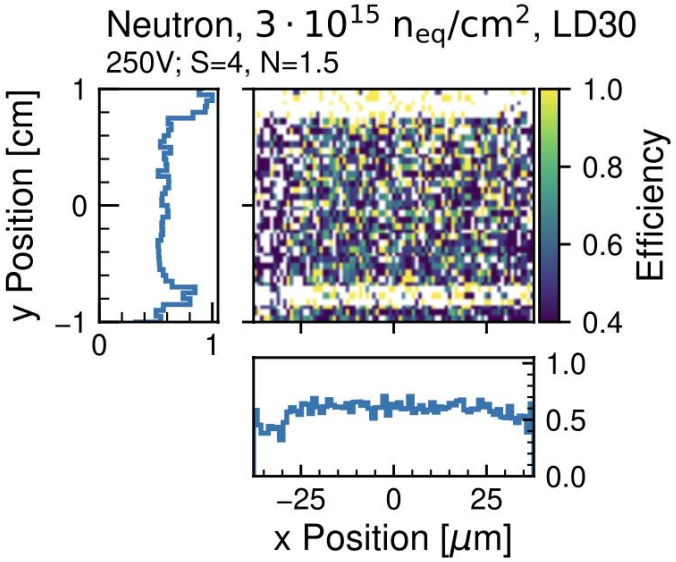


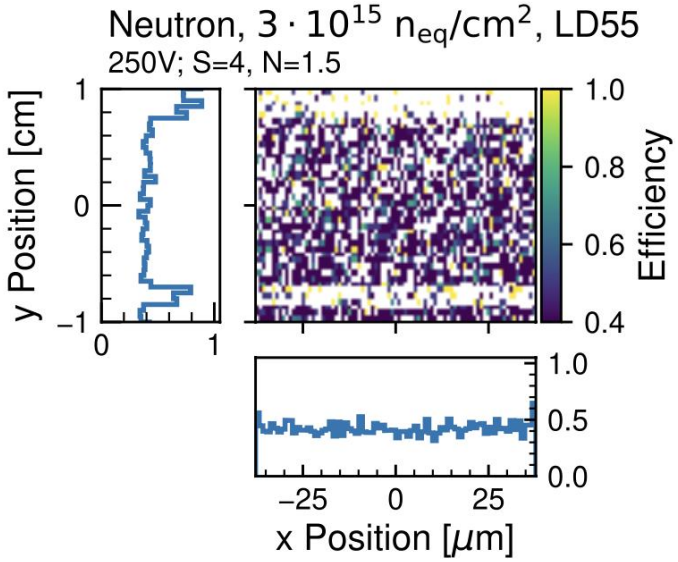



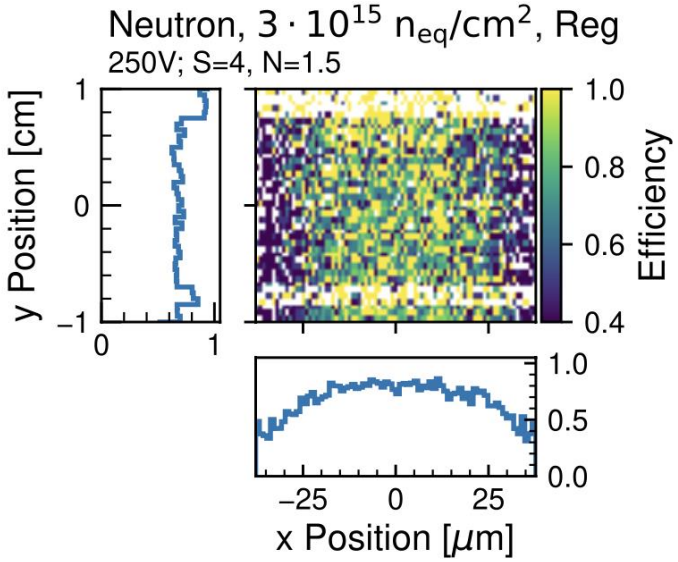



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

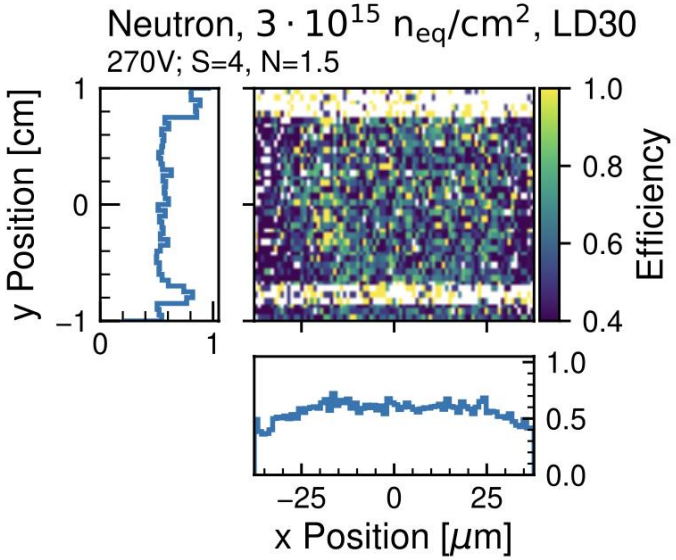


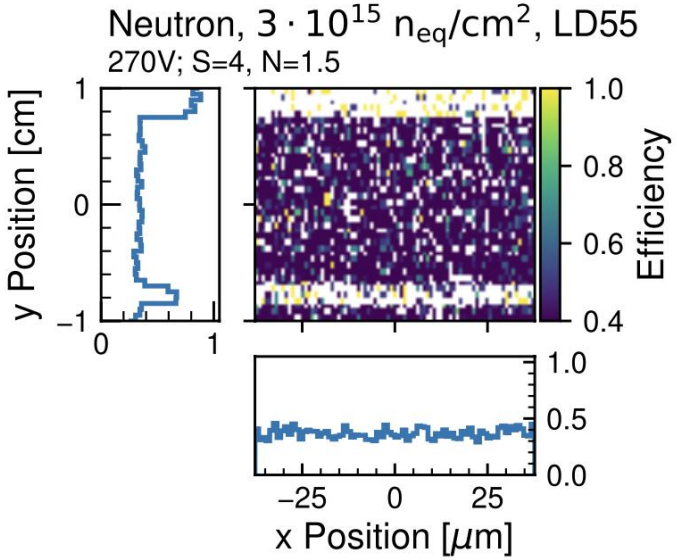



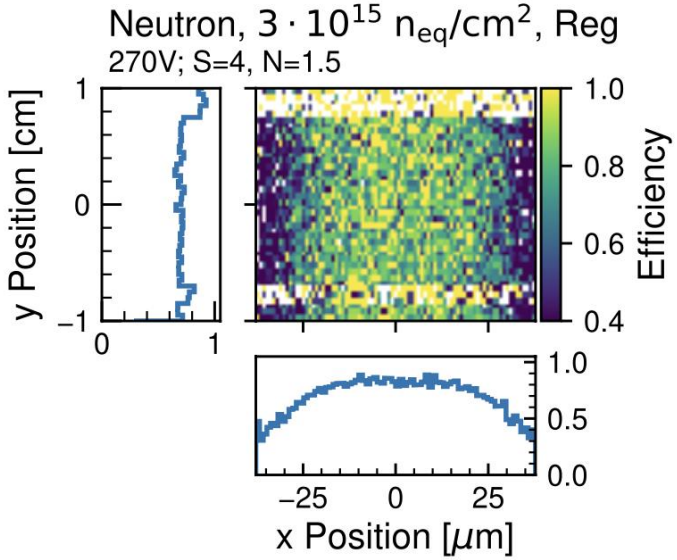



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

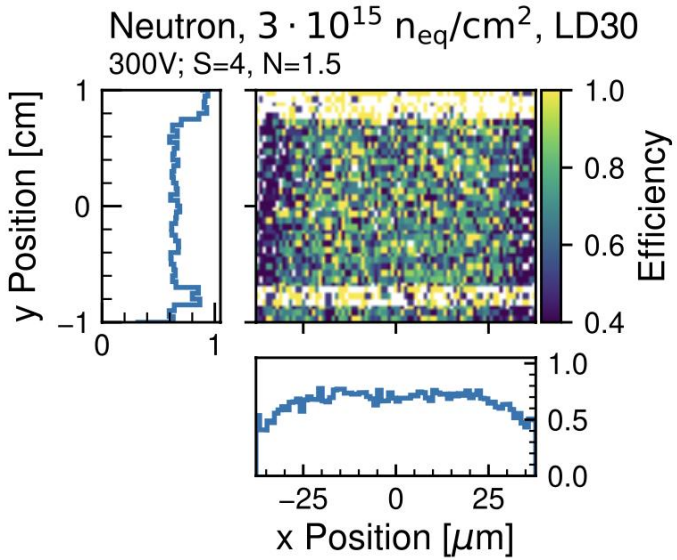


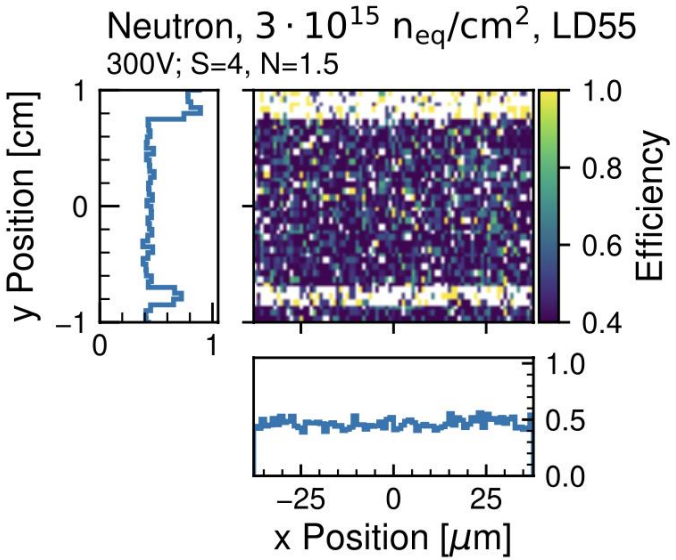



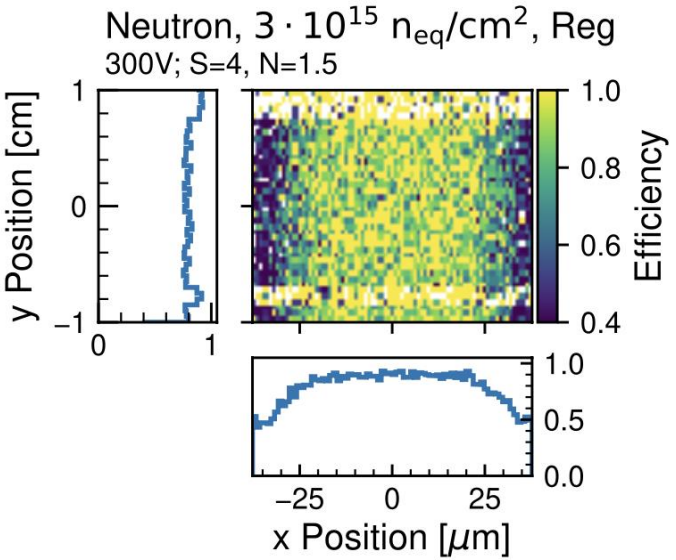



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

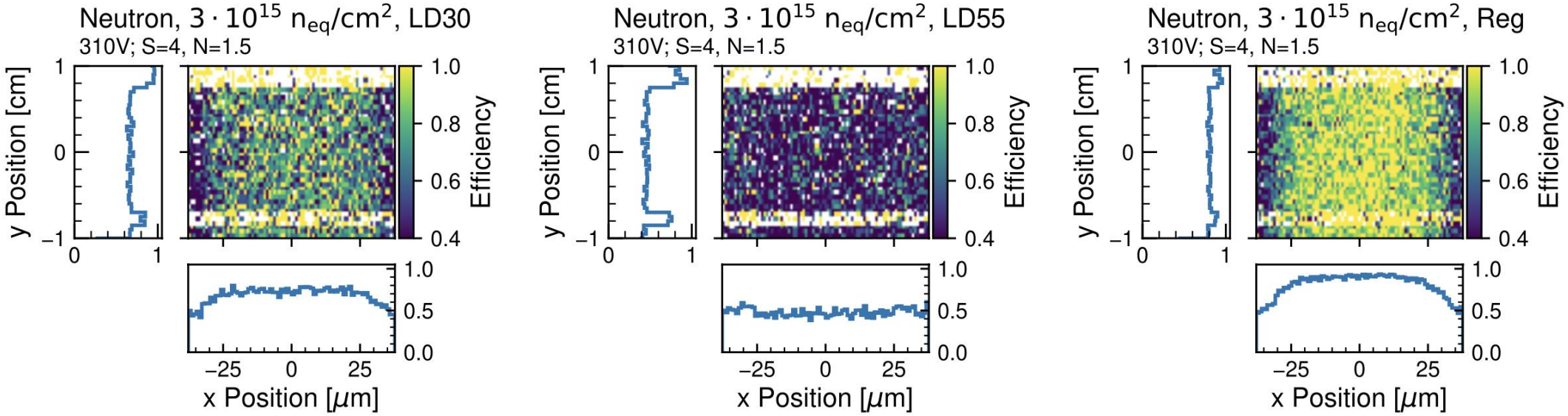


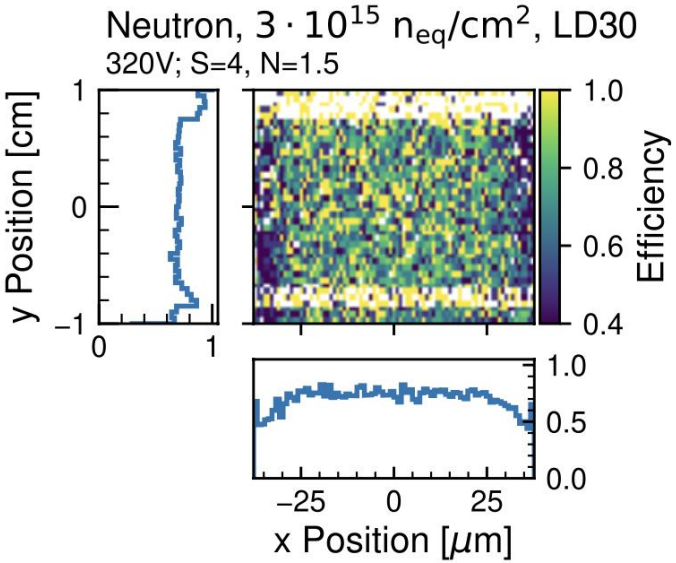
# **Passive CMOS Strips:** Efficiency Maps

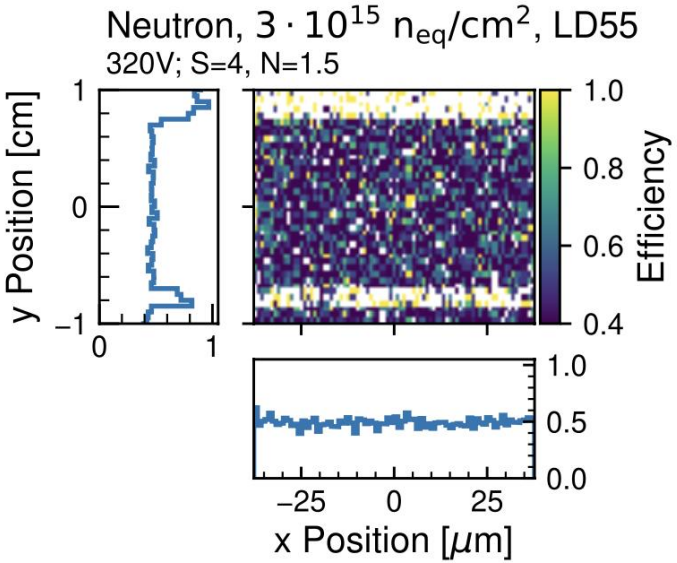
- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

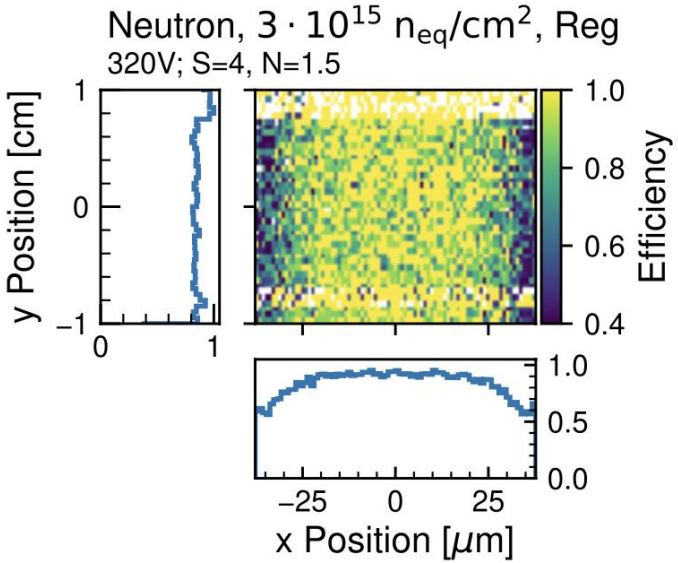


# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

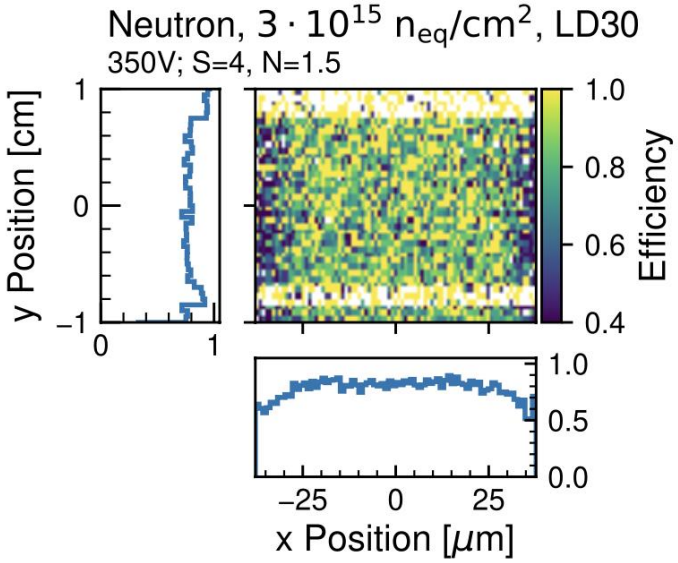


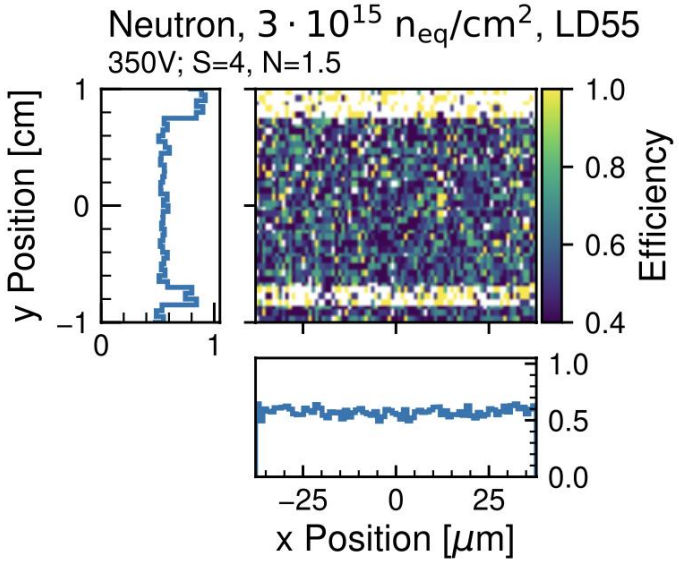



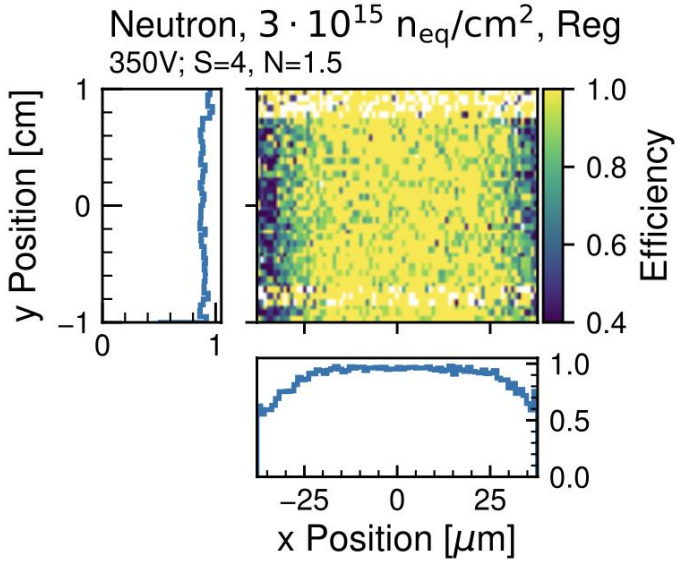



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

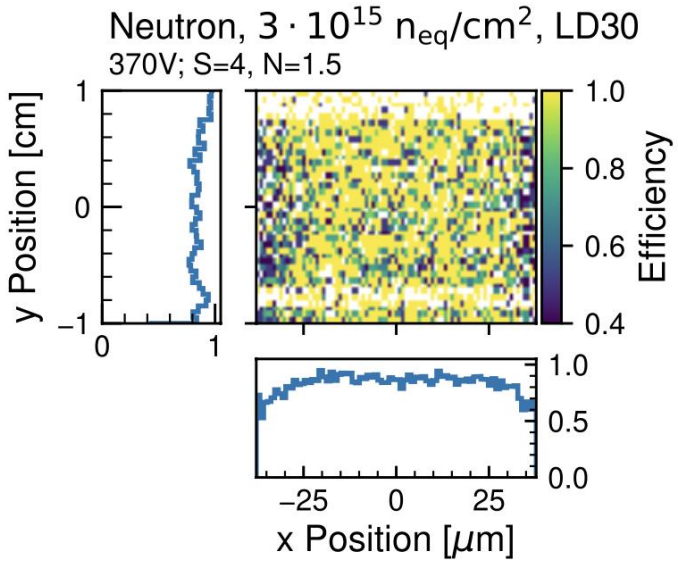


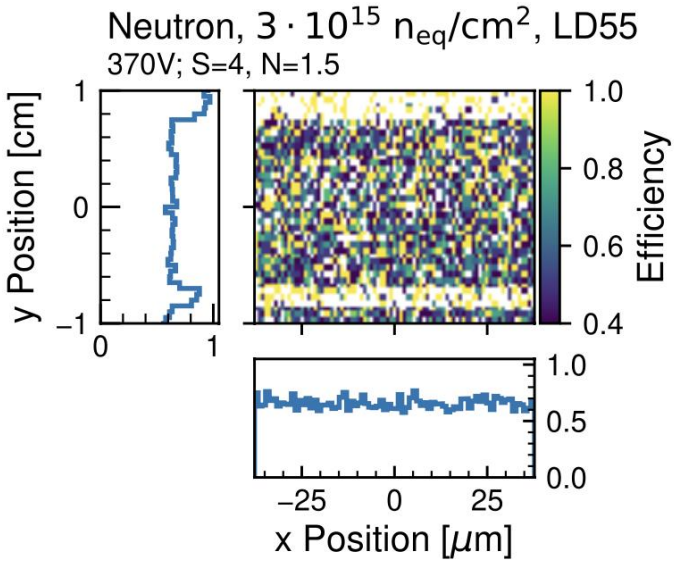



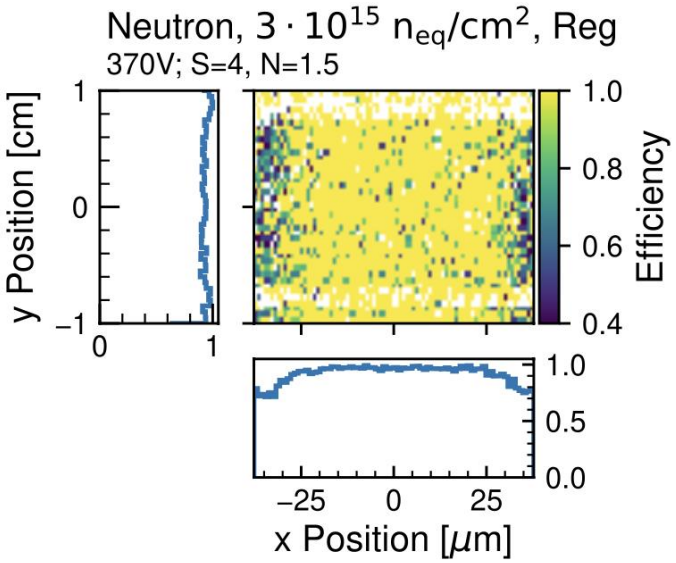



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

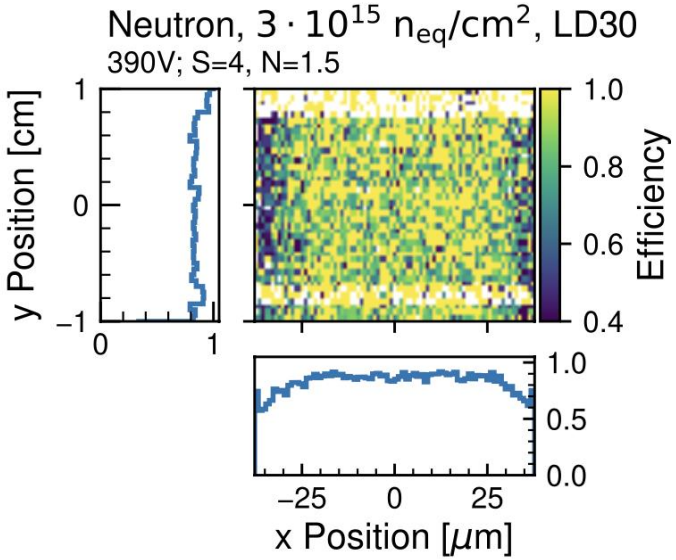


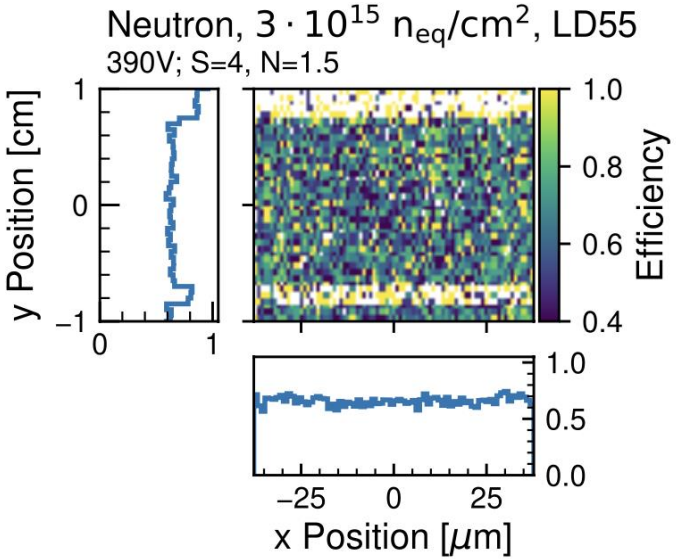



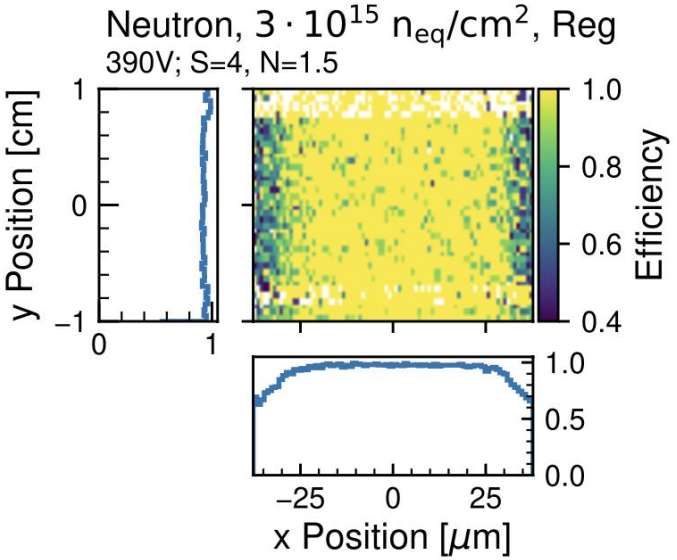



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

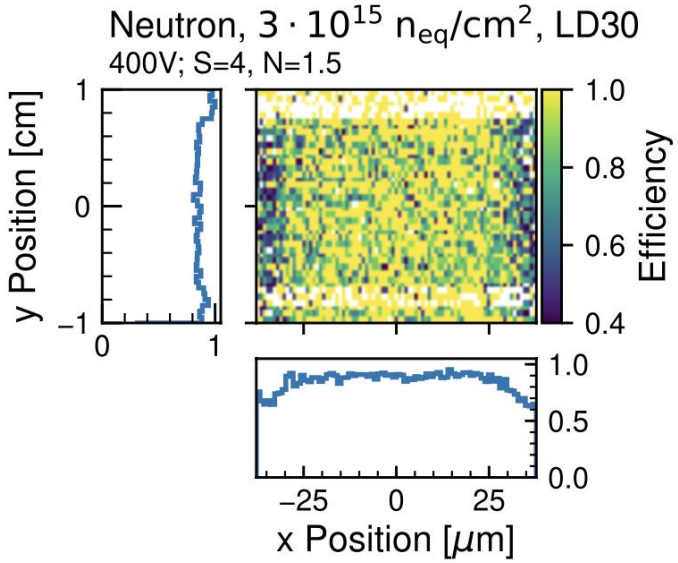


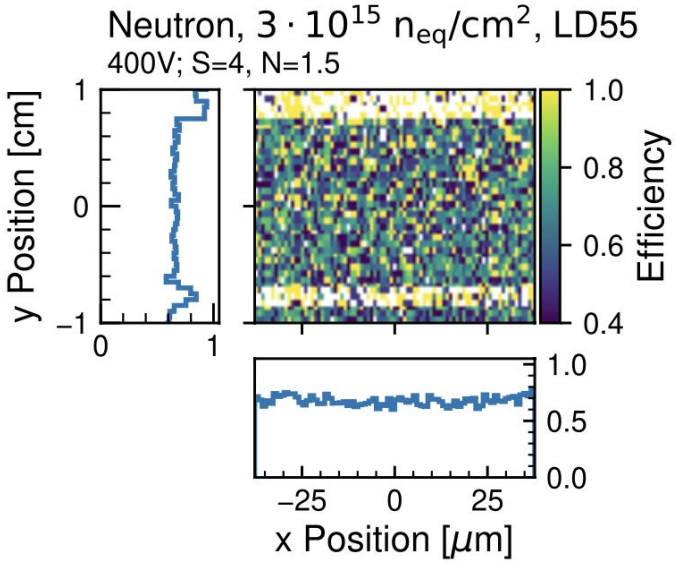



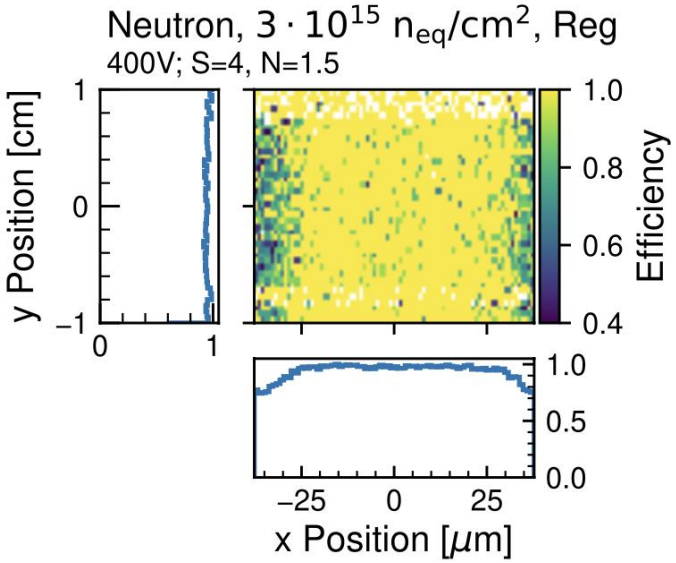



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

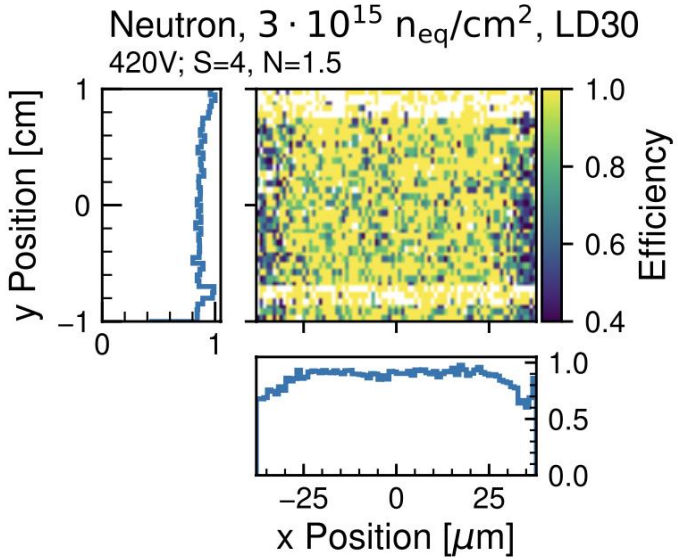


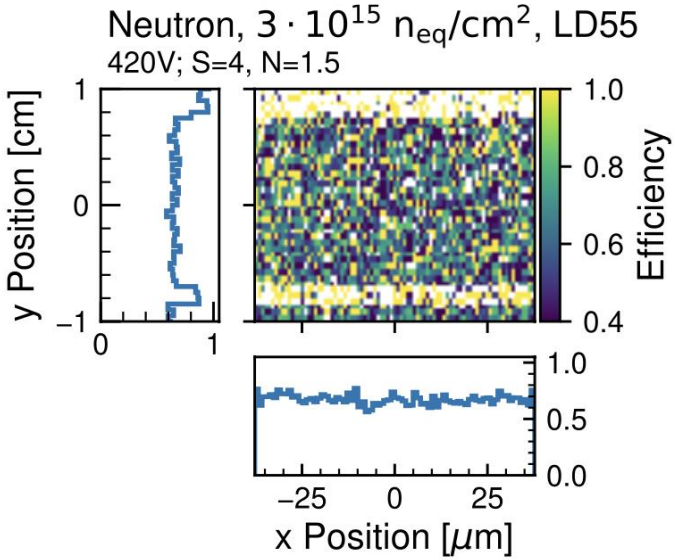



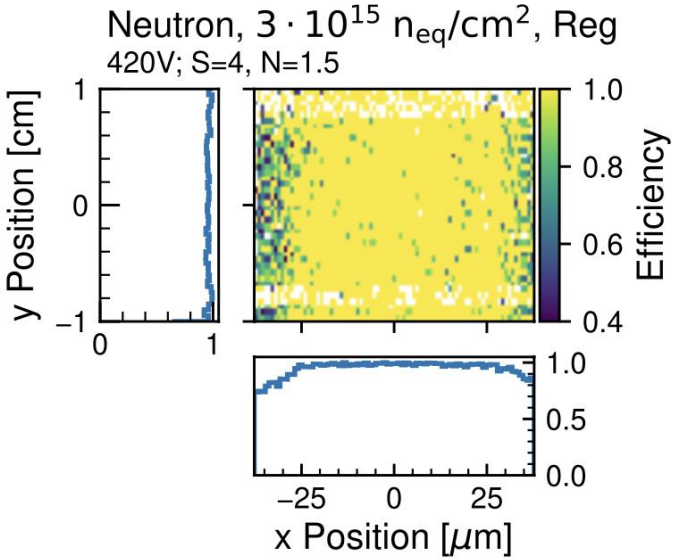



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

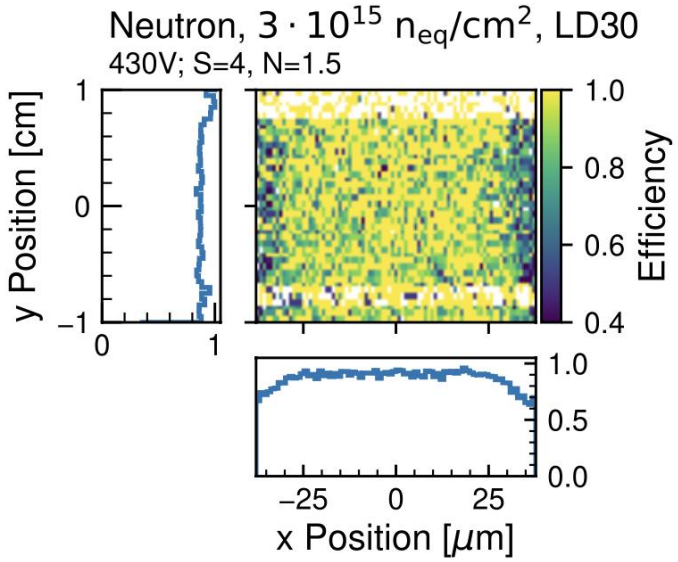


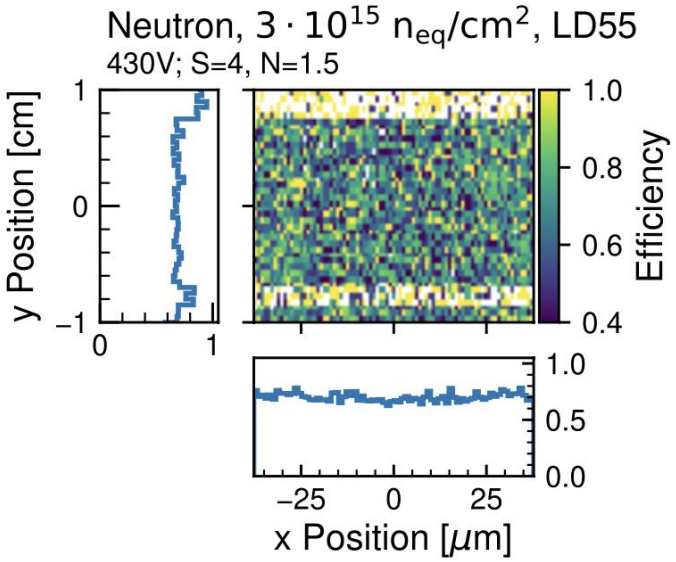



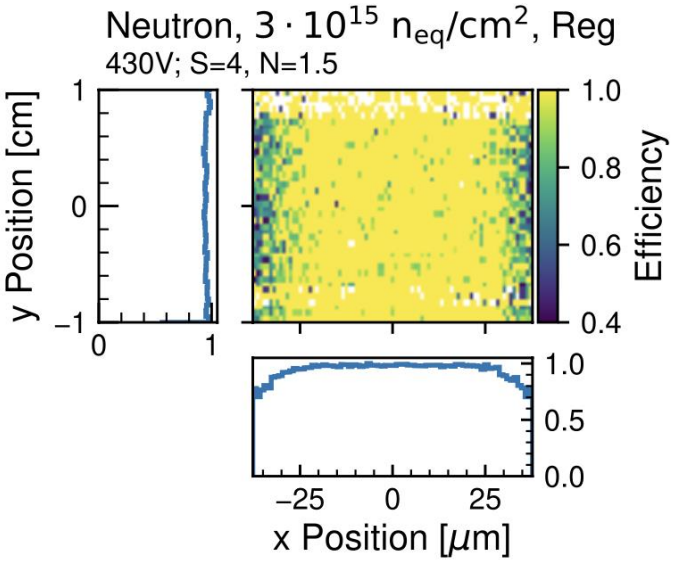



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

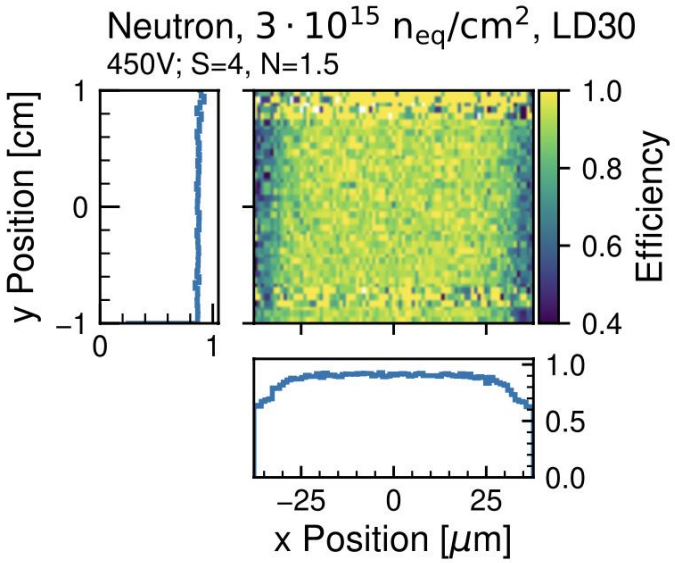


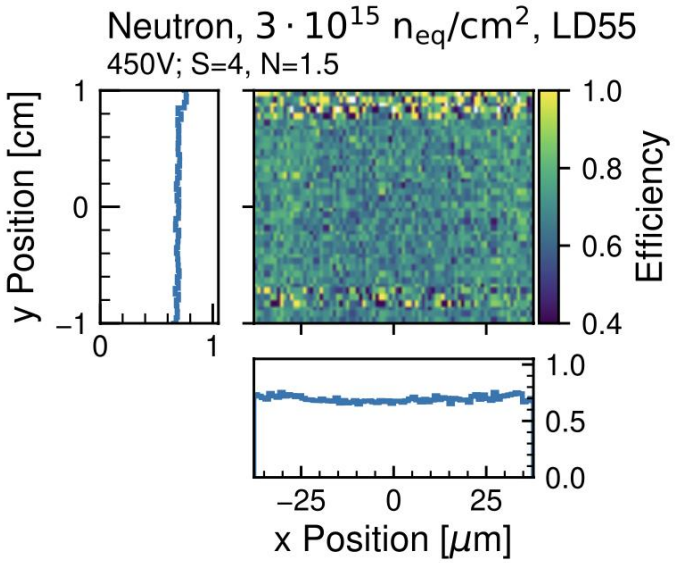



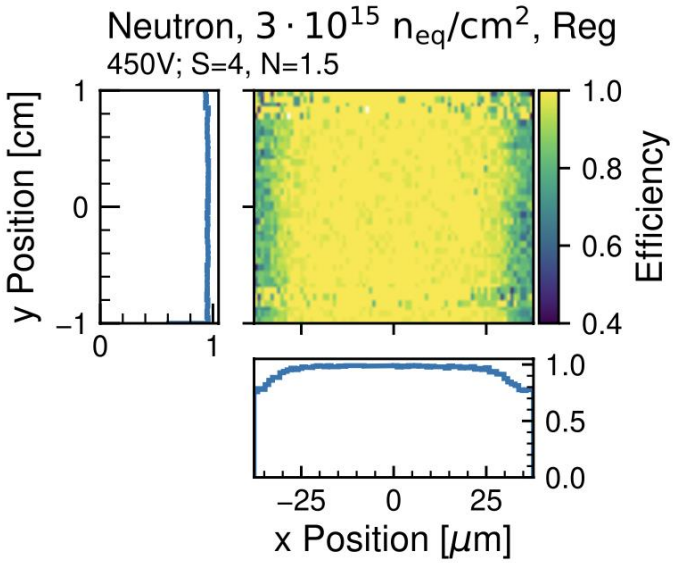



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

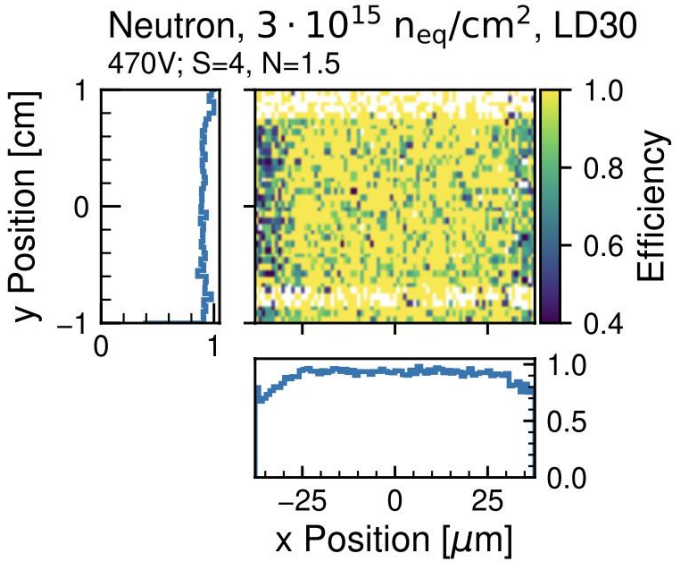


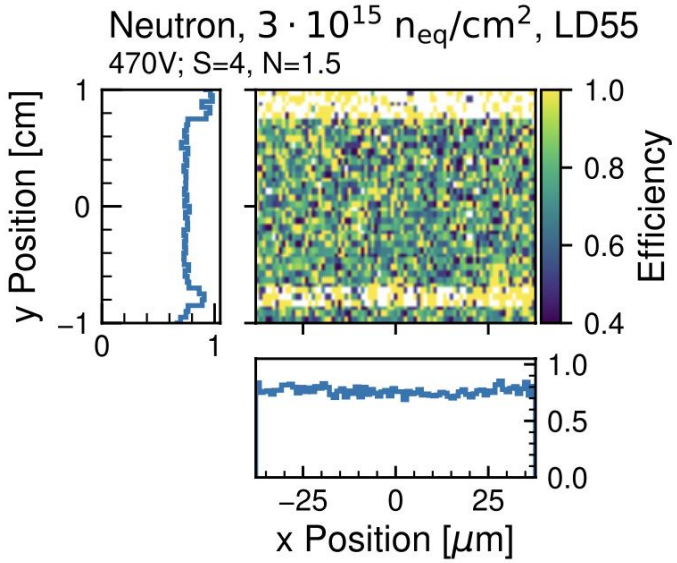



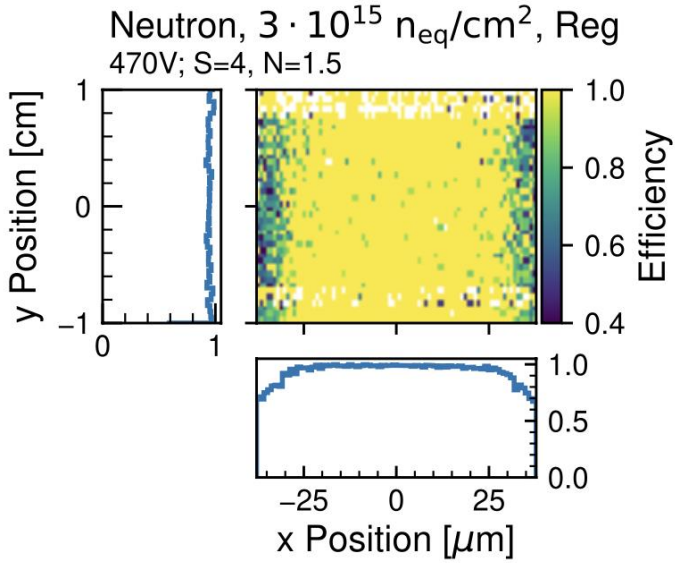



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

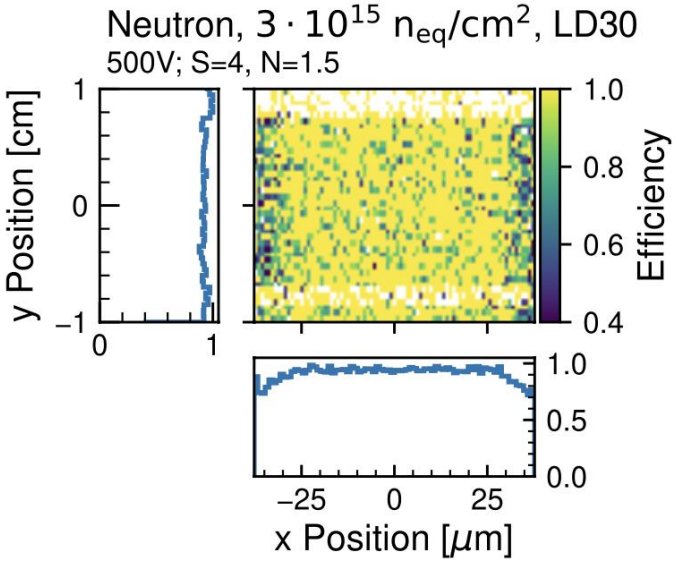


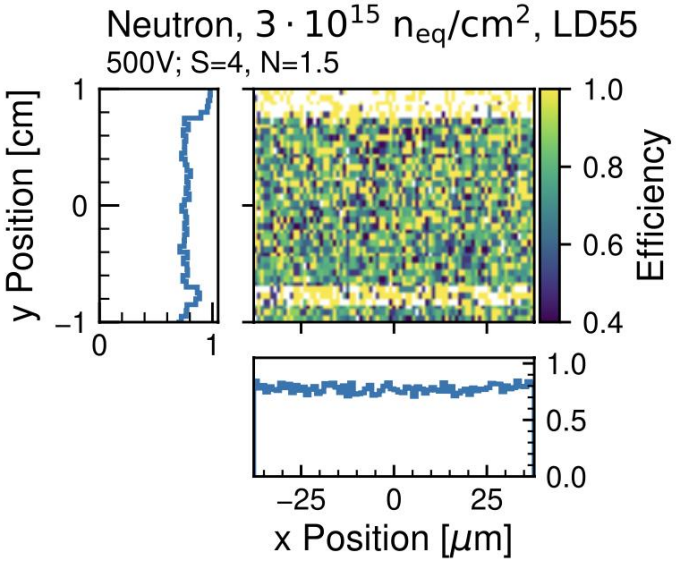



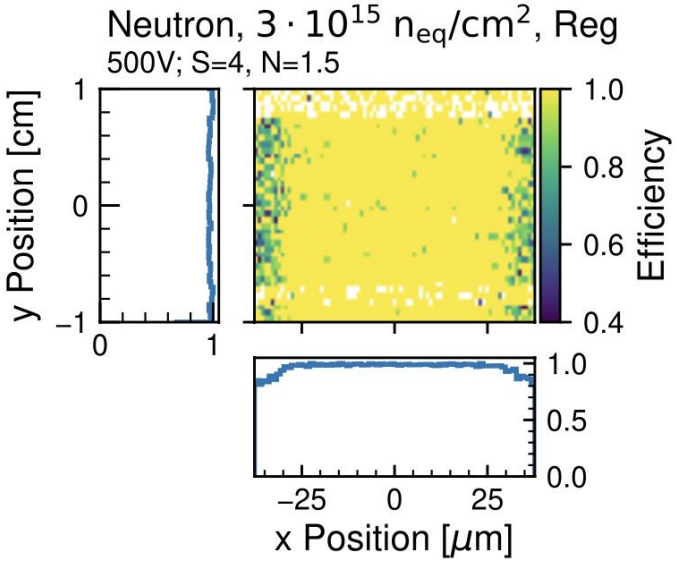



# **Passive CMOS Strips:** Efficiency Maps

- Efficiency increases with bias voltage: starts to increase for Regular (190 V), then LD30 (230 V to 250 V), then for LD55 Design (320 V to 350 V)
- "Efficient" region starts out wider than strip implant.
- Width of efficient region stays constant after few voltage steps
- Overall efficiency continually grows
- Stitching not visible anywhere in efficiency map -> stitching successful, even after irradiation!

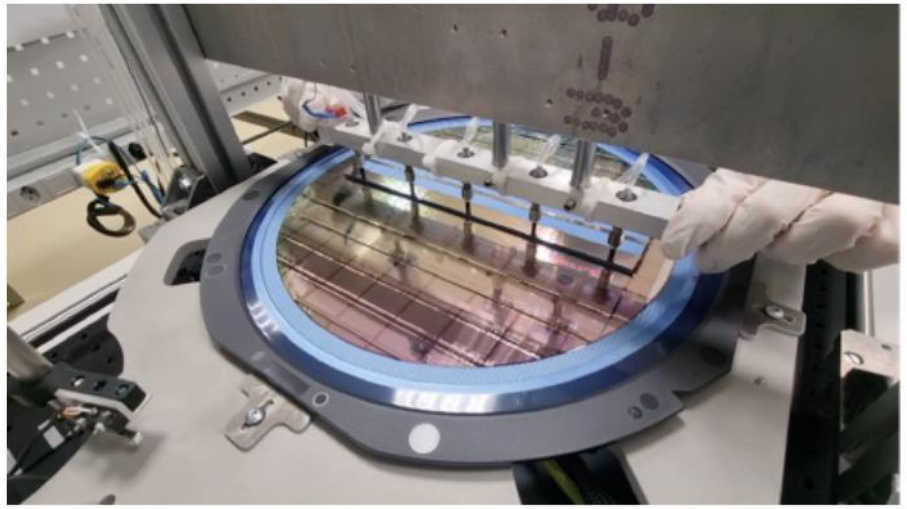


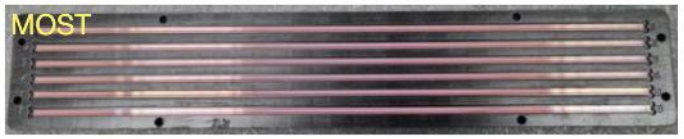



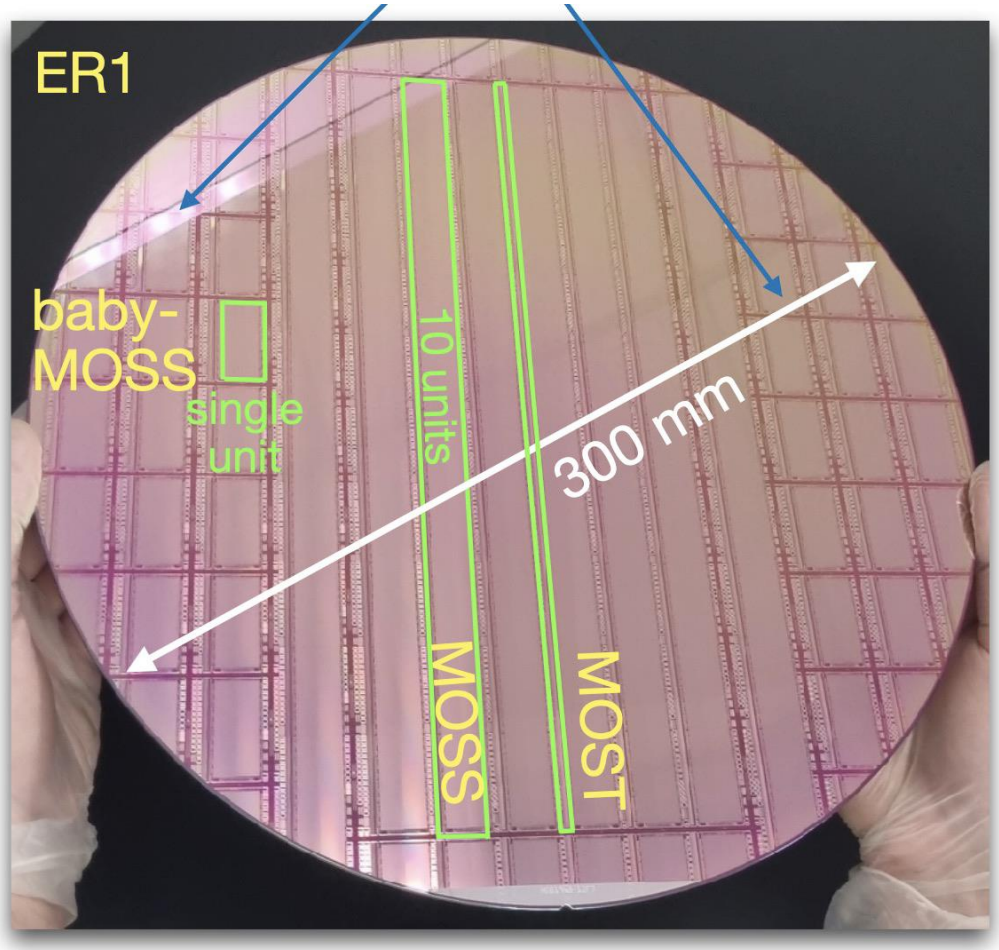



# ALICE Stitching Full Diameter on 12“ Wafer: CERN ER1 Project (Pix) MOSS/MOST

- **MOSS:** 14 mm × 259 mm, 6.72 Mpixels, (22.5 × 22.5 and 18 × 18 µm2), conservative design and layout, different layout densities
- **MOST:** 2.5 mm × 259 mm, 0.9 Mpixels (18 × 18 µm2), full density design, global power network & conservative power switches



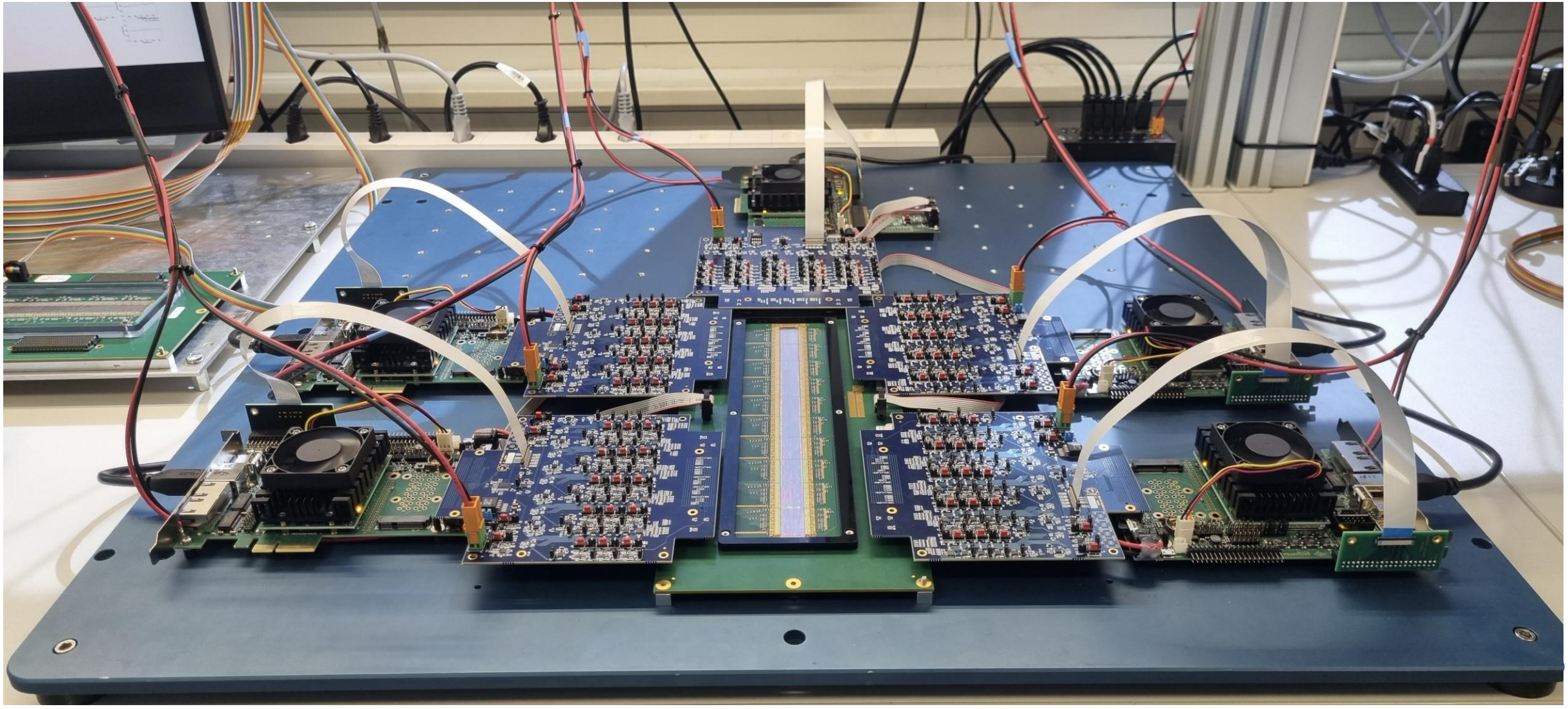




W. Snoeys EP Seminar, indico.cern.ch/event/1461789/

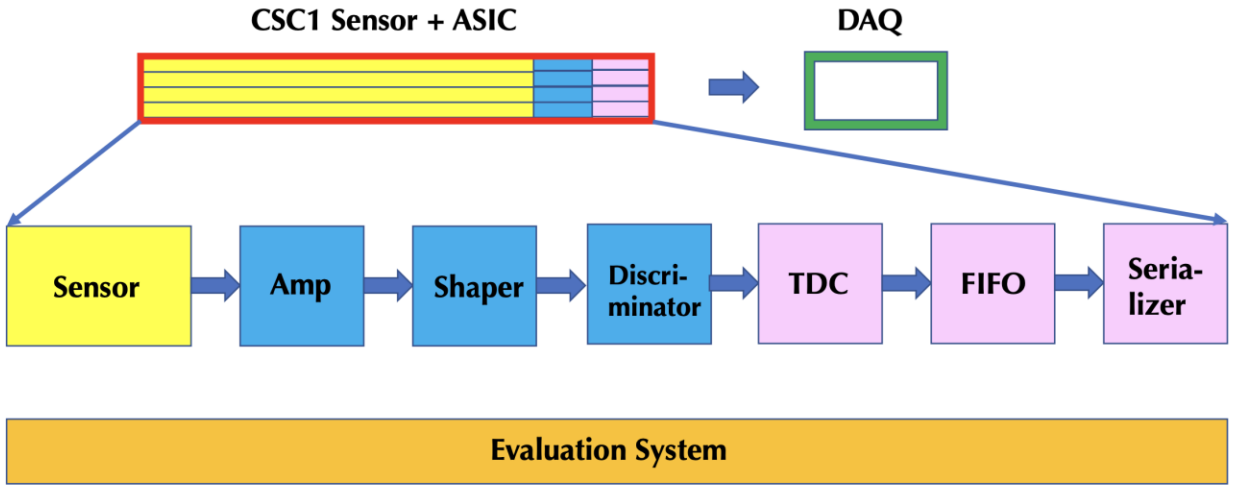
# ALICE MOSS Tests

- **Would already be a significant strip device, but a 26cm pixel sensor is a very complex beast!**
- **Valuable Lessons** on stitching, yield, handling, powering scheme, leakage currents,…..



# Continuing the Passive CMOS Strips Line

- **Two DRD3 Projects directly target large area silicon as for FCC:**
- **Bonn, DESY, Dortmund, Freiburg, “Monolithic strip sensors for large area detectors” (Jens Weingarten): monolithic but skip stitching this time, FCC-ee and others**
- **IHEP Bejing (plus many Chinese groups and labs), “CMOS Strip Chip for Future Tracking Detector”, targeting CEPC, would work for FCC-ee, (Xin Shi).**

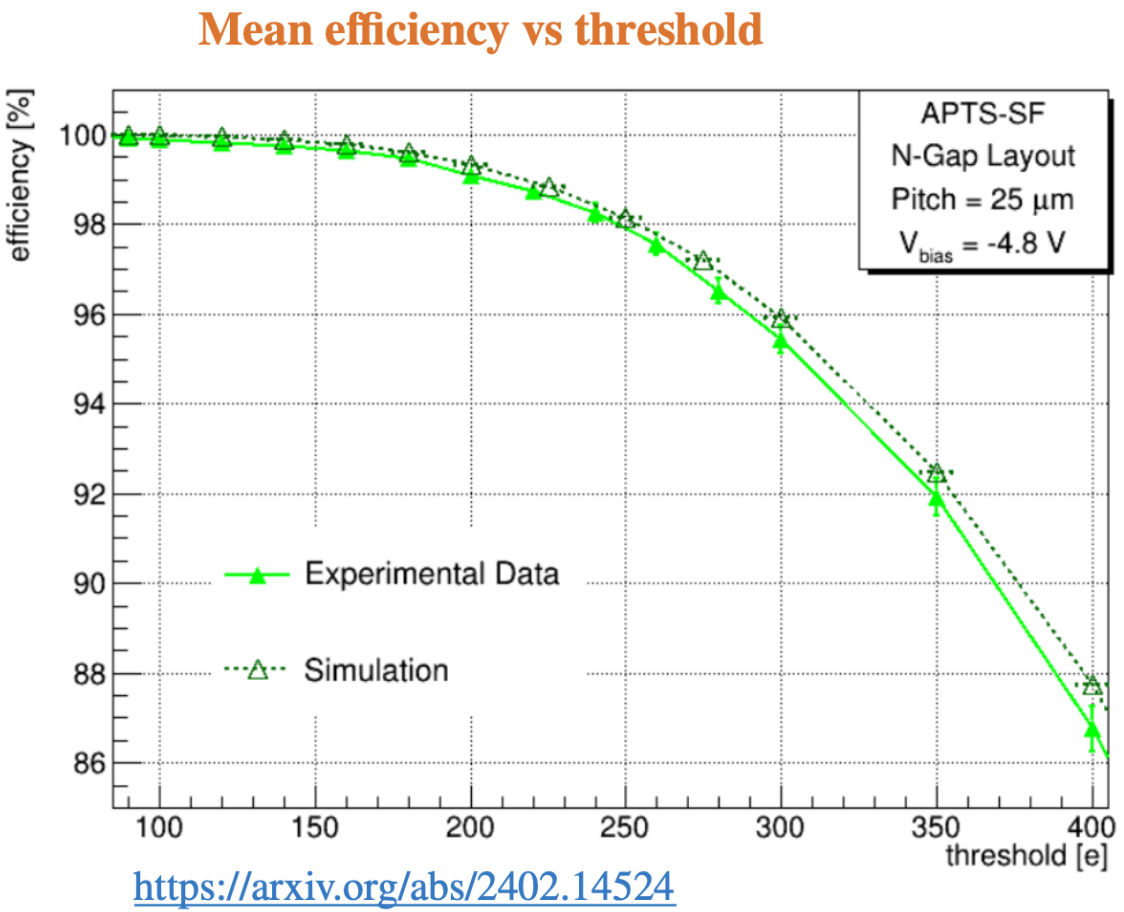


# Other Projects: Tangerine

https://www.sciencedirect.com/science/article/abs/pii/S0168900222004508

- Make sensors in 65 nm CMOS imaging process for particle physics applications
- Driven by DESY
- Sensors have been designed, extensively simulated, fabricated and thoroughly tested
- Efficiency vs. threshold results from the “Analog Pixel Test Structure” (APTS) (right). Trend between simulations and data matches well.

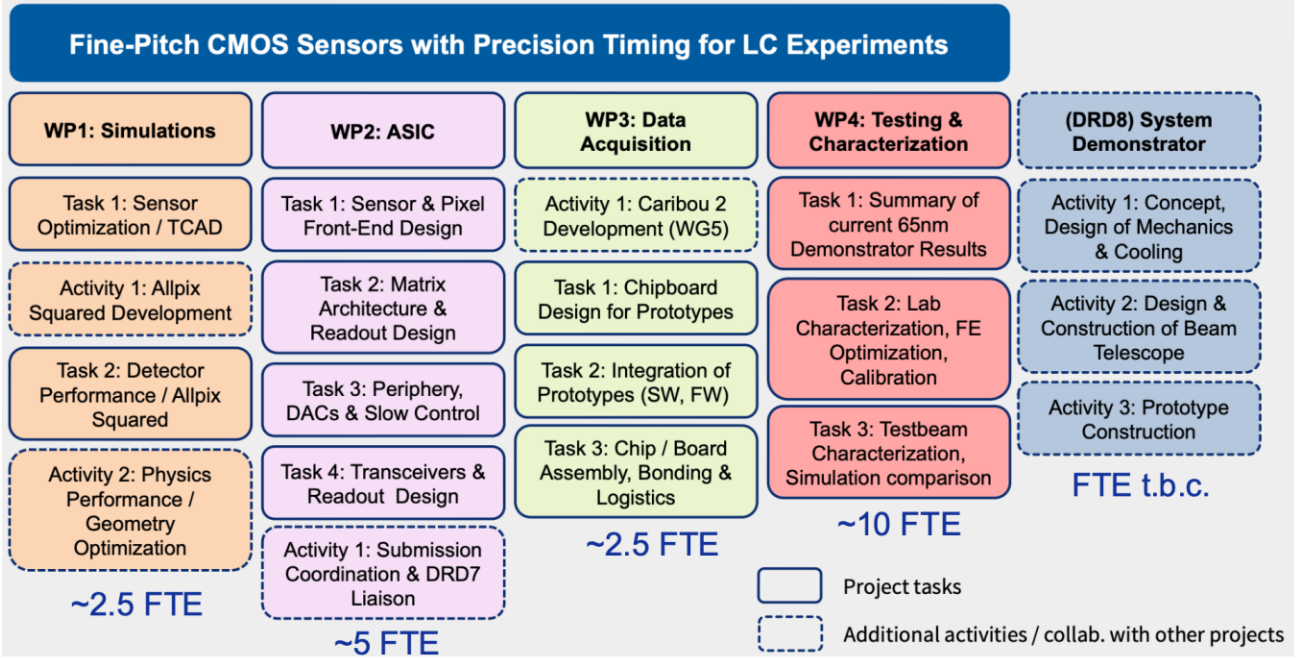
- https://www.sciencedirect.com/science/article/abs/pii/S0168900222004508




H. Wennköf, B'ham Seminar, indico.cern.ch/event/1382468//

# Other Projects: Octopus („successor“ of Tangerine)

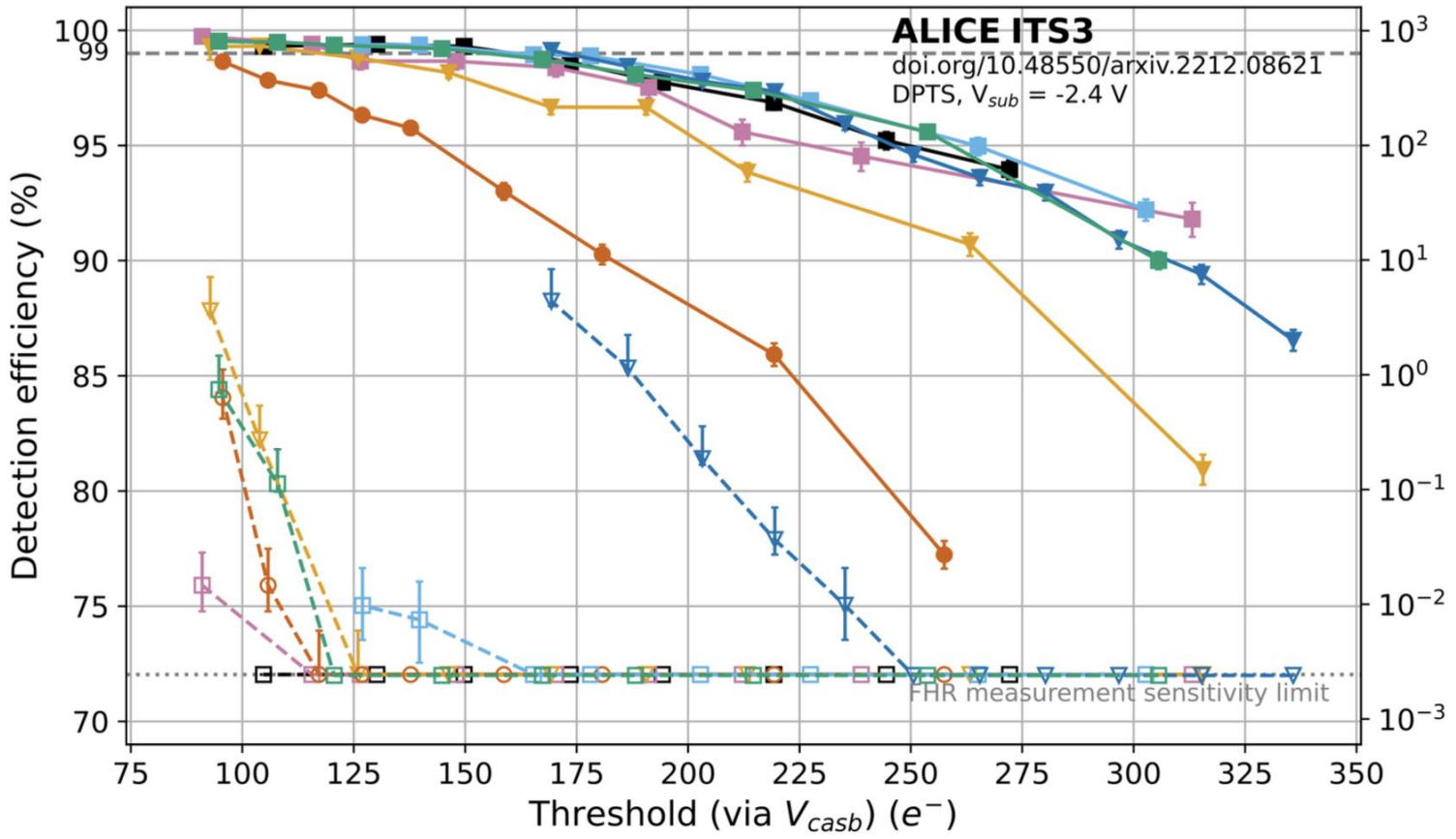
- DRD3 WP1 (CMOS) project proposal (one of 16)
- TPSCo 65 nm CMOS, 11 institutes, 38 people
- Closely linked to TPSCo65 schedule, also DRD7
  - DRD7: HEP Electronics and on-detector processing
- Fine-Pitch CMOS Sensors with Precision Timing for Lepton-Collider Experiments
- Staged approach to enable refinement of architecture in view of final development targets




D. Dannheim https://indico.cern.ch/event/1469442/

- https://indico.cern.ch/event/1469442/contributions/6186575/attachments/2955392/5196443/LC-Vertex-DRD3-Update-28Oct2024.pdf

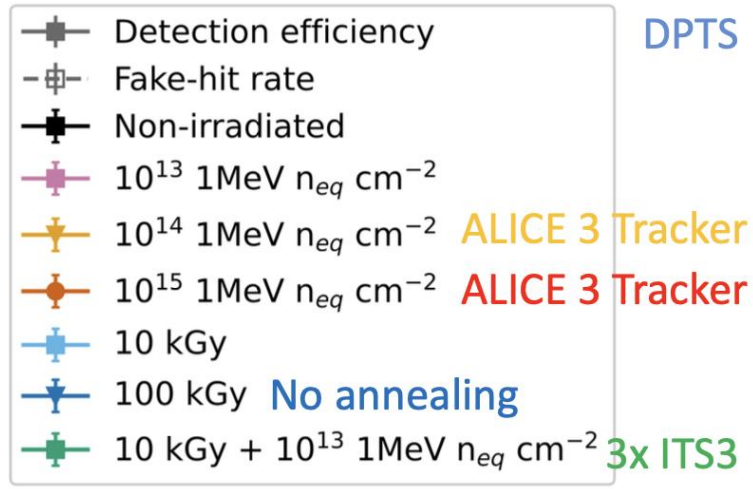
# Radiation Hardness Example from ALICE ITS3




W. Snoeys EP Seminar, indico.cern.ch/event/1461789/

- 99% efficiency at 3x$10^{15}$ $n_{eq}$/$cm^2$
- Vast majority of sensors at 3x$10^{15}$ $n_{eq}$/$cm^2$ require cooling to -20 at least, but this is achieved at room temperature!

- For full details: doi: 10.1016/j.nima.2023.168589



# Conclusions and Take Home Messages

## Main Conclusions

- Many international projects on (CMOS) Silicon sensors for FCC tracker underway
- Various technology nodes under study, from 180nm down to 55nm (mostly 65nm)
- By the time we build any FCC detectors, there will be other technologies
- Large international effort
- Radiation hardness up to $3x10^{15}$ $n_{eq}/cm^2$ demonstrated already
- FCC-hh fluences are a challenge, but can be met on the time scale given

## Take Home Messages

- If we had to build an FCC tracker in 10 years we could deliver
- On that timescale, it would be monolithic CMOS with spacial resolution as desired, and timing resolution of ~25ps or better
- 25ps timing better than required, penalties are power and mass, but future trackers likely 4D
- Assuming we have more time, Si detector R&D will still advance and/or we might have something “better”
- “Better” can mean “cheaper”, i.e., delivering the same performance at lower cost
- If the Physics Case is convincing and the funding is secured, the Si detector will materialise

# Links, Stuff, Backup

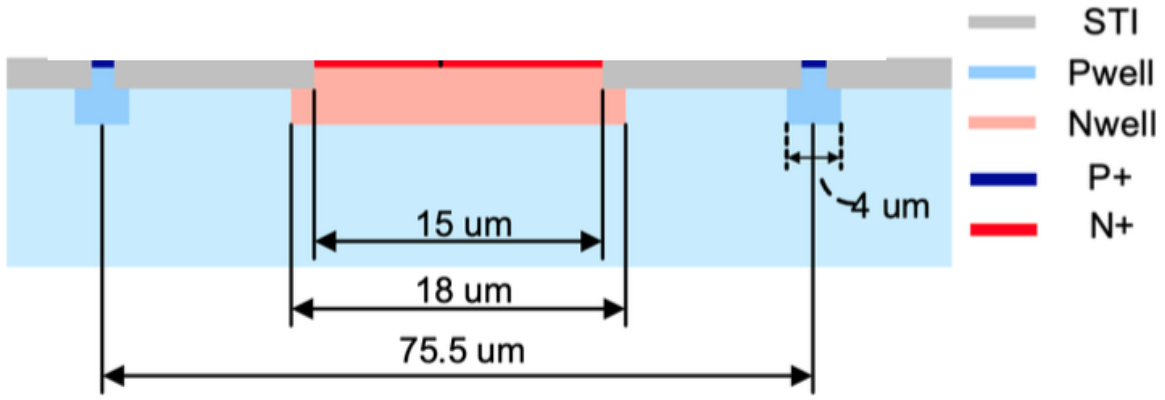
- Material: Walter Snoeys‘ excellent CERN Detector Seminar: https://indico.cern.ch/event/1461789/

# Silicon for FCC and DRD3

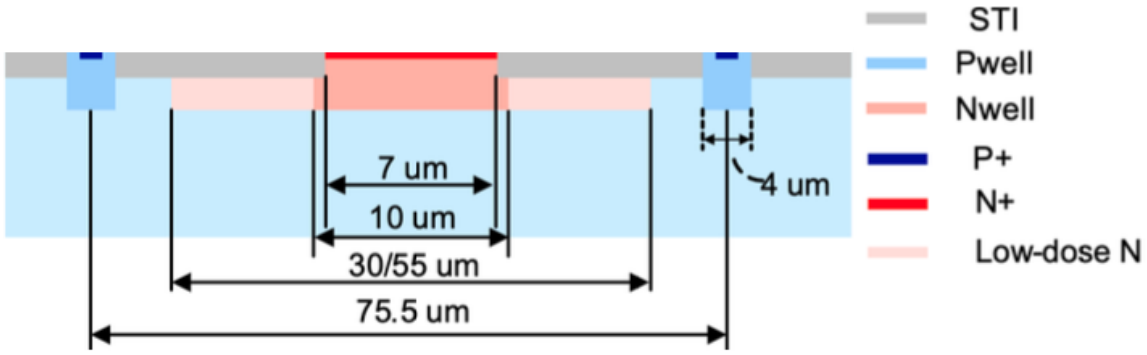
| WG1 research goals <2027 | |
|---|---|
| | **Description** |
| RG1 | Spatial resolution: ≤3 µm position resolution |
| RG2 | Timing resolution: towards 20 ps timing precision |
| RG3 | Readout architectures: towards 100 MHz/cm$^2$, 1 GHz/cm$^2$ with 3D stacked monolithic sensors, and on-chip reconfigurability |
| RG4 | Radiation tolerance: towards $10^{16}$ $n_{eq}$/cm$^2$ NIEL and 500 MRad |
| RG5 | Low-cost large-area CMOS sensors |

# Passive CMOS Strip Design Variants

**Regular**




**Low Dose 30 & 55**



# Radiation Damage Models in TCAD

**Surface effects**
oxide charge build- up
interface trap states formation

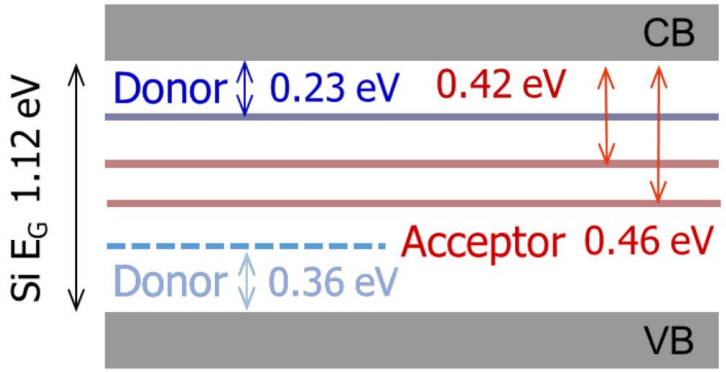
**Bulk effects**
deep level traps
recombination centres creation

**LHCb/CERN Bulk Model**

**Perugia Bulk+Surface Model**

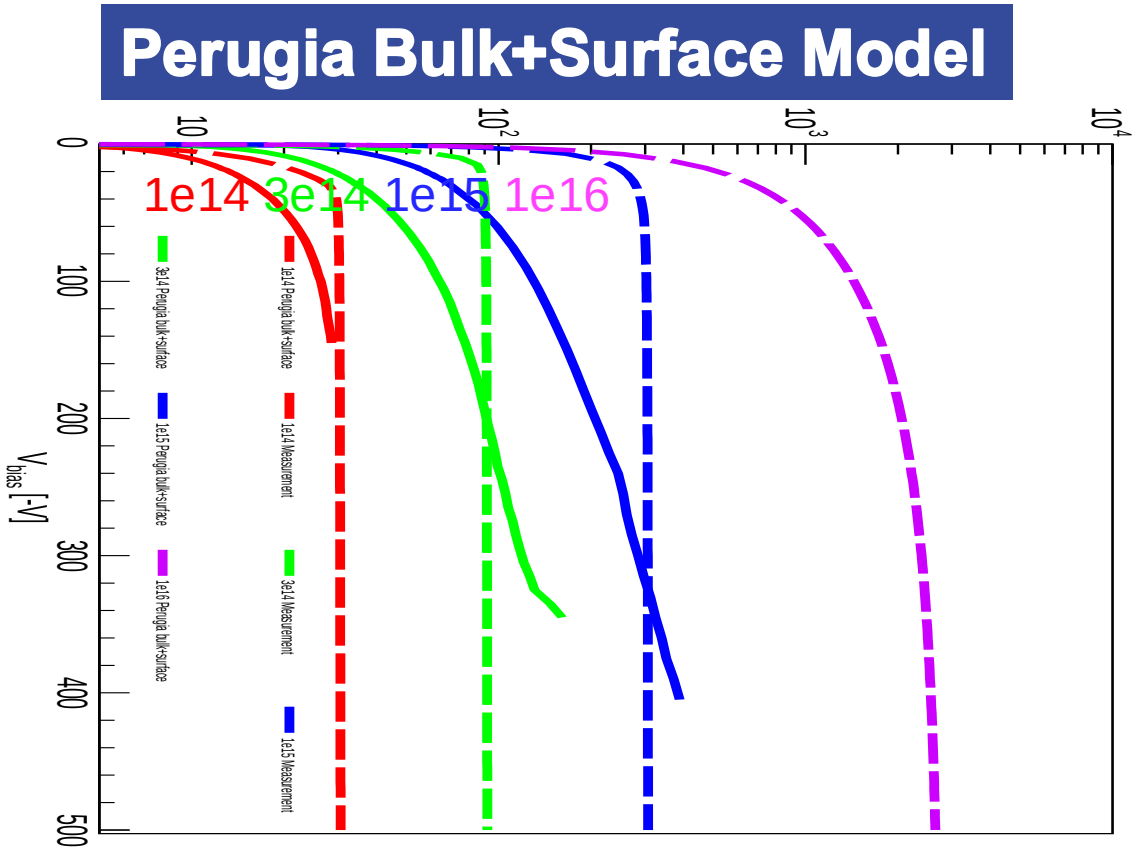
**Introducing traps in silicon region**

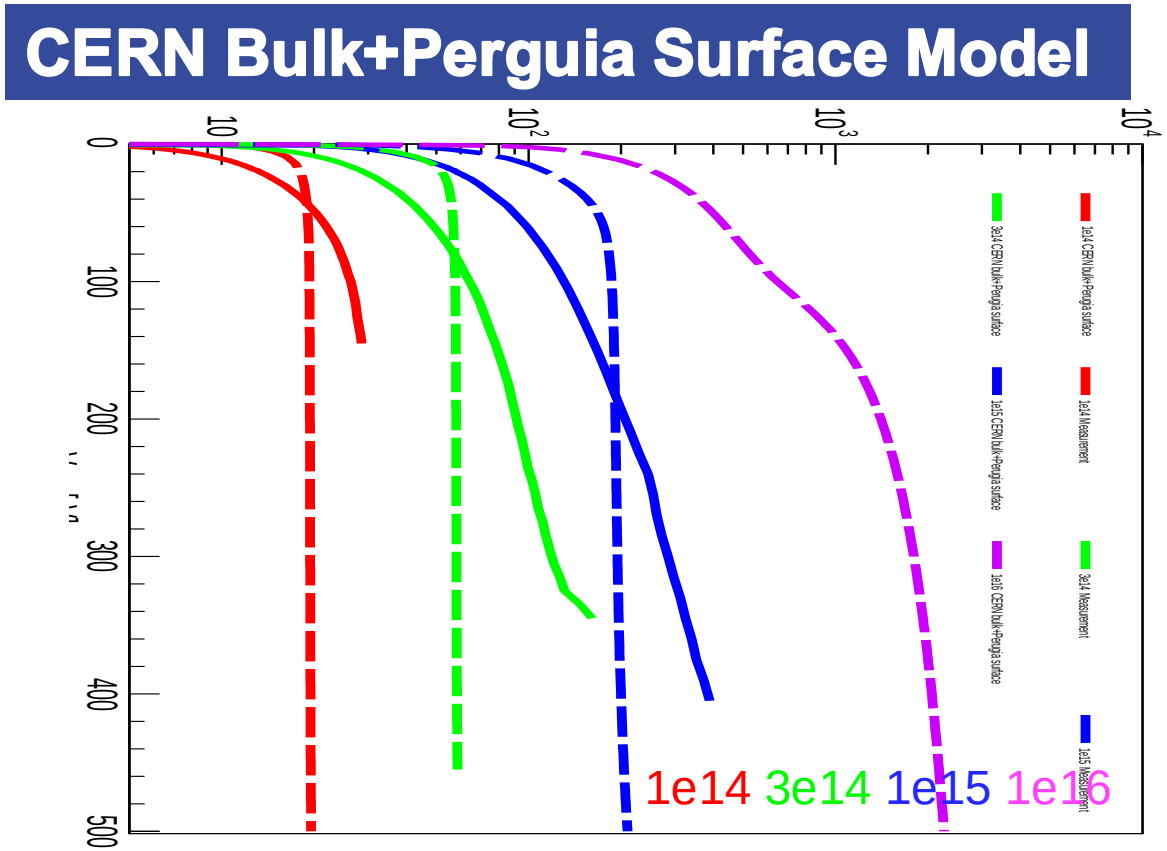
**Modifying recombination models**




← Bulk trap levels distribution in the Perugia model

# Passive CMOS Strips:
## Leakage Current Post-Irradiation: Measured and Simulated




Dashed line: simulation
Solid line: measurement

Proton and neutron irradiated,
all fluences NIEL, T = -30 °C