DAQ proposal
for the AIDA Single Arm Large Area Telescope (SALAT)

Based on our experience in DAQ systems

- **IPHC beam Telescopes DAQ for MAPS (VME, USB, PXI, PXIe)**
- **EUDET beam Telescope DAQ migration to National Instrument COTS DAQ HW**

COTS HW → National Instrument PXI Express Flex RIO board

Pixels sensor
Digital outputs

Front End
PXI 658532 I/O LVDS

Acquisition board
Flex RIO Board - PXIe 7962R

PXIe crate = Front End + Flex RIO + CPU
(Ultimate Telescope DAQ → 230 MB/s → No dead time)

IPHC PICSEL group - ASICs Test & Characterization team
http://www.iphc.cnrs.fr/-PICSEL-.html - Gilles CLAUS – gilles.claus@iphc.cnrs.fr

DAQ developer …

Difficult to follow
MAPS data throughput …

Outline

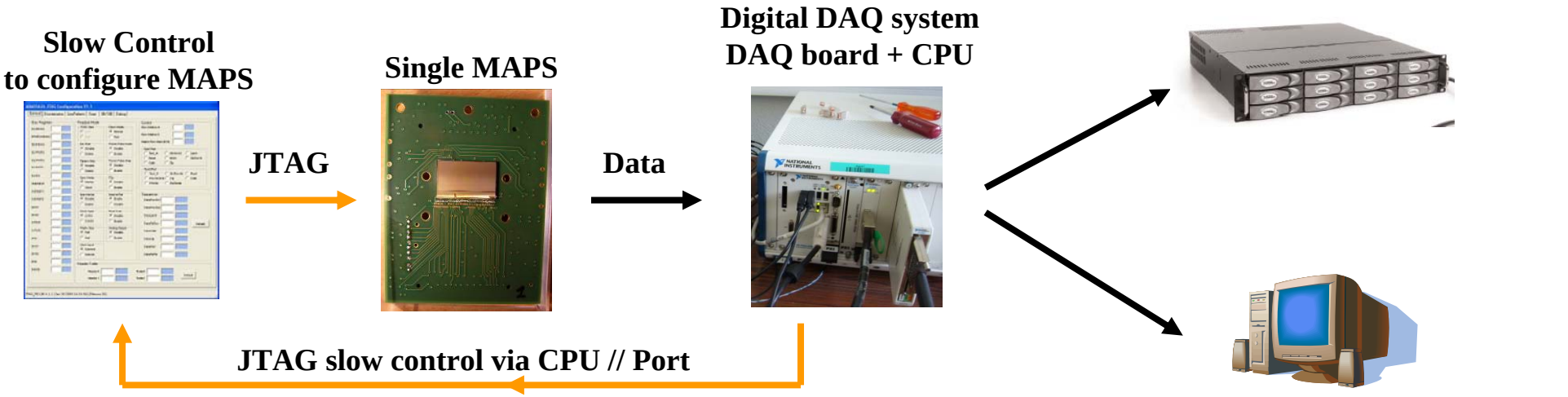
- Smart Digital MAPS (Mimosa 26, Ultimate) Steering & Readout
- DAQ system for MAPS
- Migration to National Instruments COTS DAQ … Why ?
- Successful DAQ projects based on PXIe Flex RIO
- SALAT Steering & Readout
- DAQ proposal for SALAT
- Conclusion / Planning

MAPS sensor …

10 000 frames/s …

MAPS Steering & Readout : Single MAPS DAQ architecture

DAQ architecture for single MAPS



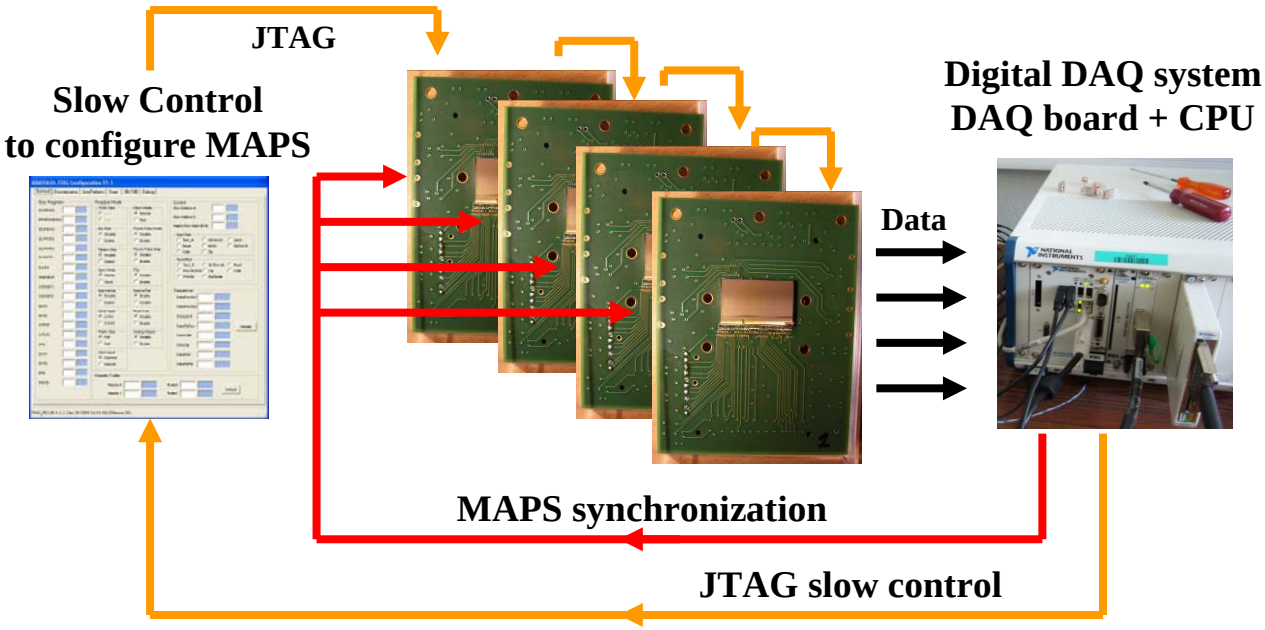
MAPS characterization / validation
→ Save data on disk
→ Off-line data processing

Integration in HEP Experiment
→ General Run Control
→ Send data on Gb/s Ethernet

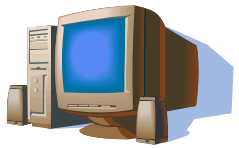
- **Steering**
  - MAPS configuration → JTAG slow control SW running on crate CPU
  - Start MAPS by slow control command
- **Readout**
  - Acquire data (DAQ board firmware)
  - Reformat data (CPU board software)
  - Save data on disk OR send them on Ethernet to run control PC

MAPS Steering & Readout : Multiple MAPS DAQ architecture

DAQ architecture for multiple MAPS



MAPS characterization / validation
- → Save data on disk
- → Off-line data processing



Integration in HEP Experiment
- → General Run Control
- → Send data on Gb/s Ethernet

- **Steering**
  - MAPS configuration → JTAG slow control → Serial chain of MAPS
  - All MAPS should / must run synchronously → Can't start by slow control → HW start needed
    - DAQ sent Clock & Start signals to all MAPS (Start distribution scheme)
- **Readout**
  - Acquire data (DAQ board firmware) & Reformat data (CPU board software)
  - Save data on disk OR send them on Ethernet to run control PC

MAPS Steering & Readout : Readout protocol

MAPS readout

- Proprietary serial protocol → 4 x LVDS pairs
  - Clock 80-160 MHz (CLKD)
  - Frame Synchro (MKD)
  - Two data lines (D00, D01)
  - Data throughput 20 – 40 MB/s
- Readout of Multiple MAPS
  - Only one MAPS provide Clock & Sync
- Same protocol for Mimosa 26 & Ultimate

Mimosa 26 (EUDET) & Ultimate (STAR)

The Mimosa 26 sensor (2009)

- Area ~ 2 cm x 1 cm = 2 cm² - 663 552 Pixels
- 8680 frames / seconde
- Clock 80 MHz – Stream ~ 20 MB/s

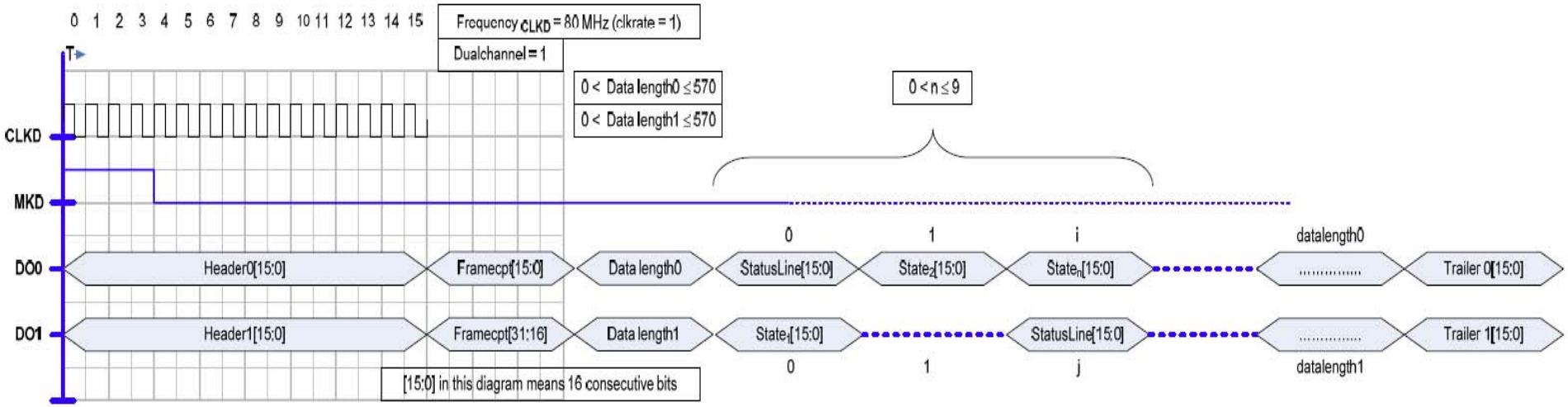
Mimosa 26

The Ultimate sensor (2011)

- Area ~ 2 cm x 2 cm = 4 cm² - 890 880 pixels
- 5388 frames / seconde
- Clock 160 MHz – Stream ~ 40 MB/s

Ultimate

Proprietary readout protocol of Mimosa 26



DAQ board specifications

- **Inputs signals (LVDS)**
  - **2 synchro signals (clock, frame sync)**
  - **+ 2 Data links / MAPS**
  - **Frequency range up to 160 MHz**

How to follow the MAPS ?

➡ **6 Planes Telescope = 14 inputs**

- **Input data stream processing**
  - **Deserialize data → Must be done by firmware**
  - **Proprietary protocol → Can be handle by software**

➡ **Specific firmware needed**

- **Data throughput (worst case = Ultimate)**
  - **6 Planes Telescope with Ultimate → 230 MB/s**

➡ **Bandwidth ~ 250 MB/s**

But don't build complex DAQ !

DAQ system for MAPS : NI PXIe 7962R Flex RIO board

NI FlexRIO FPGA Modules

NI PXI-795xR, NI PXIe-796xR *NEW!*

- NI FlexRIO FPGA modules
- PXI and PXI Express
- Xilinx Virtex-5 SXT and LX FPGAs
- Programmable with the LabVIEW FPGA Module
- Up to 512 MB onboard DRAM
- Peer-to-peer data streaming between PXI Express modules at more than 800 MB/s
- Up to 16 DMA channels
- 132 single-ended or 66 differential data lines to adapter module interface
- Up to 66 Gbits/s adapter module bandwidth
- Multi-adapter module synchronization for high-channel-count applications
- Adapter modules available from NI and third parties as well as through custom development with the NI FlexRIO Adapter Module Development Kit (MDK)

Operating Systems
- Windows 7/Vista/XP/2000
- LabVIEW Real-Time

Required Software
- LabVIEW
- LabVIEW FPGA Module

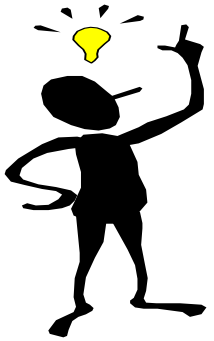
Recommended Software
- NI FlexRIO Adapter Module Development Kit

Driver Software
- NI-RIO
- NI FlexRIO adapter module support

Model	Bus/Form Factor	FPGA	FPGA Slices	FPGA DSP Slices	FPGA Memory (Block RAM)	Onboard Memory (DRAM)
NI PXIe-7965R	PXI Express	Virtex-5 SX95T	14,720	640	8,784 kbits	512 MB
NI PXIe-7962R	PXI Express	Virtex-5 SX50T	8,160	288	4,752 kbits	512 MB
NI PXIe-7961R	PXI Express	Virtex-5 SX50T	8,160	288	4,752 kbits	0 MB
NI PXI-7954R	PXI	Virtex-5 LX110	17,280	64	4,608 kbits	128 MB
NI PXI-7953R	PXI	Virtex-5 LX85	12,960	48	3,456 kbits	128 MB
NI PXI-7952R	PXI	Virtex-5 LX50	7,200	48	1,728 kbits	128 MB
NI PXI-7951R	PXI	Virtex-5 LX30	4,800	32	1,152 kbits	0 MB

Requirements

- **> 14 inputs @ 160 Mhz**
- **User defined FW**
- Bandwidth **~ 250 MB/s**
- **CPU power** needed



NI PXIe Flex RIO board

- Mother board + Front End
- I/O adaptator module
  - **LVDS - 40 Inputs 200 Mhz**
- **User** can **implement** his own **FW**
  - **Virtex 5**
- PXIe bus data throughput
  - **PXIe x 4 ~ 800 MB/s**
- PXIe architecture
  - **CPU power** available
- **Cost ~ 7 K€**
  - FE ~ 1 K€ + Flex RIO ~ 7 K€

DAQ system for MAPS : Development strategy with COTS

Pragmatic approach …

- Step by step Pragmatic approach
  - Don't start coding FW with LabVIEW FPGA …
  - Take time to look at / study Flex RIO board architecture
  - Make best use of on board HW (DRAM, Fifos) & Test them !!!
    - FW & SW test benches to evaluate each HW piece you need
  - Translate your application to Flex RIO FW → May be difficult …
    - Better to → Make your application fits with Flex RIO HW & FW Vi
      - It doesn't mean reduce application performances !

Firmware …

- Find the best trade off between FW & SW
  - Code Fast BUT Simple processing in FW → Data deserialization
  - Keep Complex BUT Slow processing in SW → Protocol handling

Software …

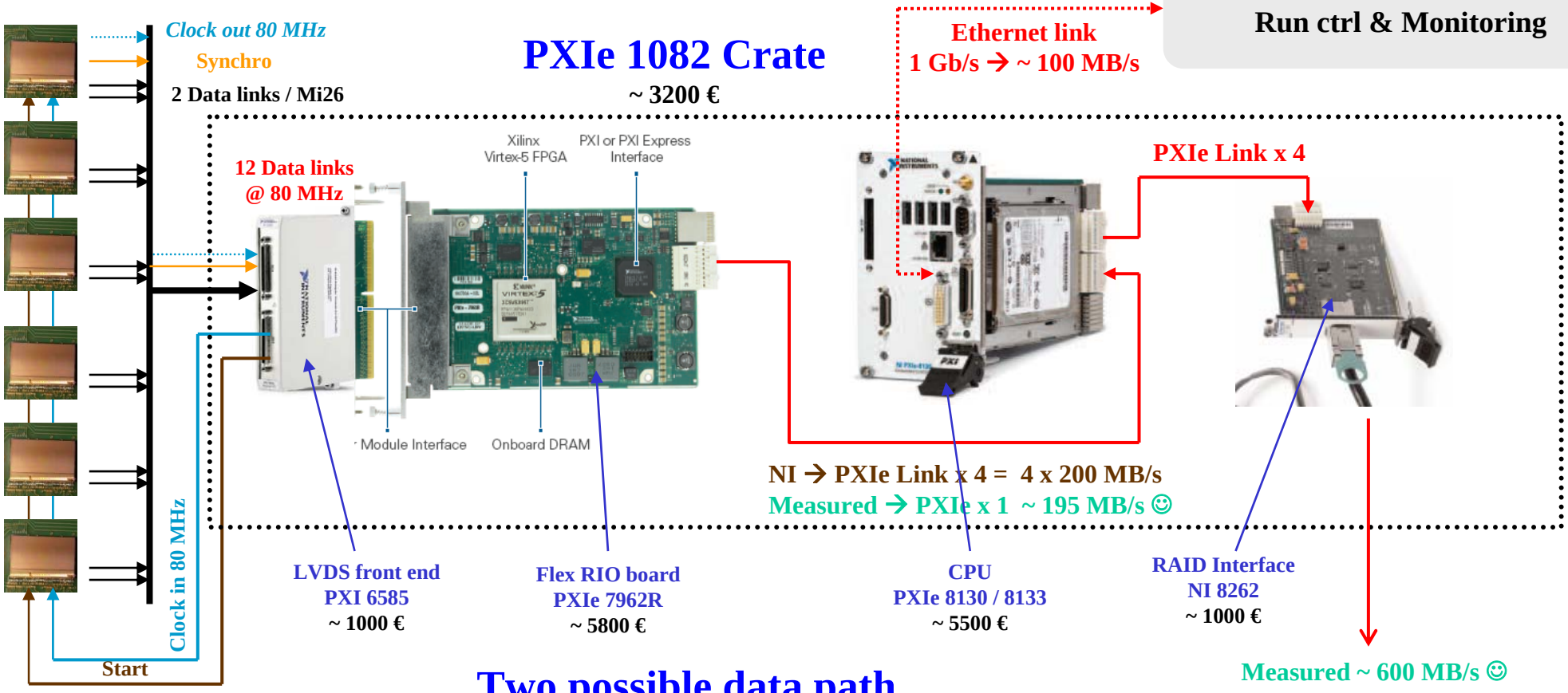
Migration to NI COST … Why ?

USB 2.0 board
4 Ana in 12 Bits 50 MHz

- **Context**
  - In the past ... we have developed acquisition boards (VME, USB)
  - Since 2009 … DAQ migration to NI PXI & PXIe COTS
- **Why ?**
  - Flex RIO board performances fits with application needs
  - Board cost is low < 1 K€ / MAPS (8 MAPS / board tested → 0,88 K€/MAPS)
  - PXIe plateforme (Crate, CPU) cost ~ same as VME ~ 8-10 K€
  - Modularity & Scalability of NI PXIe plateforme
  - No manpower needed to produce, test and repair boards
  - Manpower can be focused on firmware & software development

Successful implementations of Flex RIO : The architecture

DAQ (15,5 k€) → Crate + Flex RIO + CPU + RAID (Option)



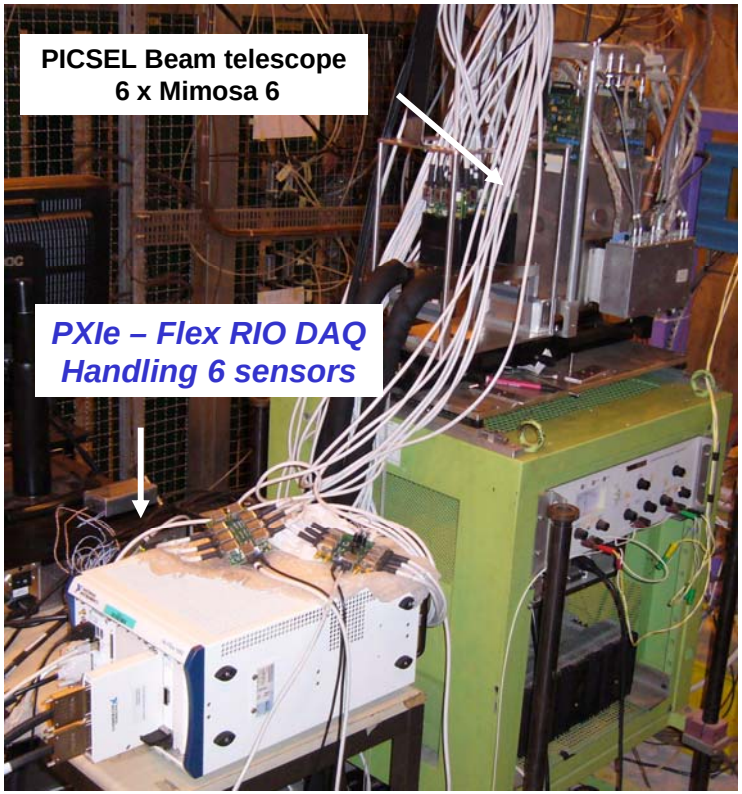
Two possible data path

- Sensors or Telescope Test & Characterization → RAID
- DAQ Integration in Experiment DAQ → Ethernet

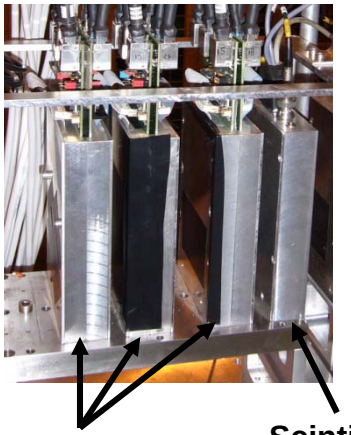
RAID Disk - 3 TB
HDD 8264
~ 4500 €

More about DAQ → http://www.eudet.org/e26/e28/Eudet-Memo-2010-25, 26, 27, 28

Successful implementations of Flex RIO : Mimosa 26 & Ultimate



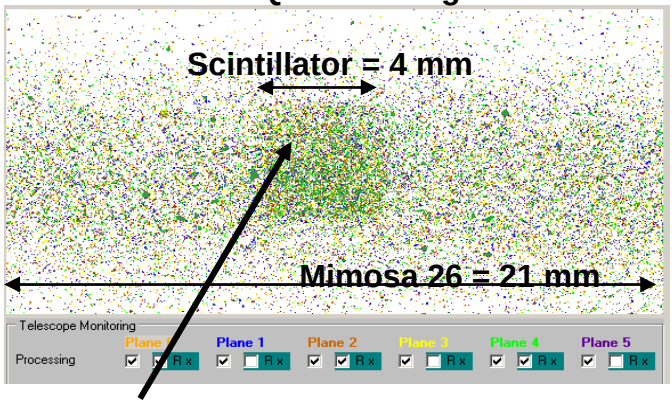
Beam telescope – 6 x Mimosa 6



Module
2 x Mimosa 26

Scintillator
4 mm x 4 mm

DAQ monitoring



Particles impacts
on sensor

Software & Firmware ?

- Board firmware → LabVIEW FPGA + VHDL
- CPU OS → Windows XP or Windows 7
- Software → LabVIEW + C/C++ code in DLL

NI PXIe Flex RIO DAQ implementation for IPHC PICSEL group Beam Telescopes

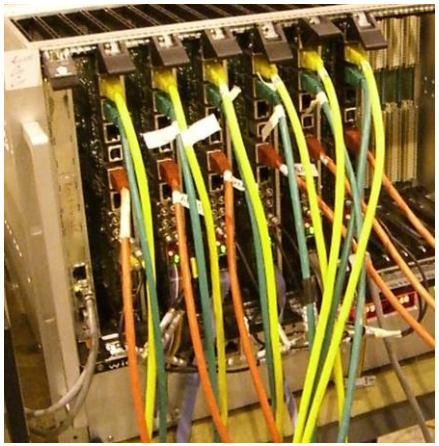
- 2010 - Mimosa 26 → 6 Sensors ~ 10 000 frames/s - Readout @ 80 MHz – 120 MB/s
- 2011 - Ultimate → 6 Sensors ~ 5 000 frames/s – Readout @ 160 MHz – 230 MB/s
- No dead time

Successful implementations of Flex RIO : EUDET Beam Telescope

EUDET JRA1 Beam telescope – 6 x Mimosa 26

EUDET → European Union project (FP6) 2006-2010
31 Institutes - 12 countries
Detectors R&D towards the International Linear Collider
JRA1 → Test Beam Infrastructure
JRA2 → Infrastructure for Tracking Detectors
JRA3 → Infrastructure for Calorimeters

Web → **www.eudet.org**



VME DAQ
→ 1 VME Board / Mimosa 26
→ 2 VME crates

DAQ specifications

- **Continuous readout of 6 x Mimosa 26 = 120 MB/s**
- **0 % dead time → Mandatory**
- **Migration from VME DAQ (INFN Ferrara) to NI Flex RIO PXIe**

Project → Tasks sharing

- **IPHC → Flex RIO Firmware + Software API + DAQ training (December 2010)**
  - **Development time + Validation → ~ 9 Men Months (Learning NI platform & tools included)**
- **DESY + Univ Geneva → Deployment in EUDET DAQ (Integration, Tests – Done in 2011)**

AIDA → European Union project (FP7) 2011-2014

80 Institutes - 23 countries

Advanced European Infrastructures for Detectors at Accelerators

9 Work Packages

WP9 → Advanced Infrastructures for Detectors R&D

Task9.3 → Precision Pixel Detector Infrastructures

→ aida.web.cern.ch/aida/index.html

Advancing European detector development

The AIDA project addresses infrastructures required for detector development for future particle physics experiments. In line with the European strategy for particle physics, AIDA targets user communities preparing experiments at a number of key potential future accelerators: SLHC (luminosity-upgraded LHC), future Linear Colliders (ILC and CLIC), future accelerator-driven neutrino facilities or future B-physics facilities (e.g. Super-B).

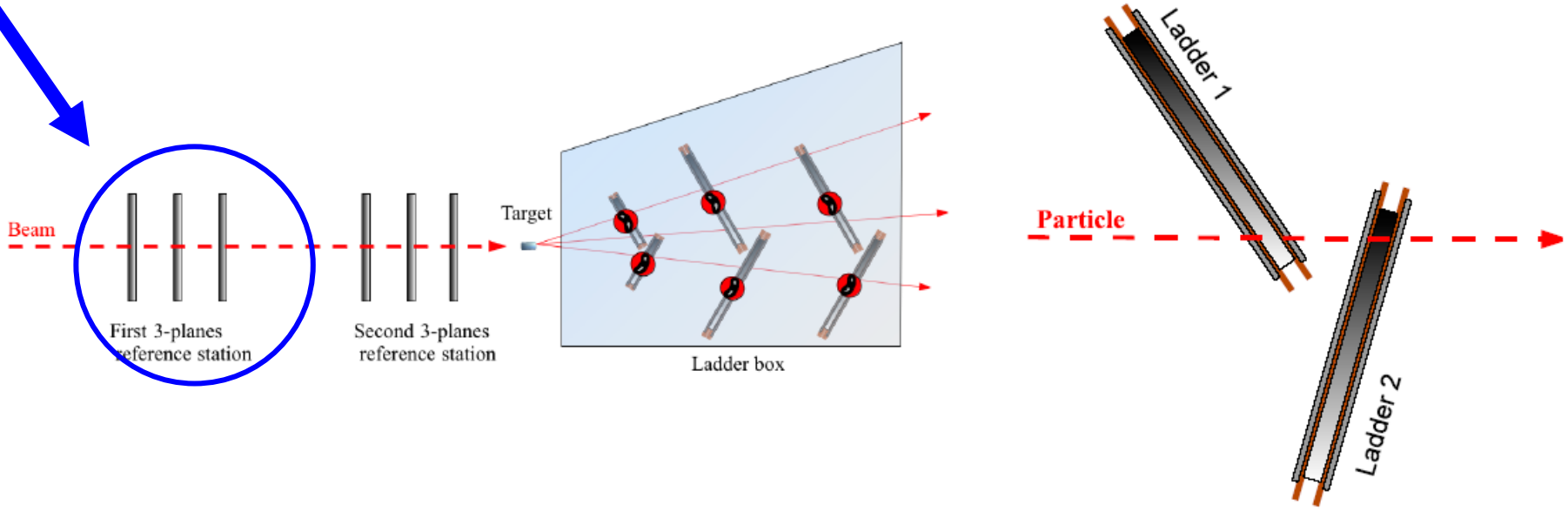
DESY wire chamber, courtesy of Interactions

The infrastructures covered by the AIDA project are key facilities required for an efficient development of the future experiments, such as: test beam infrastructures (at CERN and DESY), specialised equipment irradiation facilities (in several European countries), common software tools, common microelectronics tools and engineering coordination offices. The project, coordinated by CERN, involves more than 80 institutes and laboratories from 23 countries as beneficiaries or associate partners. *Read more >>*

SALAT Steering & Readout : Single Arm Large Area Telescope

VTX Oriented Infrastructures Proposed for AIDA WP-9.3

- On-beam test infrastructure:
  - Large Area beam Telescope (LAT) ⟼ has become Single Arm LAT ≡ SALAT
  - Alignment Investigation Devices (AID): mini-telescope and/or ladder box
  - Very thin removable target



M. Winter
AIDA kickoff – February 2011

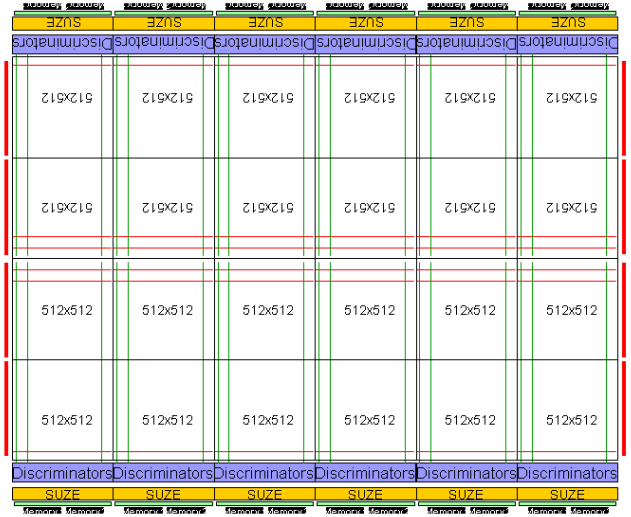
SALAT Steering & Readout : Demonstrator & Final sensors

SALAT sensor → ~ 25 cm² ~ 2 µm resolution → Reach goal in two steps

- 2012 → Demonstrator sensor
  - Assembling 4 x Ultimates on mylar foil
    - Avoid dead zone → Not like on this picture ;-)
  - 1920 columns x 1856 rows
  - Pitch 20,7 µm
  - 4 cm² x 4 cm²
  - Readout 185,6 µs

4 x Ultimate → ~ 4 cm x 4 cm = 16 cm²

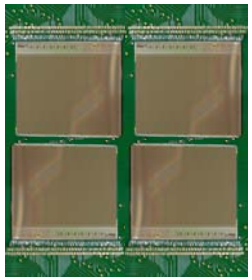
- 2014-2015 → Final sensor = MIMAIDA
  - stitching of 24 sensors (FSBB Full Scale Basic Block)
    - 1 cm x 1 cm
    - 512 x 512 pixels
    - 20 µm pitch
  - Total surface 6 cm x 4 cm
  - 3072 columns x 2048 rows
  - Readout ~ 200 µs



Final sensor → ~ 6 cm x 4 cm = 24 cm²

DAQ constraints demonstrator sensor (worst case)

- 2012 → Demonstrator sensor
  - Assembling 4 x Ultimates on mylar foil
  - 160 MHz signal – 40 MB/s



4 x Ultimate → ~ 4 cm x 4 cm

- Readout → Per sensor
  - 10 signals
    - 2 synchro signals
    - 4 x 2 = 8 data links
  - Data throughput 160 MB/s (230 MB/s → already achieved = Ultimate Telescope DAQ)

➡ One FlexRIO board

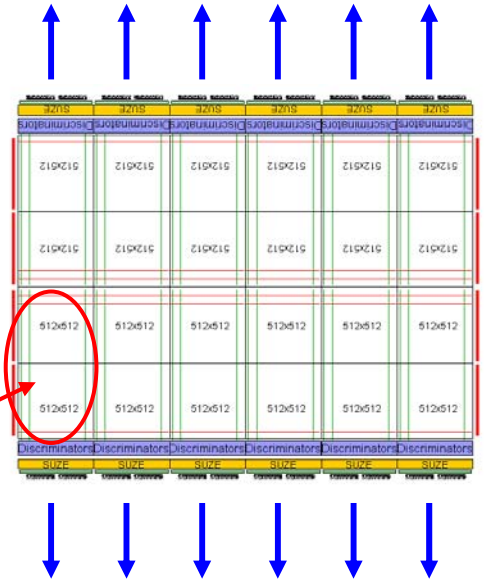
- Readout → SALAT = 3 sensors
  - 30 signals
  - 456 MB/s

➡ One crate with 2 FlexRIO → 320 MB/s

➡ One crate with 1 Flex RIO → 160 MB/s

DAQ constraints final sensor (worst case)

- 2014-2015 → Final sensor
  - Surface 6 cm x 4 cm – 3072 columns x 2048 rows
  - Readout ~ 200 µs
  - Data throughput evaluation → Scaling on
    - Mimosa 26 – 5 x 10^5 /hits/cm²/s → 109 MB/s
    - Ultimate – 1 x 10^6 hits/cm²/s → 268 MB/s
  - Worst case → one bloc → 268 / 12 = ~ 22 MB/s
    - → 12 Outputs @ 160 MHz (Ultimate 20 MB/s /output)



Final sensors → ~ 6 cm x 4 cm – 12 Outputs

- Readout → Per sensor
  - 14 signals – 160 MHz – 268 MB/s

➡ One FlexRIO board

- Readout → SALAT = 3 sensors
  - 38 signals
  - 804 MB/s

➡ One crate with 2 FlexRIO → 536 MB/s

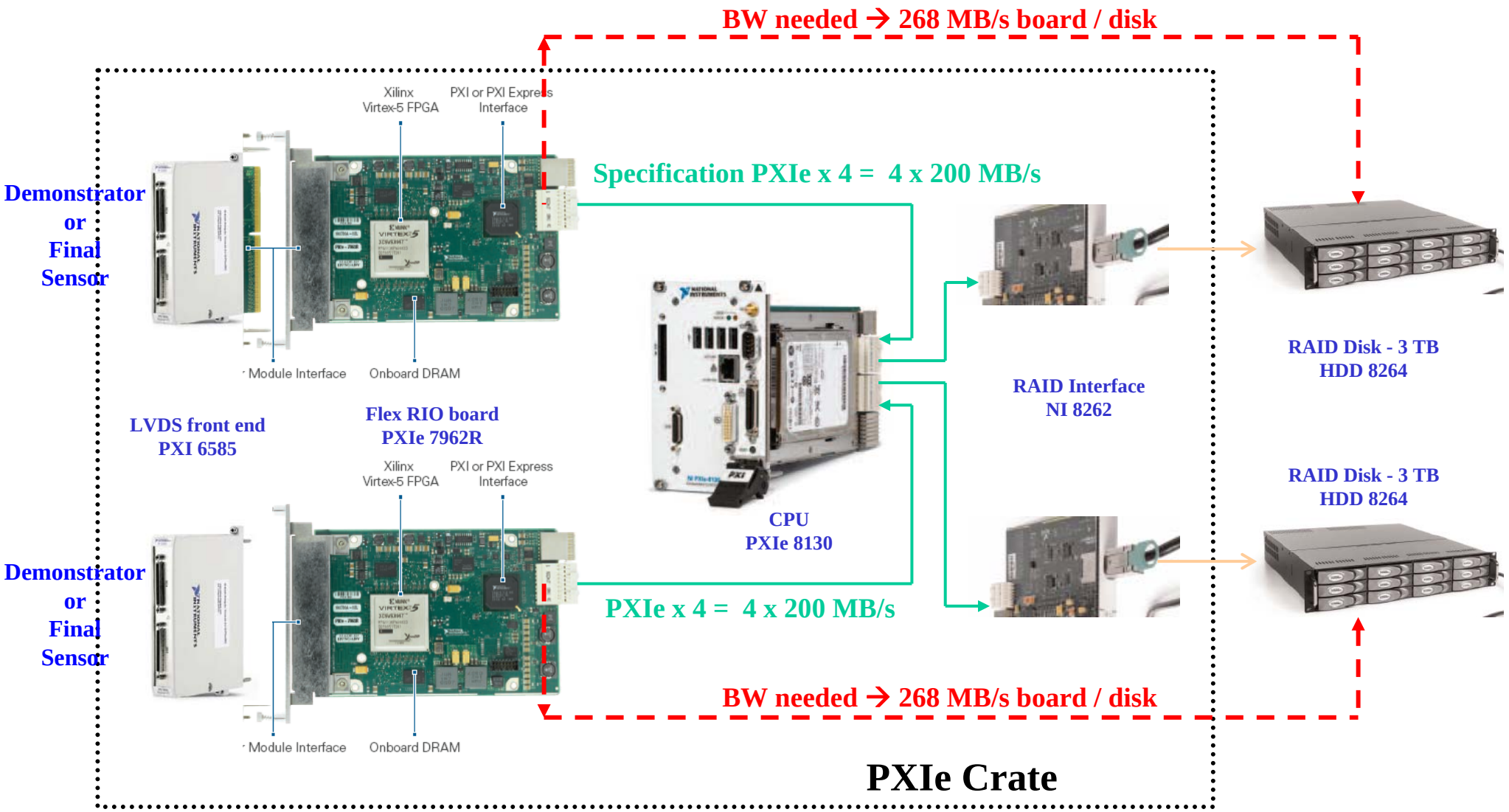
➡ One crate with 1 Flex RIO → 268 MB/s

DAQ constraints Demonstrator & Final sensor (worst case)

- DAQ constraints worst case
  - Per Flex RIO board → 12 links @ 160 MHz – 268 MB/s
  - Per crate → 2 x Flex RIO boards → 536 MB/s
- Performances already reached
  - 6 Planes Ultimate Telescope → 12 links @ 160 MHz – 6 x 40 MB/s
  - Single Flex RIO board - Single crate → 240 MB/s
- Two DAQ options
  - The goal → 3 Flex RIO board in 2 Crates
  - The backup (already achieved) → 3 Flex RIO boards in 3 Crates

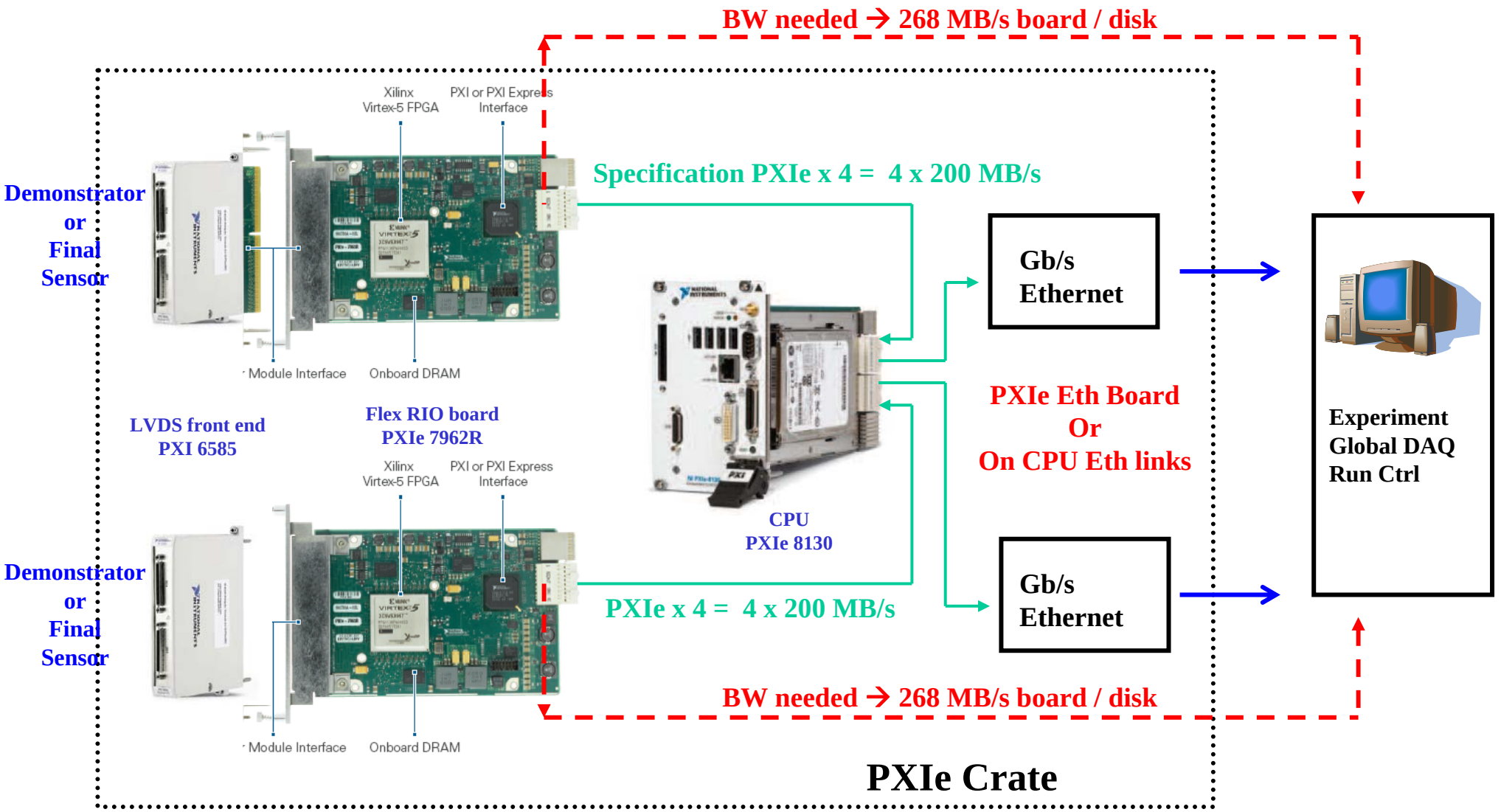
DAQ proposal for SALAT : The Implementation for Sensors testing

One Demonstrator or Final sensor / Flex RIO board – 2 Crates → Save data on disk



DAQ proposal for SALAT : The Implementation for Integration / Experiment DAQ

One Demonstrator or Final sensor / Flex RIO board – 2 Crates → Ethernet links



Data throughput on Ethernet link(s) from PXIe crate / Experiment Global DAQ

- Worst case → Data throughput based on Ultimate & 2 Crates option
  - Crate with 1 x Flex RIO → 268 MB/s → Use two Eth links of CPU board (2 x 1 Gb/s = 200 MB/s not so far)
  - Crate with 2 x Flex RIO → 536 MB/s → Need 10 Gb/s Eth board (No NI product now, may come later …)
    - Better to use three crates → 268 MB/s / crate
- Easiest case → Data throughput based on Mimosa 26 & 2 Crates option
  - Crate with 1 x Flex RIO → 87 MB/s → One CPU Eh link
  - Crate with 2 x Flex RIO → 174 MB/s → Two CPU Eth links
- Conclusion
  - There is always one solution → Use three crates if needed
  - NI PXIe Ethernet boards 10 Gb/s should come soon or later
  - JTAG slow control (now done by SW + // Port) can be integrated in Flex RIO
    - Reduce configuration time → In case many MAPS are chained (MIMAIDA or MAPS ladders)

Conclusion / Planning

Current status & Next steps …

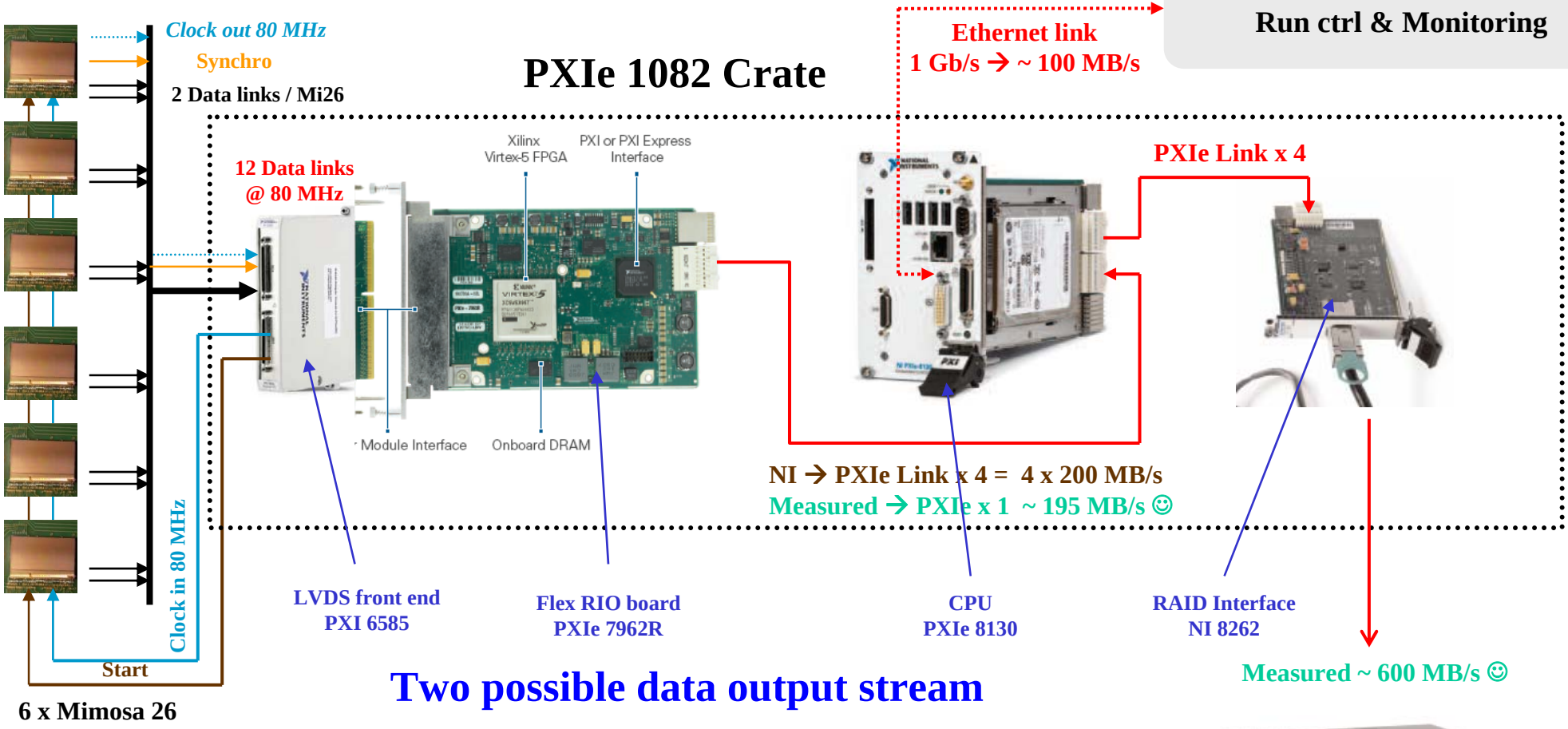
- SALAT Demonstrator & Final sensors DAQ
  - DAQ requirements are in the performances range of NI PXIe Flex RIO architecture
  - Three Flex RIO boards are needed
  - The adjustment variable is the crates number → 2 or 3 ?

- Planning
  - December 2011 – January 2012 → System load evaluation → To define crates number
  - February / March 2012 → DAQ system ready for Demonstrator sensor tests at lab
  - ~ June 2012 → DAQ system ready for Demonstrator sensor beam test (standalone DAQ)
  - ~ November 2012 → Off-line interface with (Priority → Both can't be achieved for november)
    - SABT (Second Arm Beam Telescope) DAQ
    - AID Box
  - 2013
    - DAQ package setup – DAQ training to collaborators (DESY)
    - FW & SW upgrade for Final sensor

Backup slides

EUDET Telescope DAQ : System architecture

DAQ → 1 Flex RIO + 1 CPU + 1 RAID



Two possible data output stream

- " Weak beam intensity " → Data stream << 120 MB/s → Ethernet
- " Strong beam intensity " → Data stream ~ 120 MB/s → RAID

RAID Disk - 3 TB
HDD 8264

More about DAQ → http://www.eudet.org/e26/e28/Eudet-Memo-2010-25, 26, 27, 28 & Slide 40

Specifications …

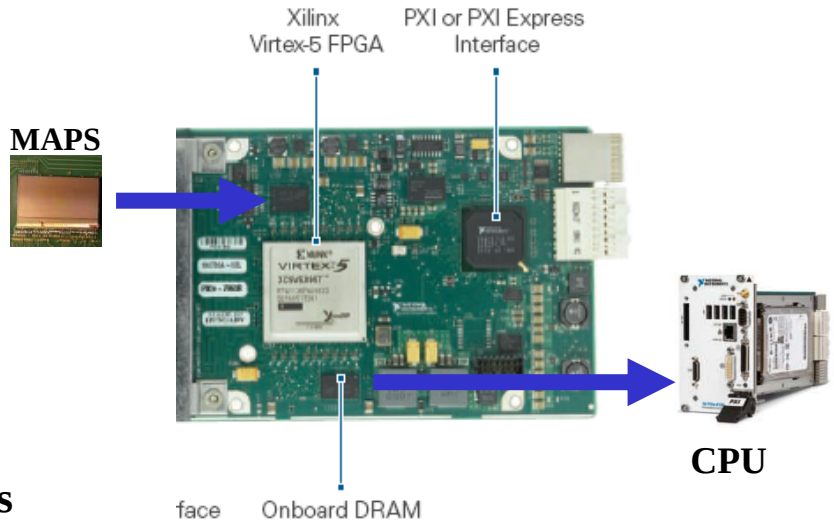
DAQ specifications for EUDET Telescope DAQ

- 0 % dead time → What about PXIe bus & SW latency ?
- Minimize FW development time

Pragmatic approach …

Pragmatic approach → No time to study in details …

- Latency → Bufferize on board
  - Flex RIO has two DRAM
  - MAPS fills one DRAM / CPU reads the other
  - Filling 207 ms / Reading 84 ms
    - → 123 ms margin / 207 ms = 60 % free time
- FW development time → SW development time
  - Keep FW as simple as possible → Simple HW tasks
  - Move processing to SW → Use PXIe BW & CPU Power

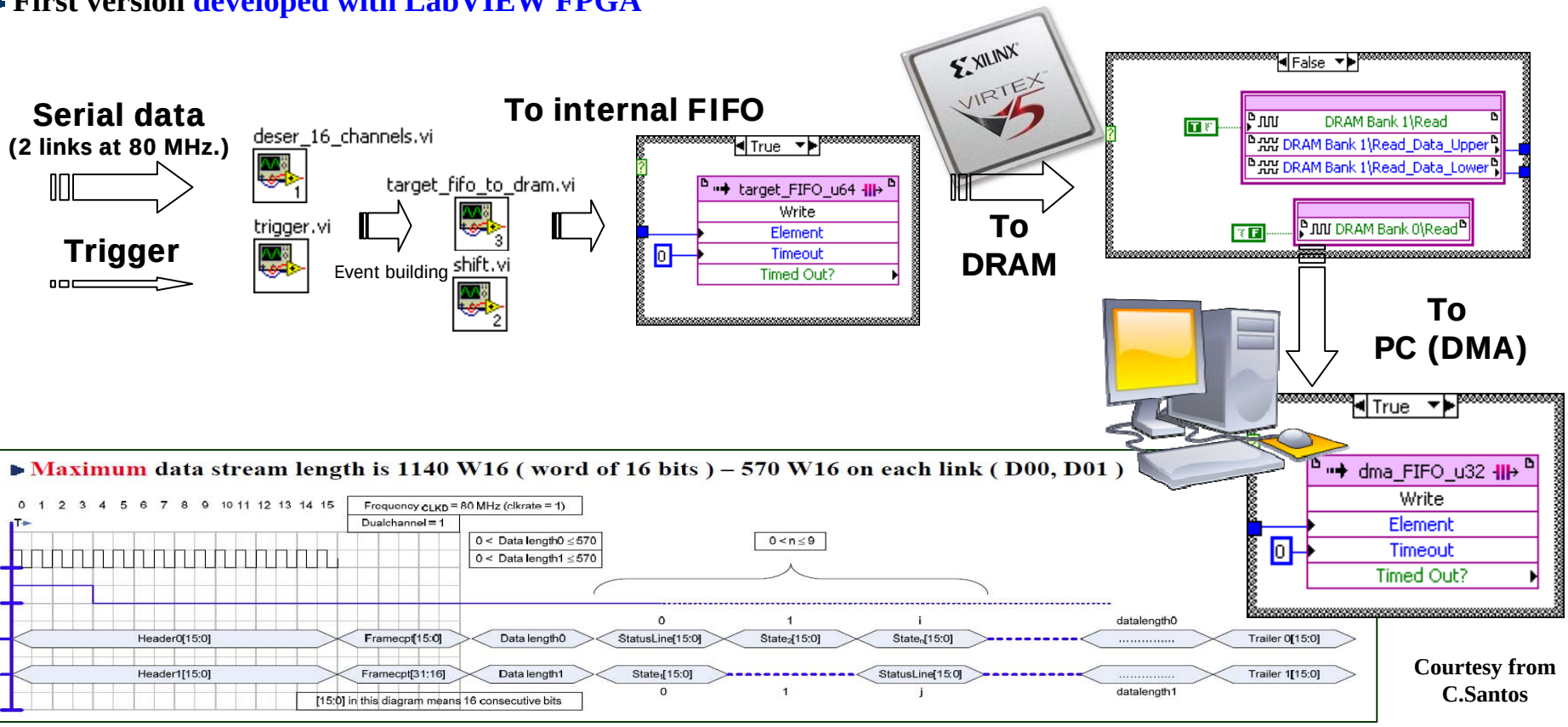


Firmware & Software developed at laboratory by us

- Data deserialization (16 Mimosa 26 read in parallel)
- Swap between the two DRAM banks (To reduce dead time risk)
  - Mimosa 26 fill one DRAM / The second DRAM is read by SW via PXIe bus
- Trigger handling → Store trigger information from PMT
- First version developed with LabVIEW FPGA

C. Santos

G. Claus

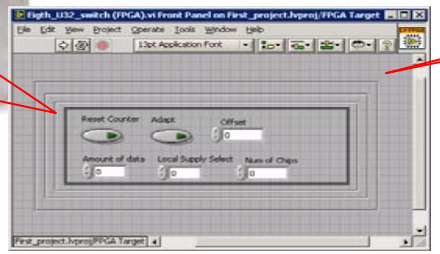


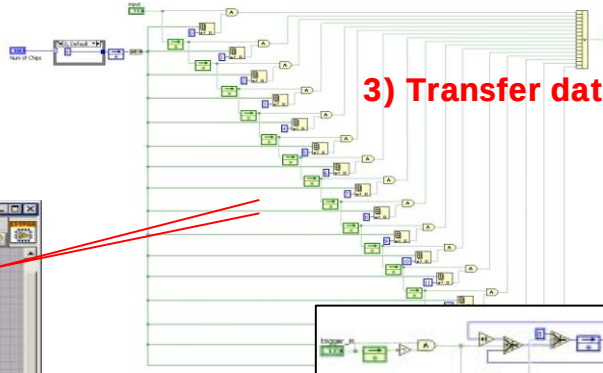
Courtesy from C.Santos

EUDET Telescope DAQ : Detailed view of firmware …

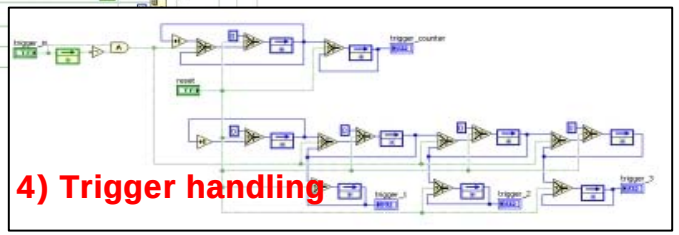
deser_16_channels.vi

FPGA vi



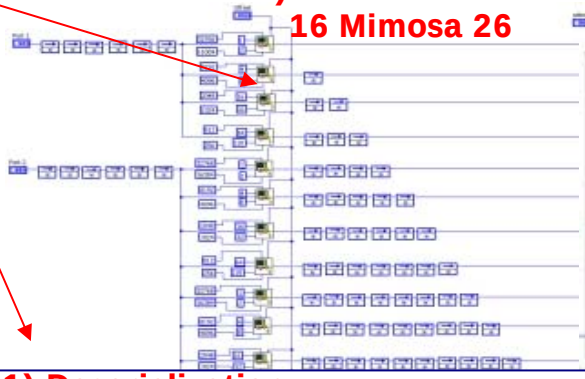


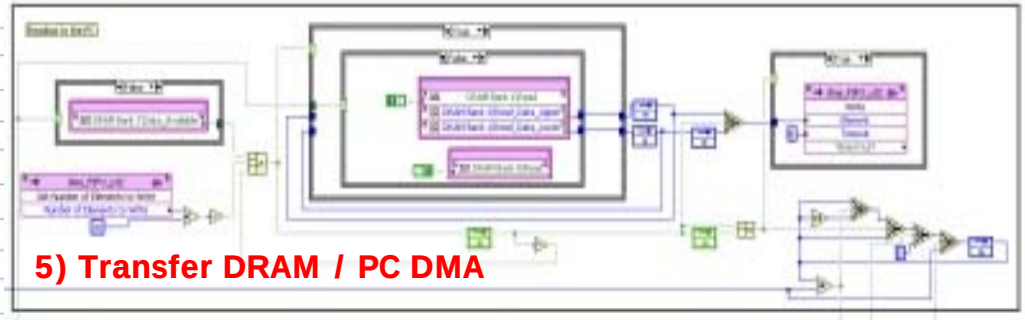
3) Transfer data / on board DRAM



4) Trigger handling

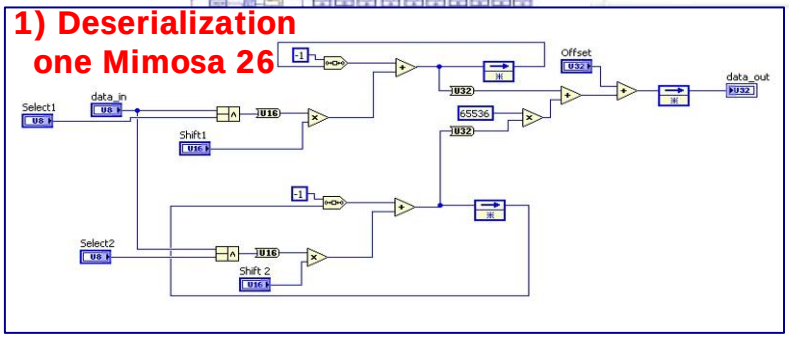
2) Deserialization
16 Mimosa 26





5) Transfer DRAM / PC DMA

1) Deserialization
one Mimosa 26



FW development done by Cayetano Santos
cayetano.santos@iphc.cnrs.fr

EUDET Telescope DAQ : Status

- Flex RIO fulfilled project requirements with safety margin
  - No dead time → 60 % free time – FPGA filled at ~ 30 %
  - System upgrade → SW upgrade (easy) / FW should not change
  - HW Evaluation + Development → ~ 9 men-month (2 Engineers)

- Development & DAQ deployment
  - Development done by IPHC - Transfer to EUDET done (one week training December 2010)
  - Deployment & interface / EUDET DAQ done by EUDET collaborators
    - Integration of one Telescope DAQ is running – One more foreseen …

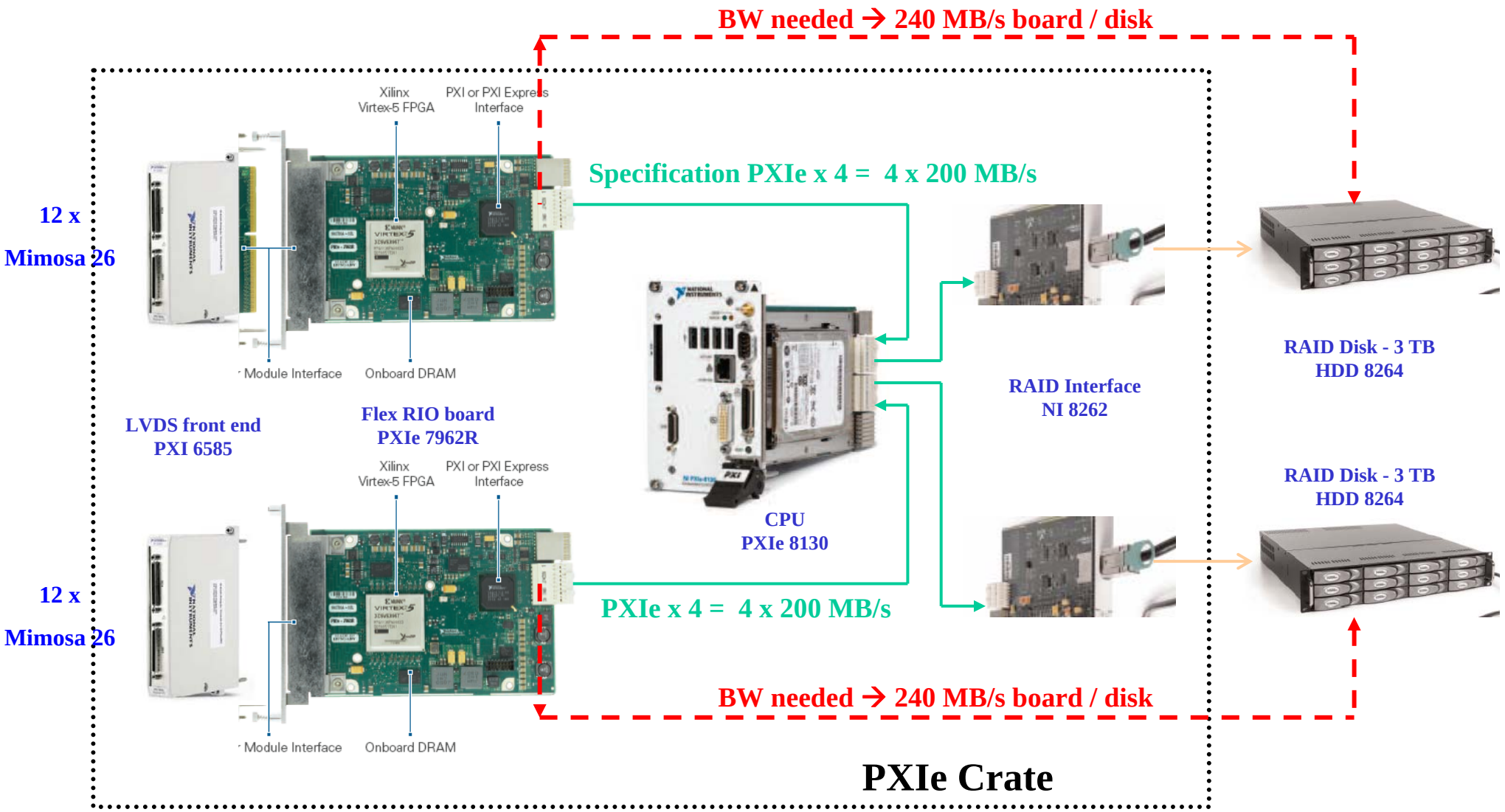
- Flex RIO foreseen for AIDA project
  - Readout of 72 x Mimosa 26
  - Data rate = 72 x 20 = 1440 MB/s
  - 10 X EUDET Beam Telescope data rate

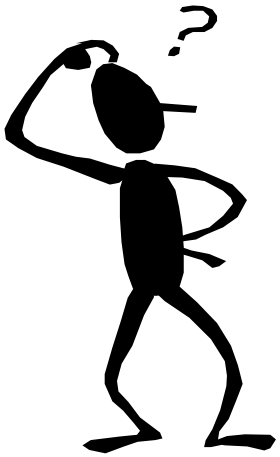
AIDA → European Union project (FP7) 2011-2014
80 Institutes - 23 countries
Advanced European Infrastructures for Detectors at Accelerators
9 Work Packages
→ *WP9 Advanced Infrastructures for Detectors R&D*
→ *Task9.3 Precision Pixel Detector Infrastructures*

Web → **aida.web.cern.ch/aida/index.html**

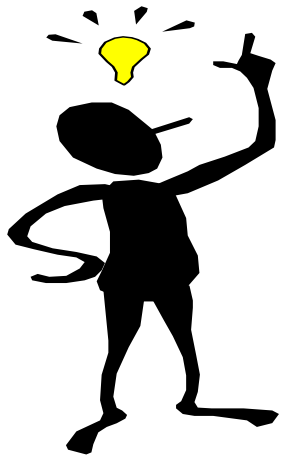
AIDA project DAQ (2012) : Scalability of Flex RIO architecture ☺

AIDA 72 Sensors → 12 Mimosa 26 / board – 2 boards / crate → 3 Crates



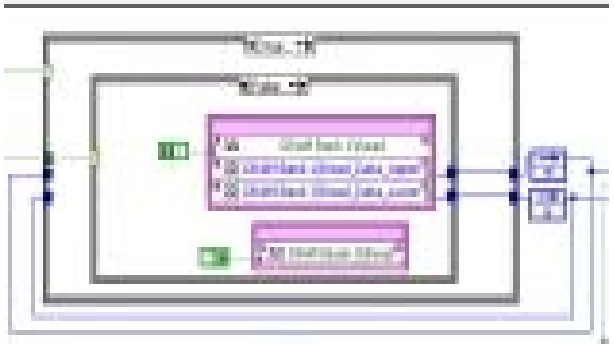


What have we learnt on Flex RIO projects ?



Firmware language : LabVIEW FPGA or VHDL ?

- Validate Flex RIO HW / Project specifications
  - Evaluate blocks performances → Desererializer, DRAM, DMA
  - LabVIEW FPGA perfect for test benches (based on NI examples)
  - LabVIEW FPGA used for the " proof of principle " DAQ FW



- Implement more complex processing (Trigger handling, TLU, …)
  - Processing code written in VHDL (→ Need FW Engineer)
  - "Glue code" written in LabVIEW FPGA
    - Gives a global / top view of system architecture
    - Allows non FW expert to modify system
      - Configure / disable parts, perform tests …

```
architecture rtl of DemoClipAdder is
  signal data_tmp : unsigned(63 downto 0)

begin

  process(clk, aReset, reset)
  begin
    if (aReset = '1' or reset = '0') then
      data_tmp <= unsigned(reset_to);
    elsif (clk'event and clk = '1') then
        if (enable = '1') then
          data_tmp <= data_tmp + 1;
      end if;
    end if;
  end process;

  data <= std_logic_vector(data_tmp);

end rtl;
```

- Conclusion
  - LabVIEW FPGA & VHDL are two complementary tools
  - LabVIEW FPGA fits well with bottom-up approach → Tests, Iterations to reach goal

Who should process data : FW or SW ?

- Case study → EUDET Telescope DAQ
  - Deserialize data stream @ 80 MHz → FW
  - Detect & store triggers information @ 2,5 MHz → FW

  - Handle frame length (function of hits nb / frame) @ 10 KHz → SW
  - Handle frame format (header, data part, trailer …) @ 10 KHz → SW

- First step = Keep FW as simple as possible
  - PXIe bandwidth & CPU power allow to make part of processing by SW (C or LabVIEW)
  - It will be easier to develop and debug SW in C / FW → Less development time ☺
- Second step = Move SW processing to FW
  - Split the job in small tasks → Manageable by students …

Conclusion : COTS for MAPS DAQ Systems ?

- **Proof of principle done ☺ … until next MAPS data throughput upgrade …**
  - **Digital MAPS characterization → All DAQ in PICSEL group are based on NI COTS**
  - **Digital MAPS applications → EUDET Beam Telescope**

- **NI DAQ distribution for MAPS / Lab custom DAQ boards**
  - **Less manpower needed → No boards production & test**
  - **Allow to follow MAPS users request for DAQ systems …**
    - **Installed systems → IPNL Lyon, CEA Saclay, DESY Hambourg, … Bohn, Univ Colombia**
    - **Future systems → University of Bristol, Tel-Aviv, Lubiana, Copenhague … Brookhaven (BNL)**

- **Key ideas**
  - **Check each "fw piece" → Bottom-up approach**
  - **Find best trade-off between FW / SW → Keep FW as simple as possible**
  - **Focus development "Task force" To FW and SW – Reduce manpower on PCB design**