The PANDA HPS front-end system

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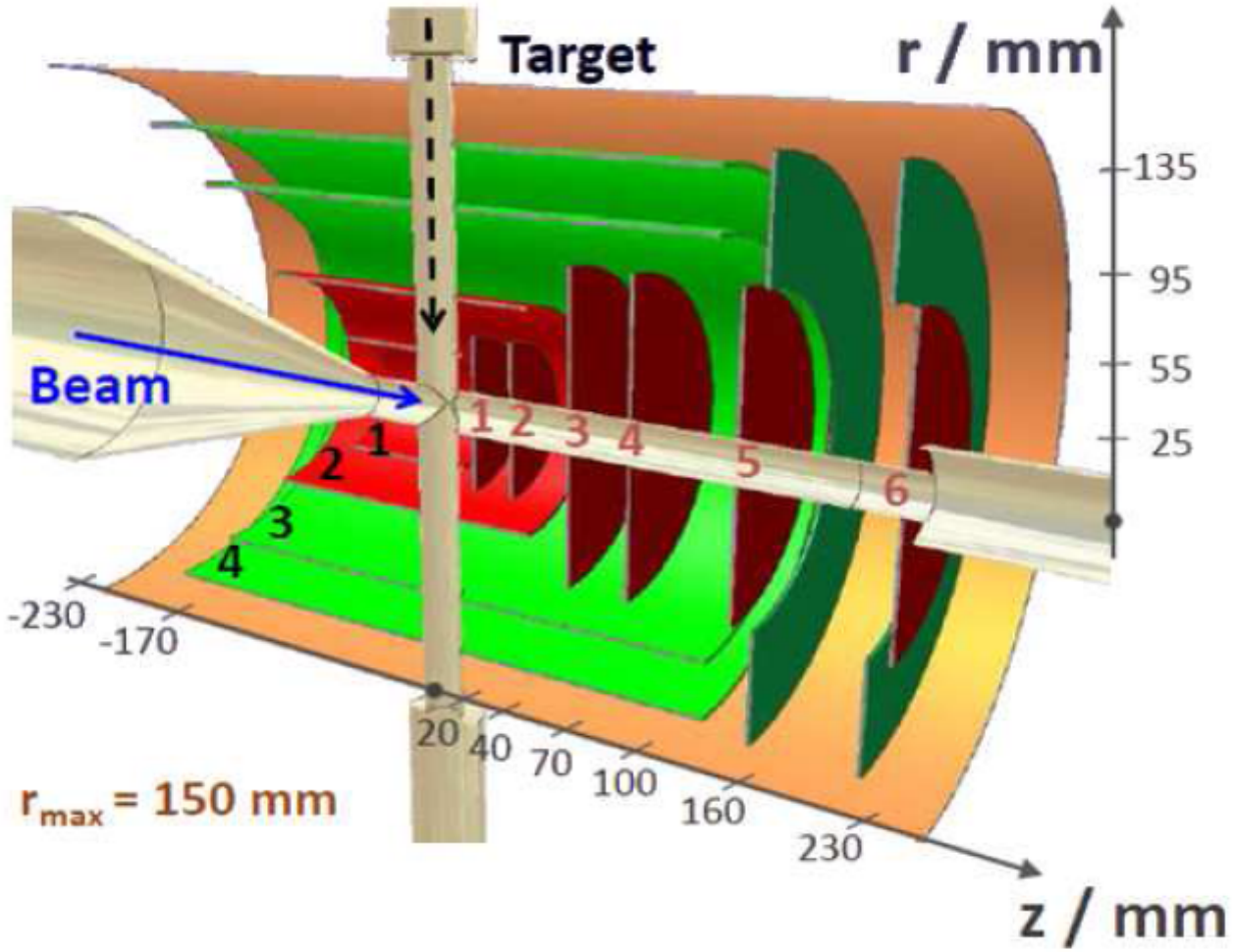
System overview



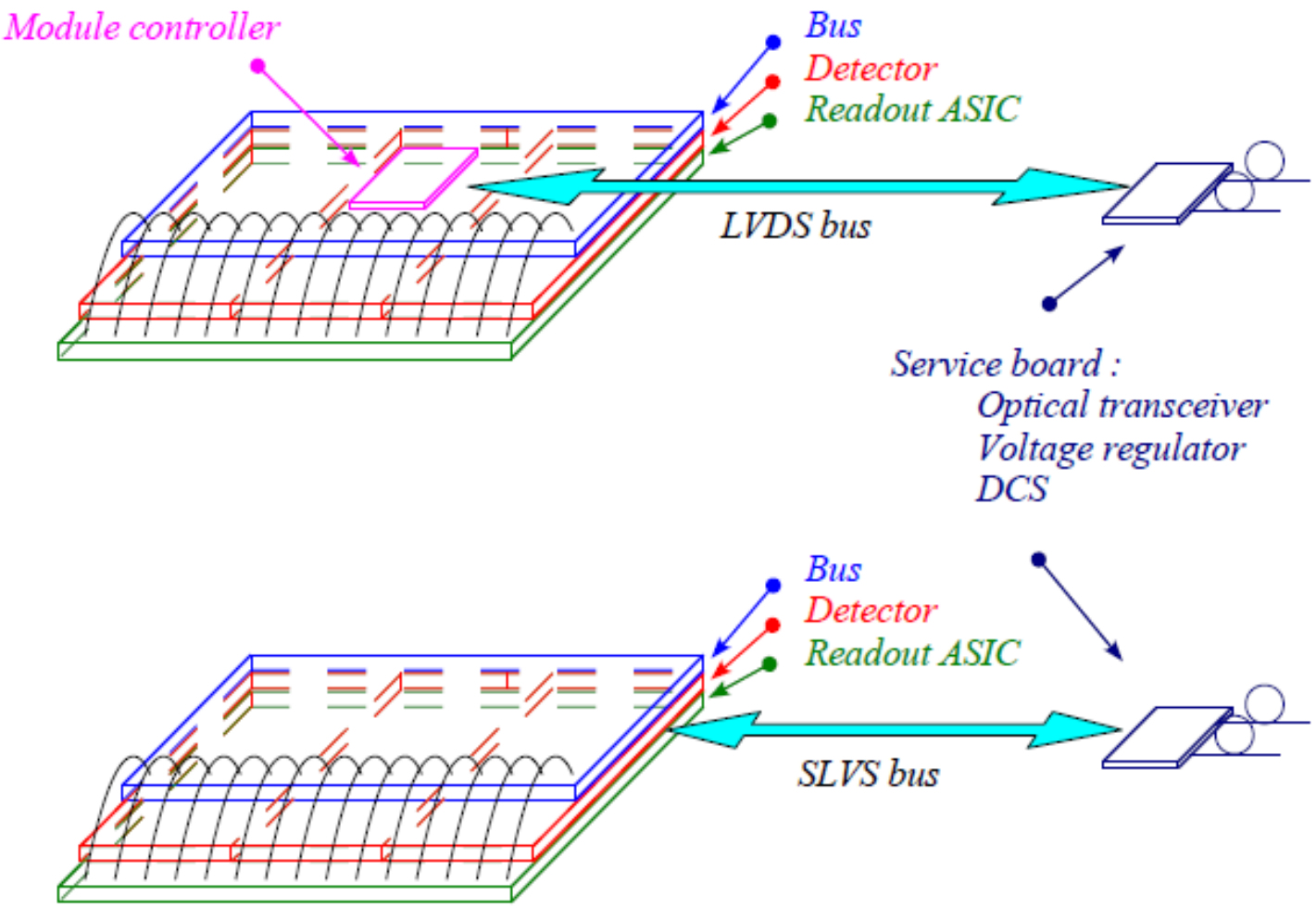
- Barrels: two layers of hybrid pixel sensors and two of strips.
- Disks: four equipped with hybrid pixels and two mixed disks.
- All layers have analog read-out for dE/dx.

System requirements

Pixel size	100 µm x 100 µm
Chip active area	11.4 mm x 11.6 mm
Noise floor	< 200 rms electron
Dynamic range	12 bits (ToT)
System clock	155.52 MHz
Time stamp resolution	6.25 ns
Power consumption	< 500 mW/cm2
Total ionizing dose	10 Mrad
1 MeV equivalent neutron	10E14

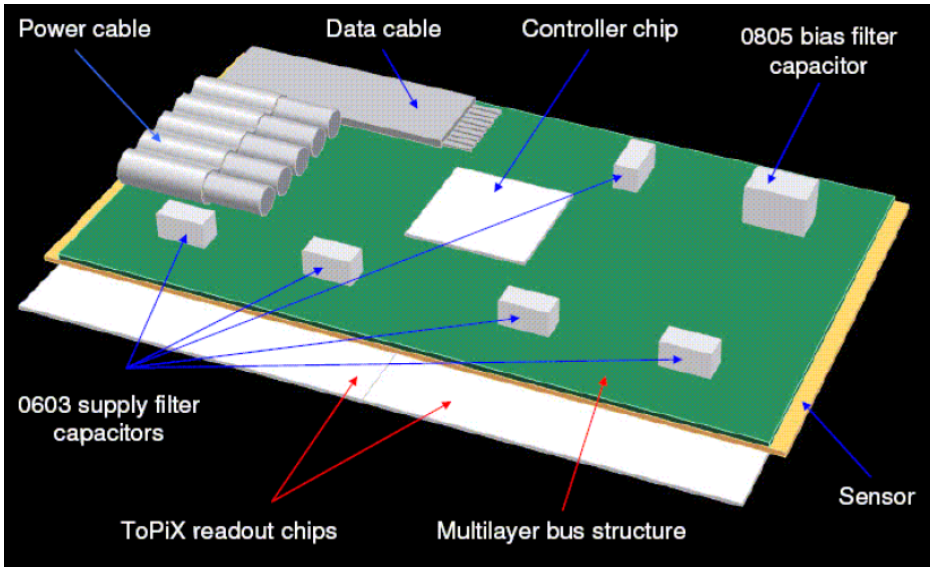
- Technology for the front-end ASIC: CMOS 0.13.
- Chip size chosen to minimize number of modules and optimize the coverage.
- Baseline sensor choise: p-type epitaxial.
- Front-end design to cope with sensor of either polarity.
- Data rate per chip O(300 Mb/s)

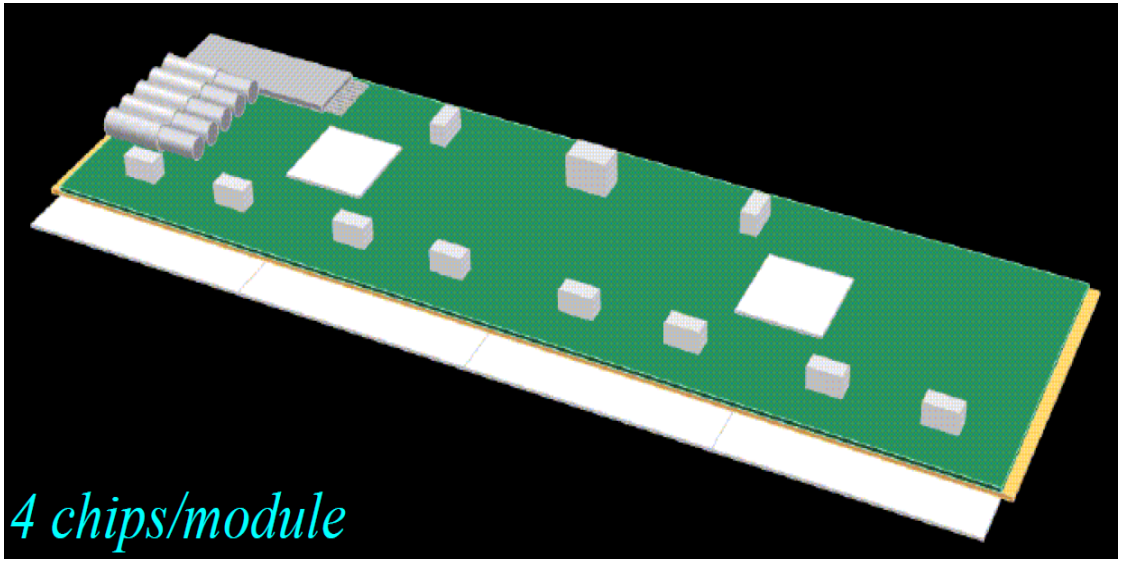
Module concepts under consideration

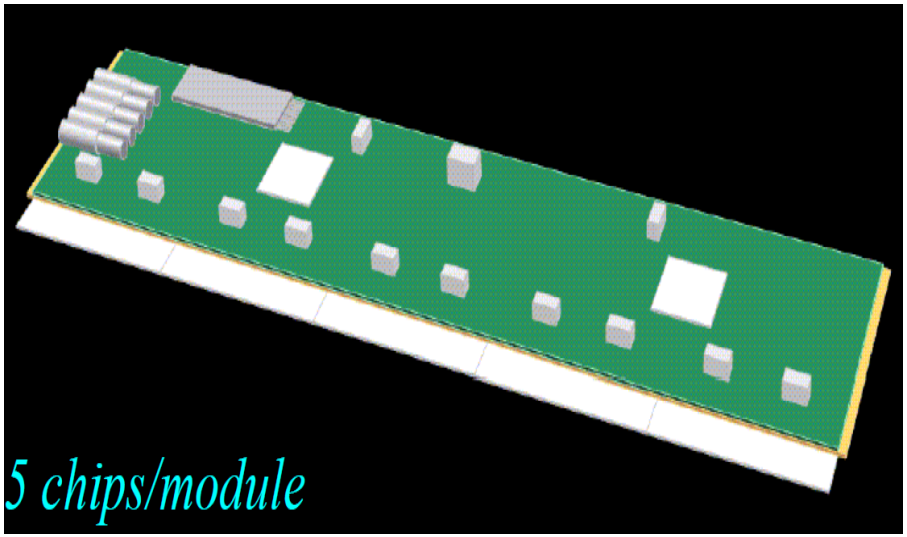


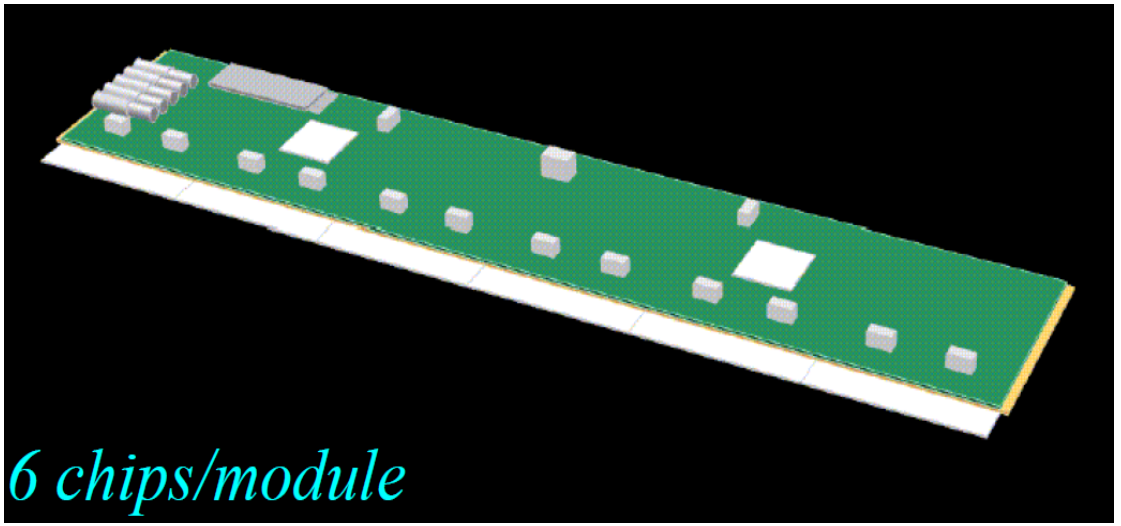
- With option 1 less cables.
- Option 2 eliminates a single point failure and the need of developing an extra chip.

Module designs

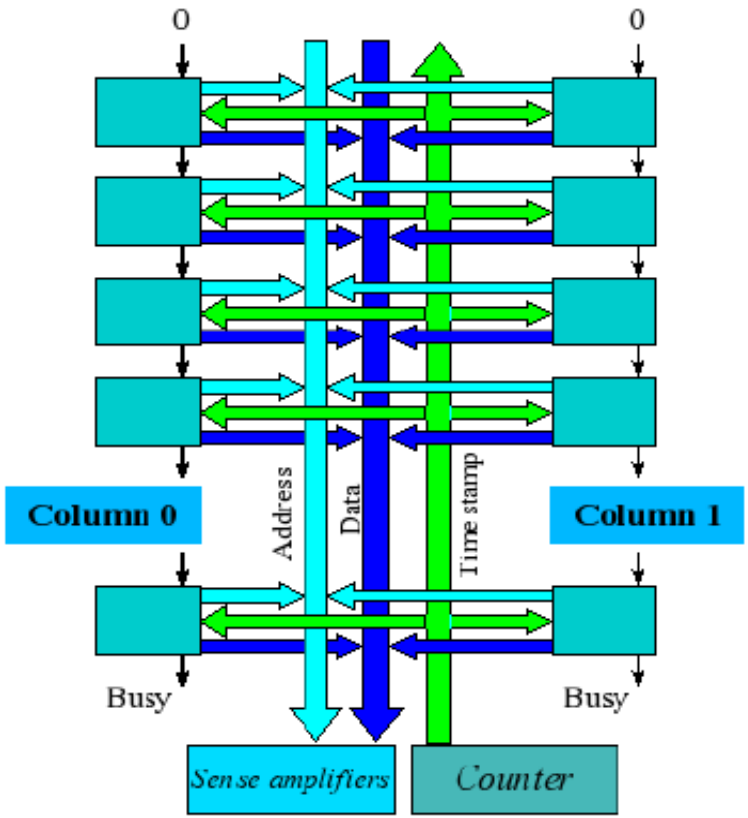








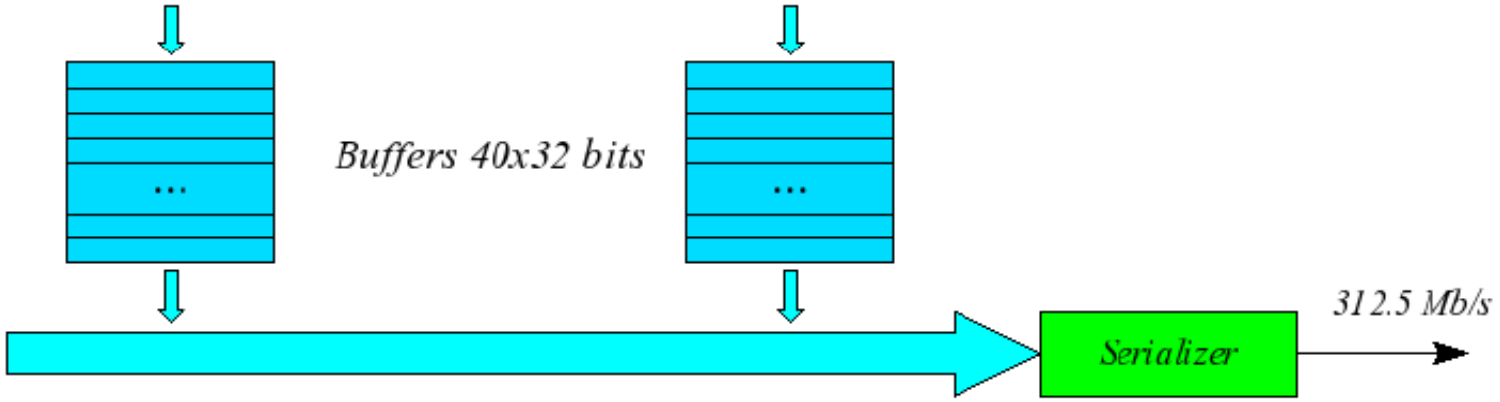
ASIC architecture



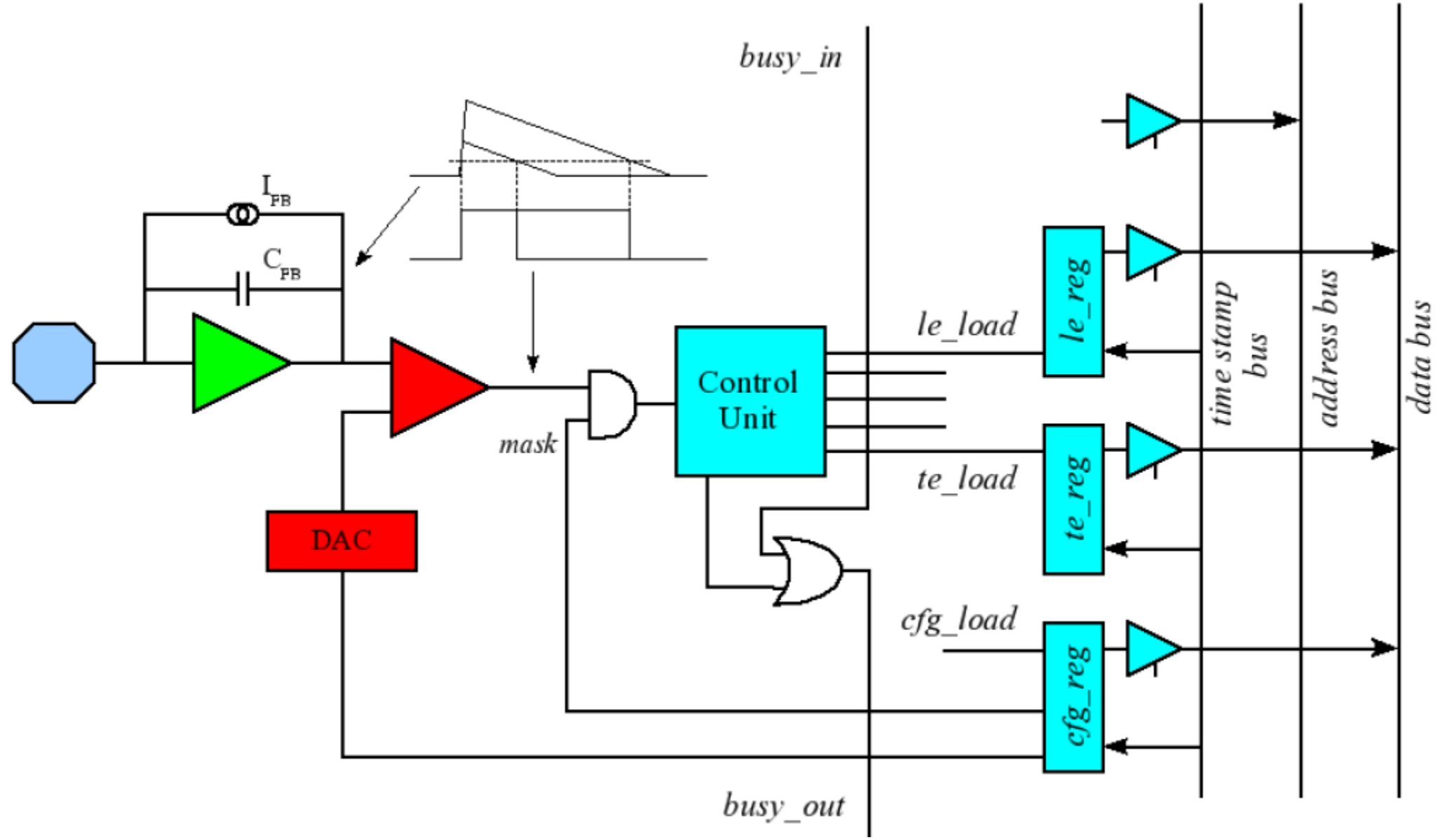
Double column structure
Common time reference
Readout data :
- Address
- Leading edge time
- Trailing edge time

End of column buffering
Serial data out

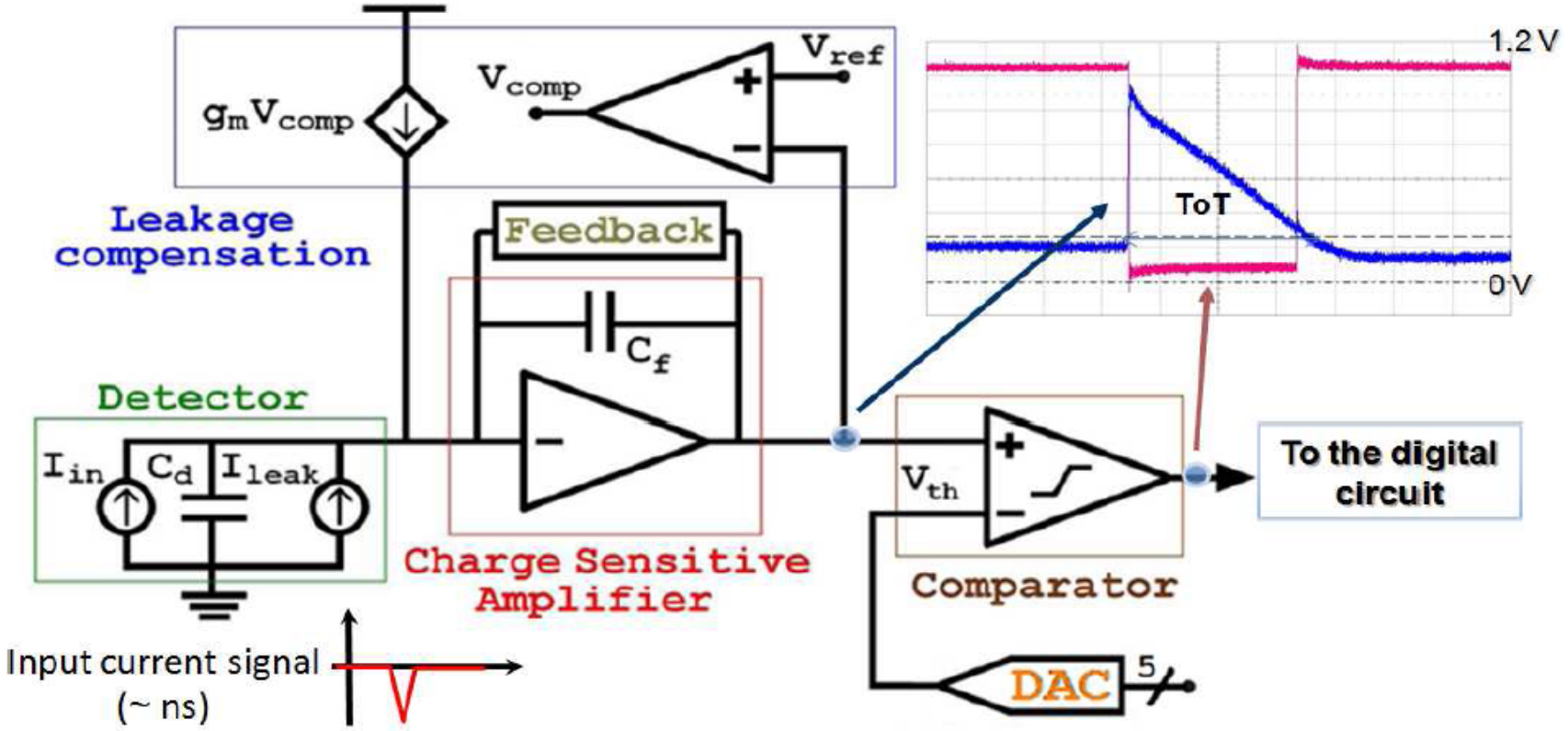
- Triple redundancy protection on the digital logic.



Pixel cell architecture

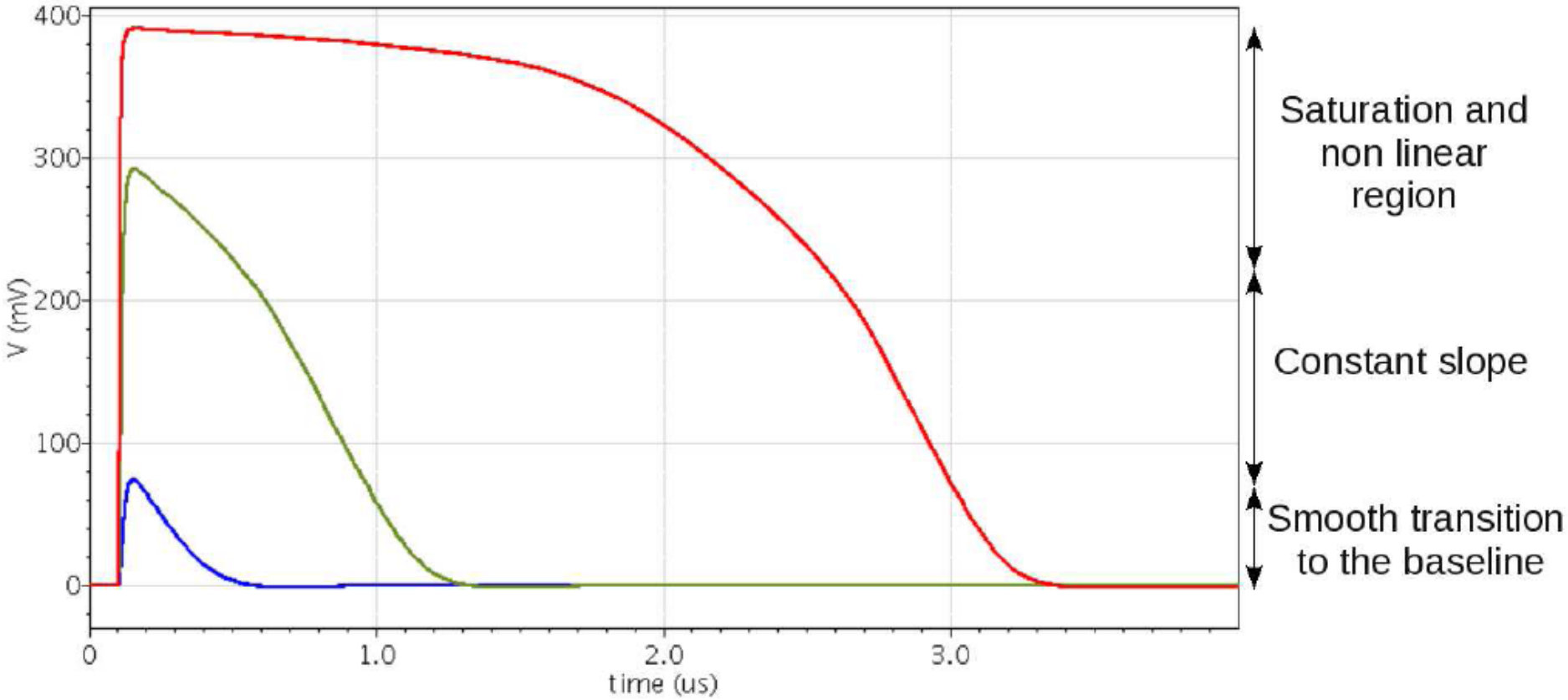


Some design challenges



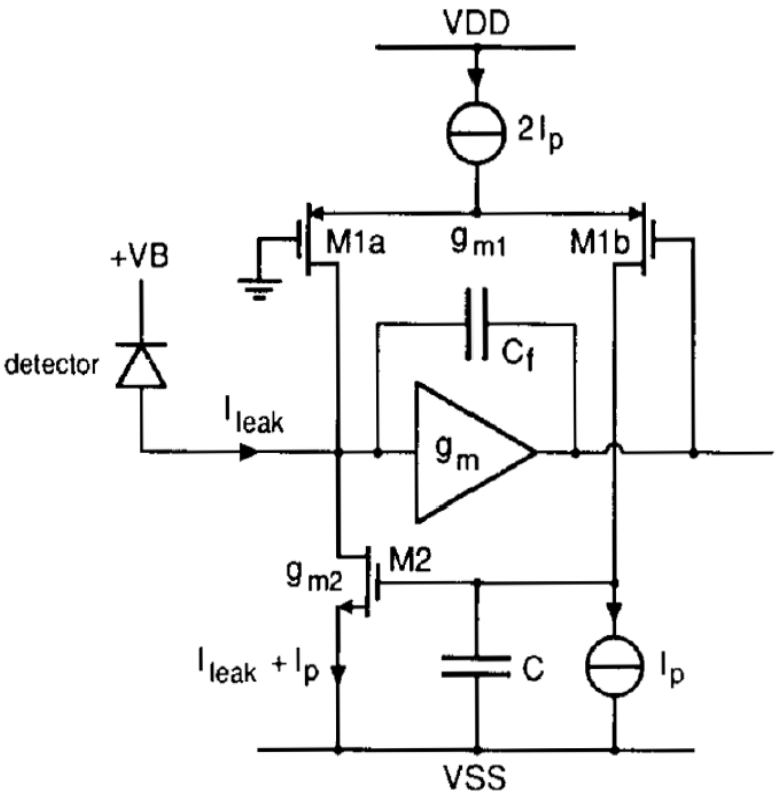
- Relatively compact cell (in comparison to functionality required)
- Design of the leakage compensation scheme has to cope with very long integration times (up to 15 us).
- Front-end design to cope with sensor of either polarity.

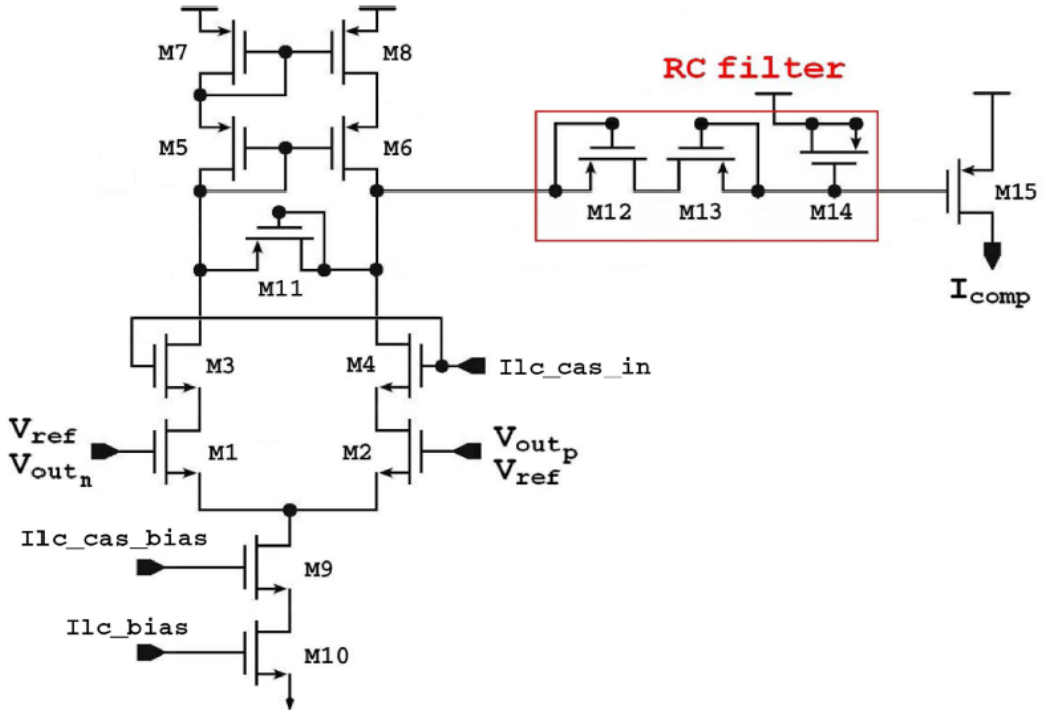
Time over Threshold with large inputs



- Due to the limited power supply, the linear dynamic range at the preamp output is limited.
- The constant current discharge extends the linear dynamic range well beyond the preamplifier saturation.
- Integration time depends on the applied signal.

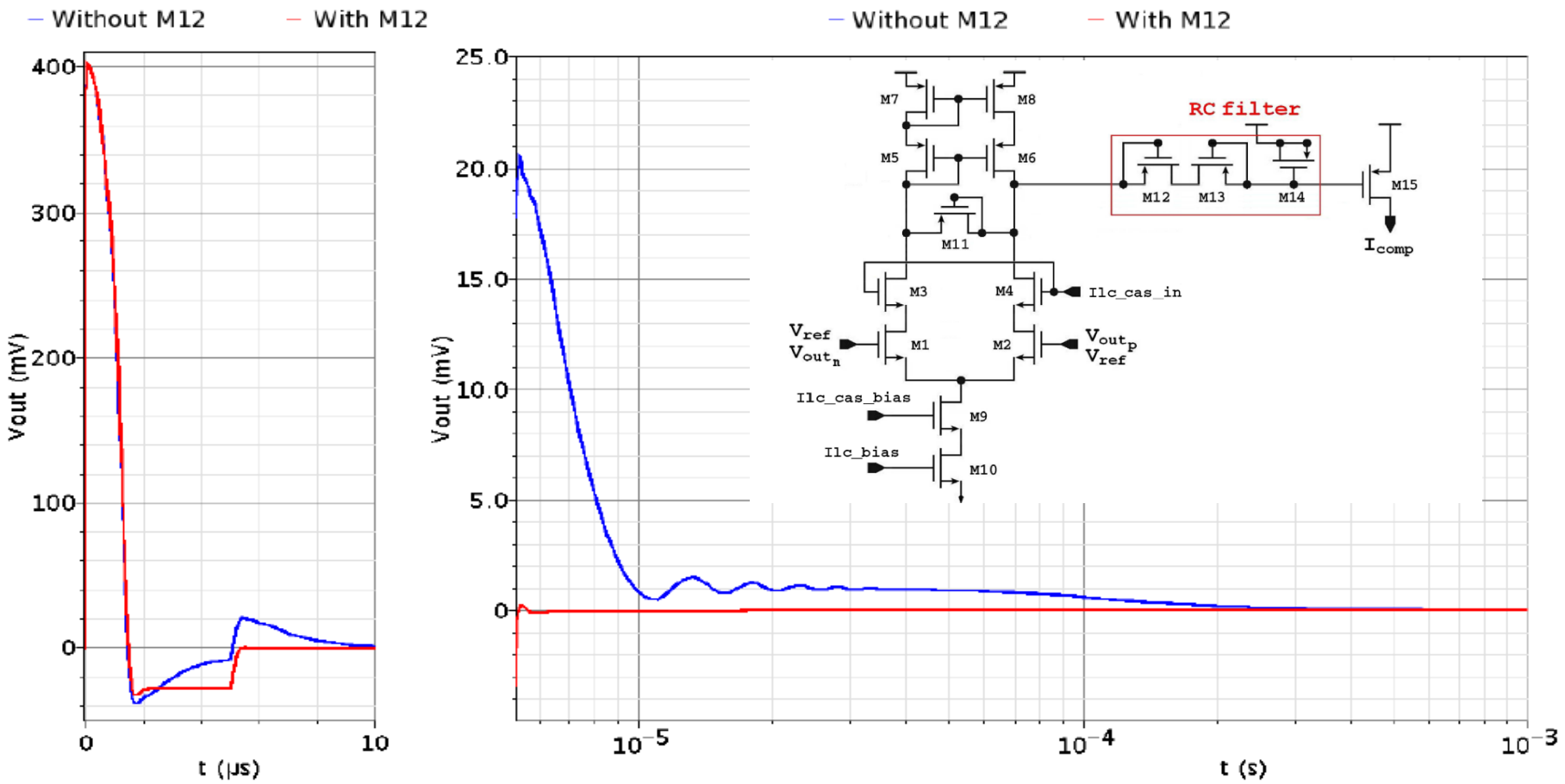
Leakage compensation scheme





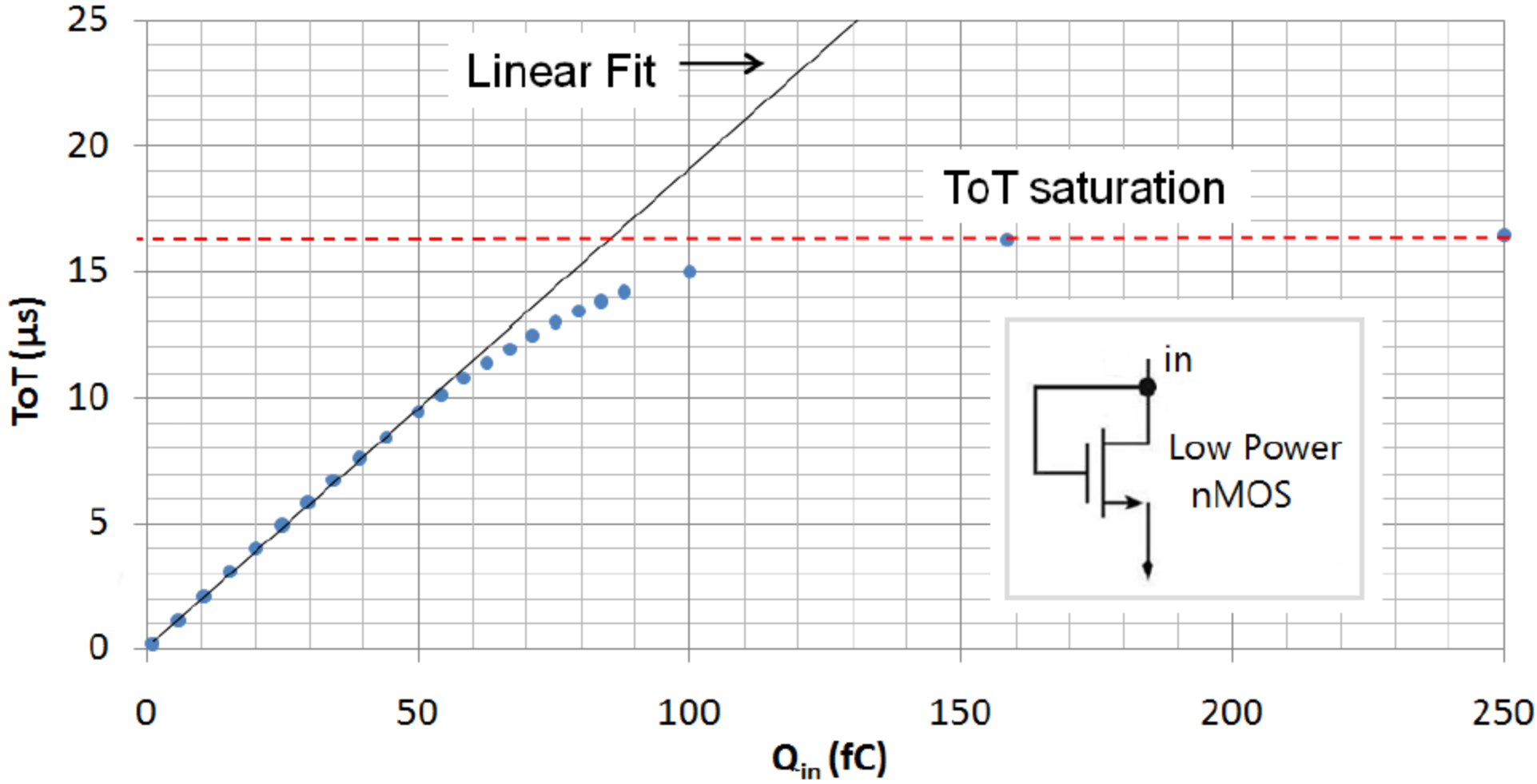
- Very long integration times challenge the leakage compensation scheme.
- Classical Kummenacker topology (left) requires too big capacitors
- Modified scheme implemented in a very compact area taking advantage of the characteristics of the 0.13 um process.

Baseline restoration performance



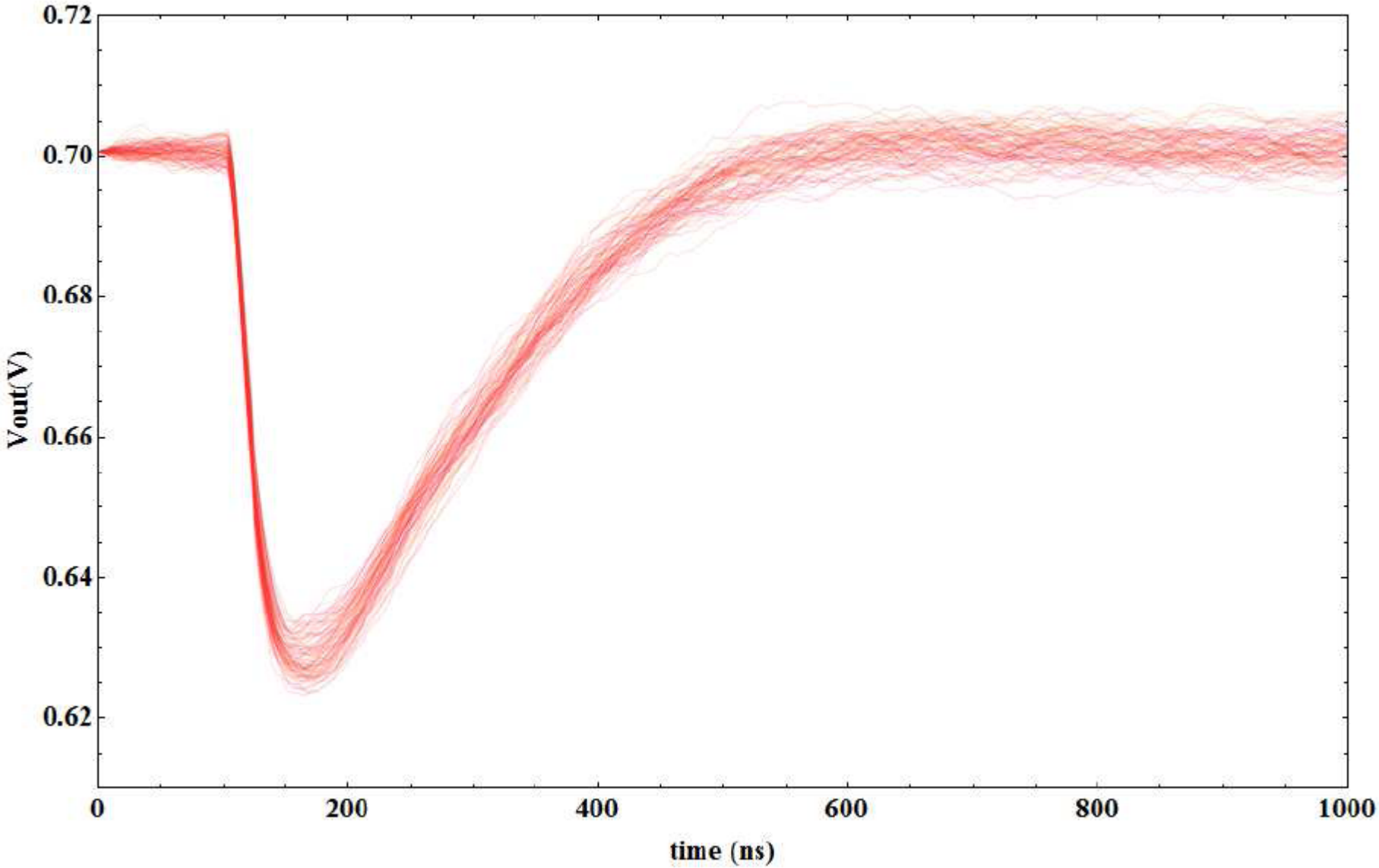
- Use of double diodes improves return to baseline with signal of “wrong polarity” (i.e. opposite to the one expected from the detector)
- Relevant for testing with calibration capacitor
- Important also for cross-talk events.

Overdrive protection



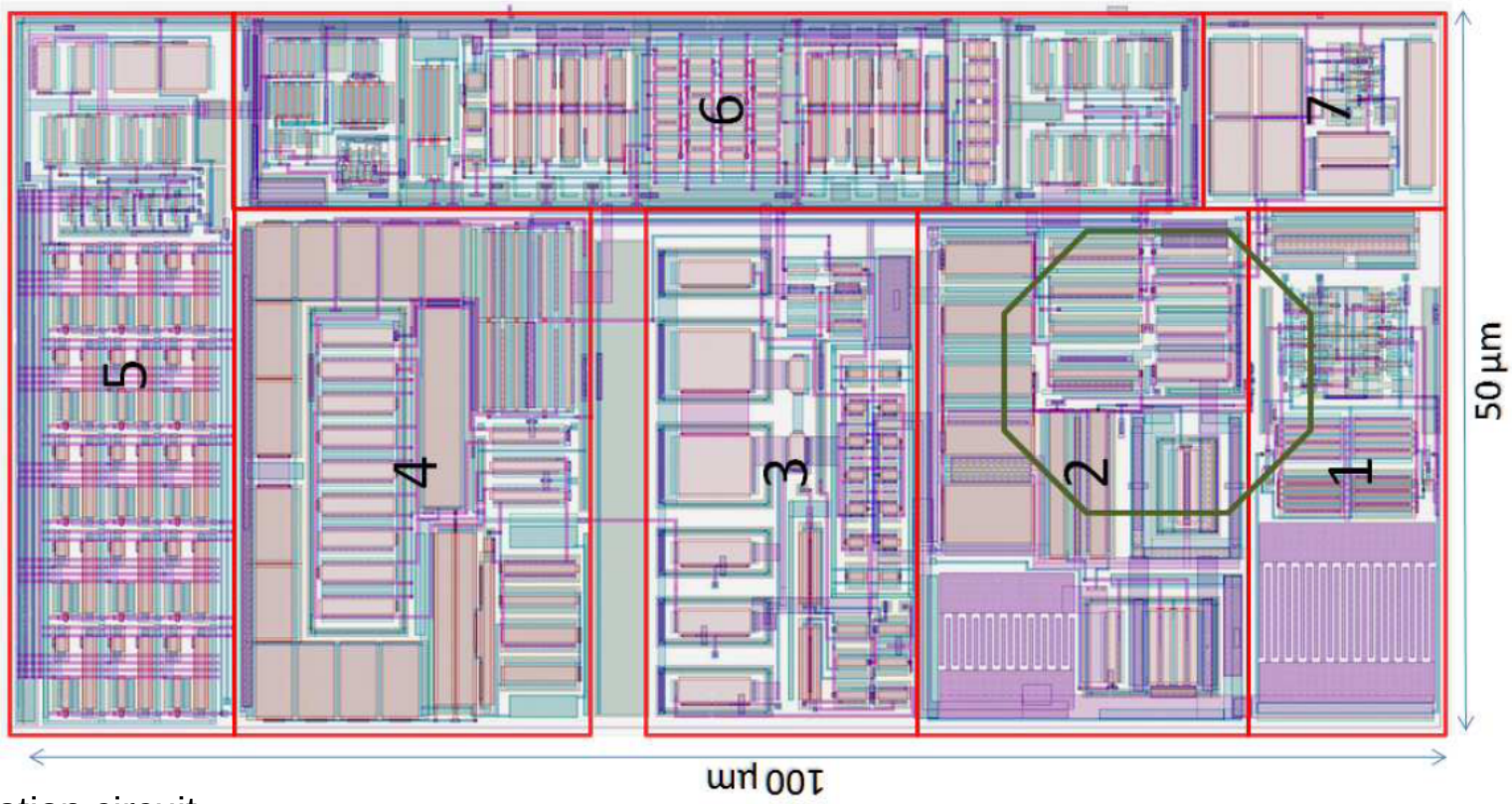
- To prevent very long dead-time from anomalous events a clipping circuit is introduced
- Charge measure linear up to 50 fC.

Expected noise performance



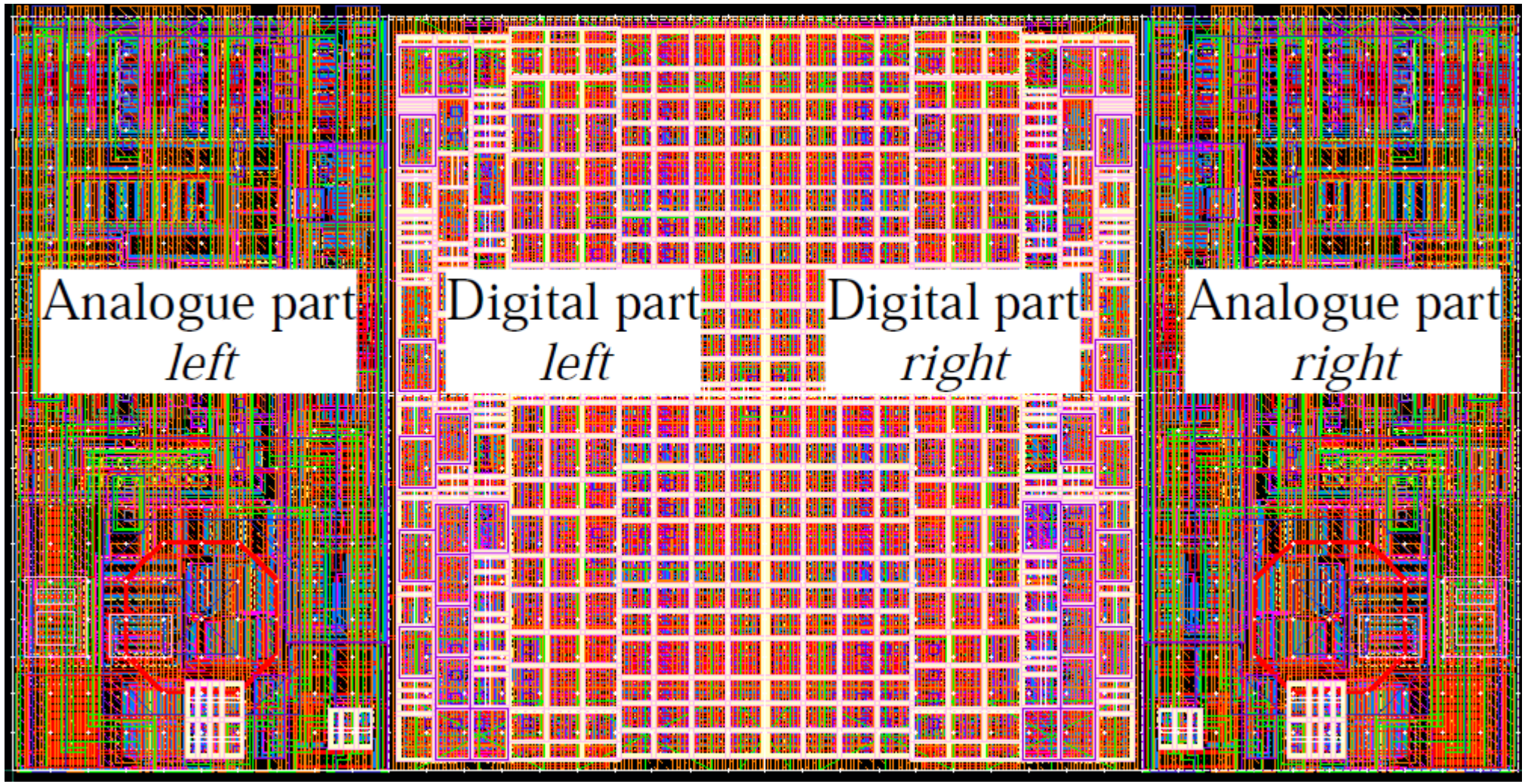
- Example of simulated noise performance.

Analog cell layout



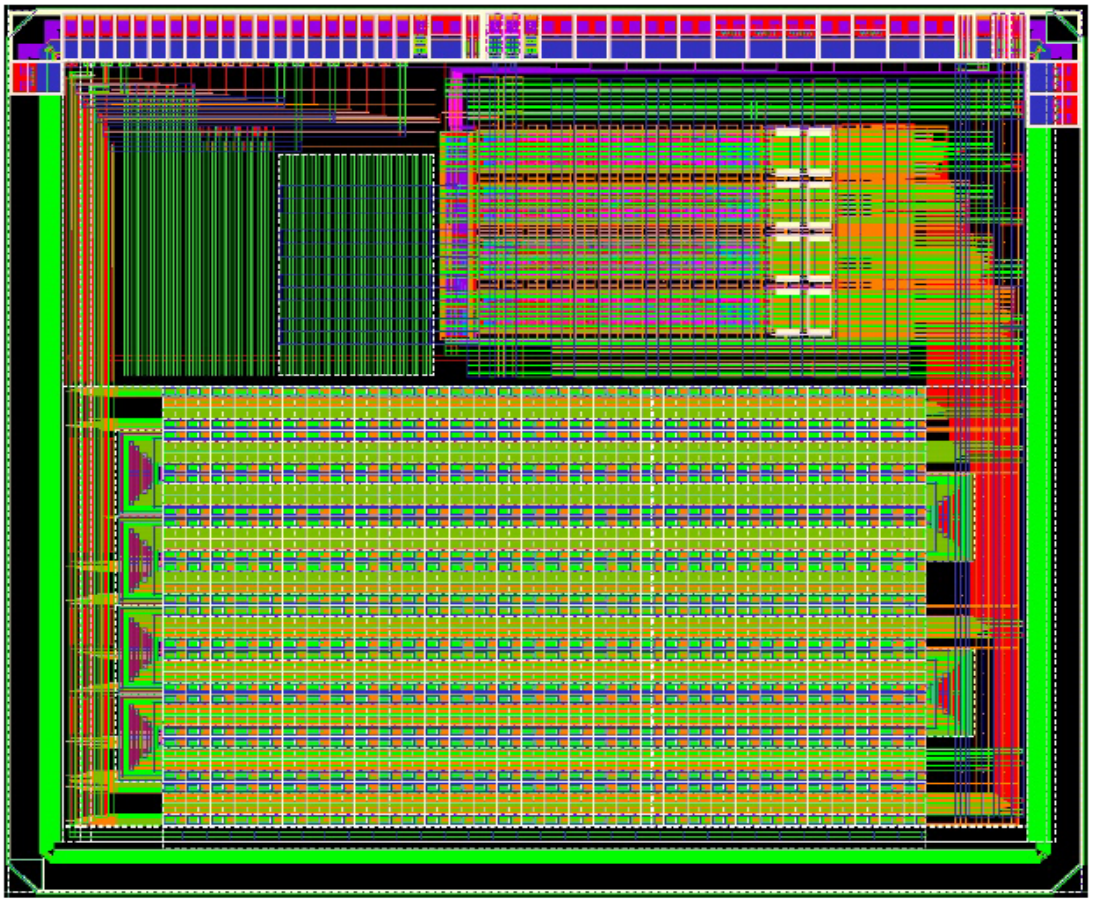
- 1. Calibration circuit
- 2. CSA
- 3. Contant current feed-back
- 4. Baseline holder
- 5. DAC
- 6. Comparator
- 7. Clipping circuit

Double pixel layout

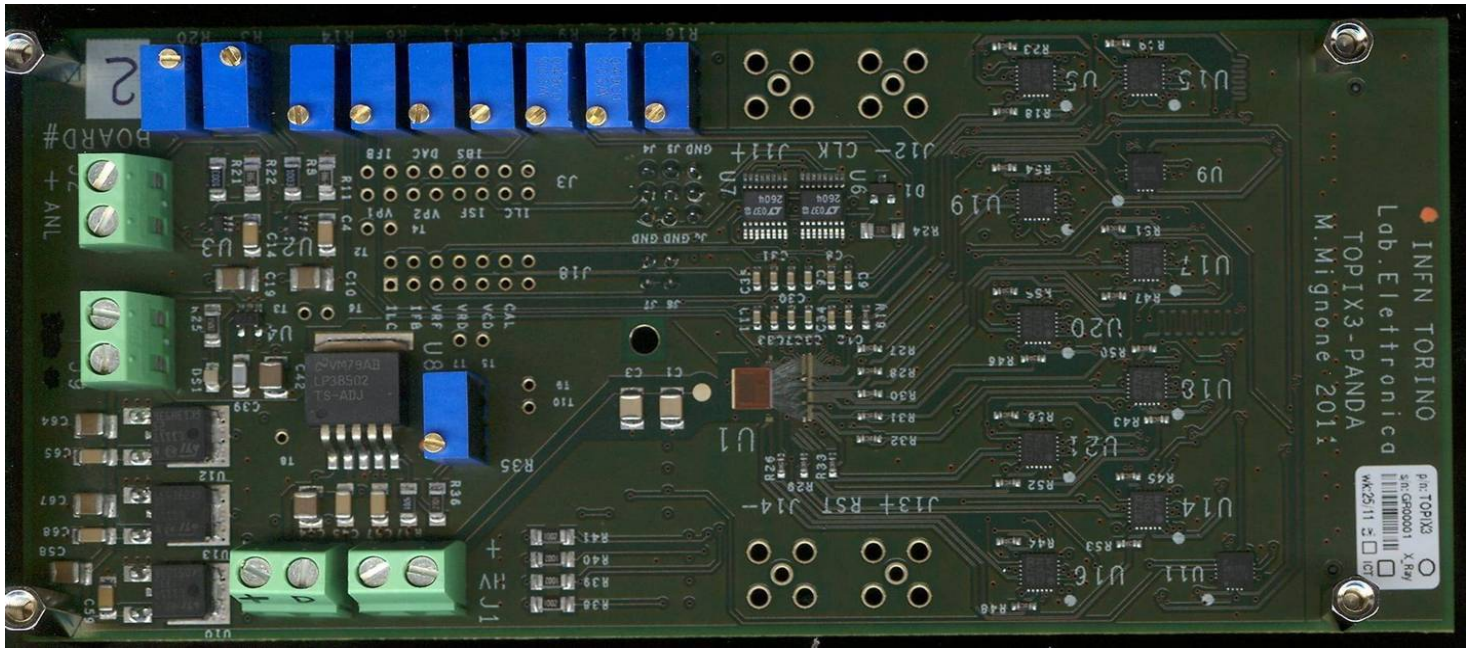


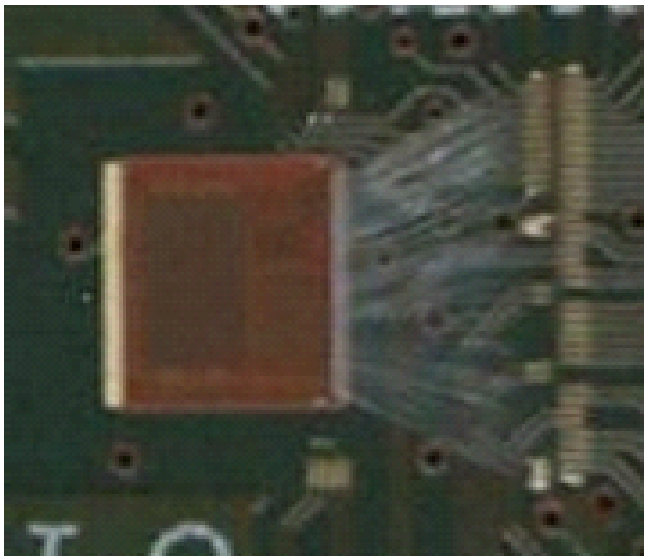
Prototyping phases

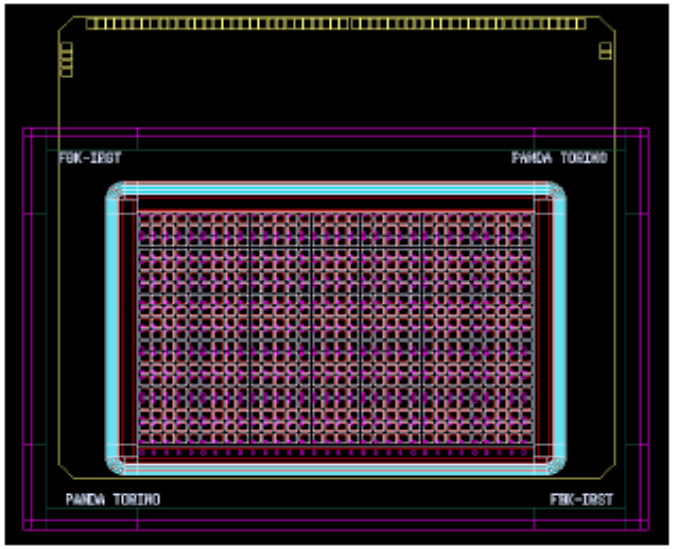
- First prototype with 32 pixels: only the analog part to understand the technology and relevant issues.
- Second prototype with full pixel cell and simplified end of column logic
- Third prototypes with 640 pixels. Bump bonding for connection to sensor
- Full end of column logic included.



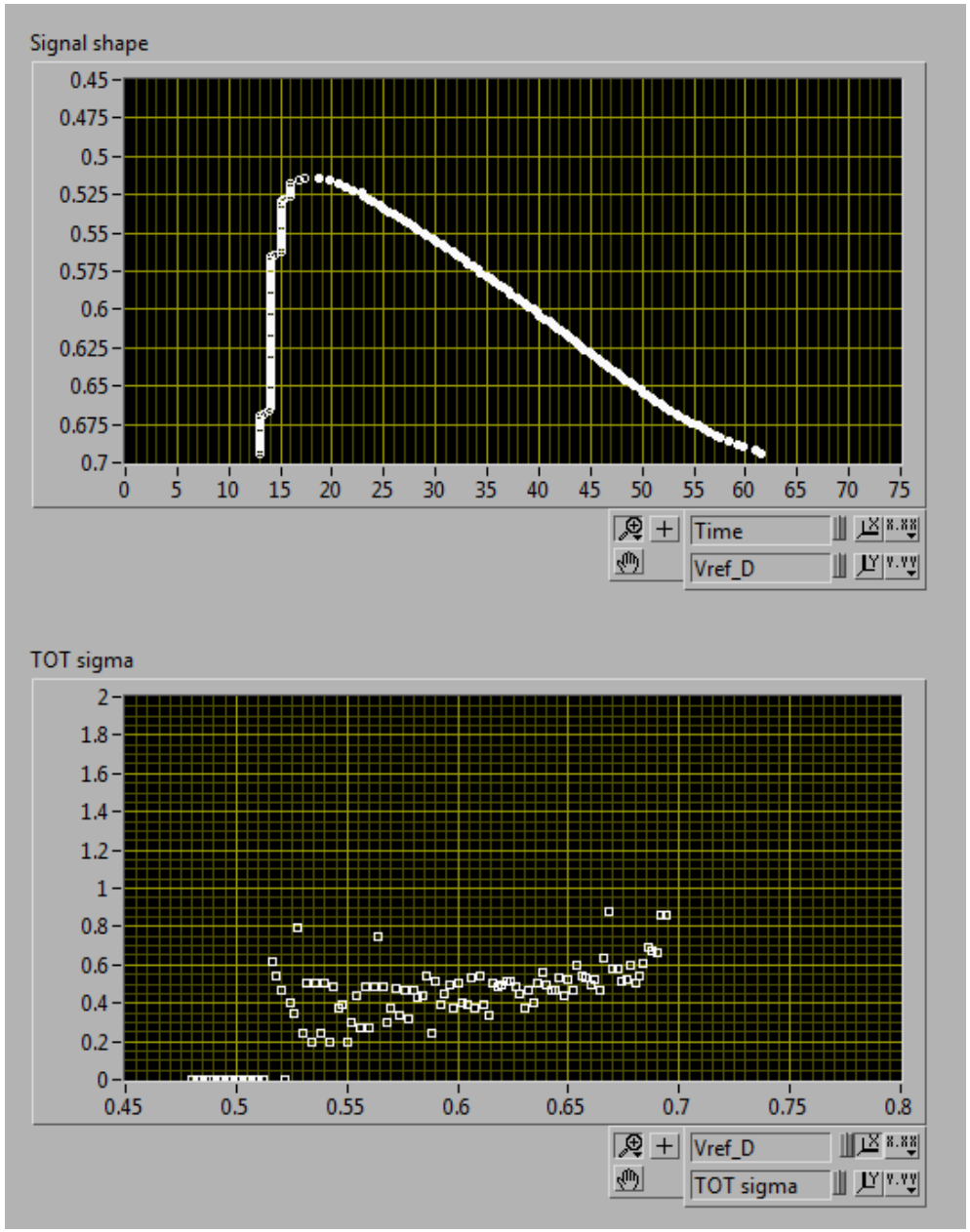
Test board

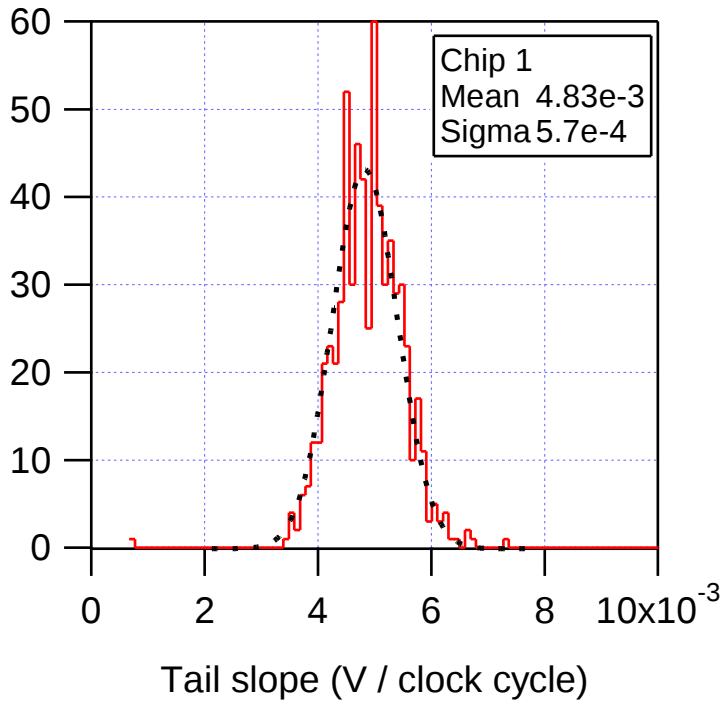

INFN TORINO
Lab.Elettronica
TOPIX3-PANDA
M.Mignone 2011




FBK-IRST
PANDA TORINO
PANDA TORINO
FBK-IRST

Reconstructed analog pulse

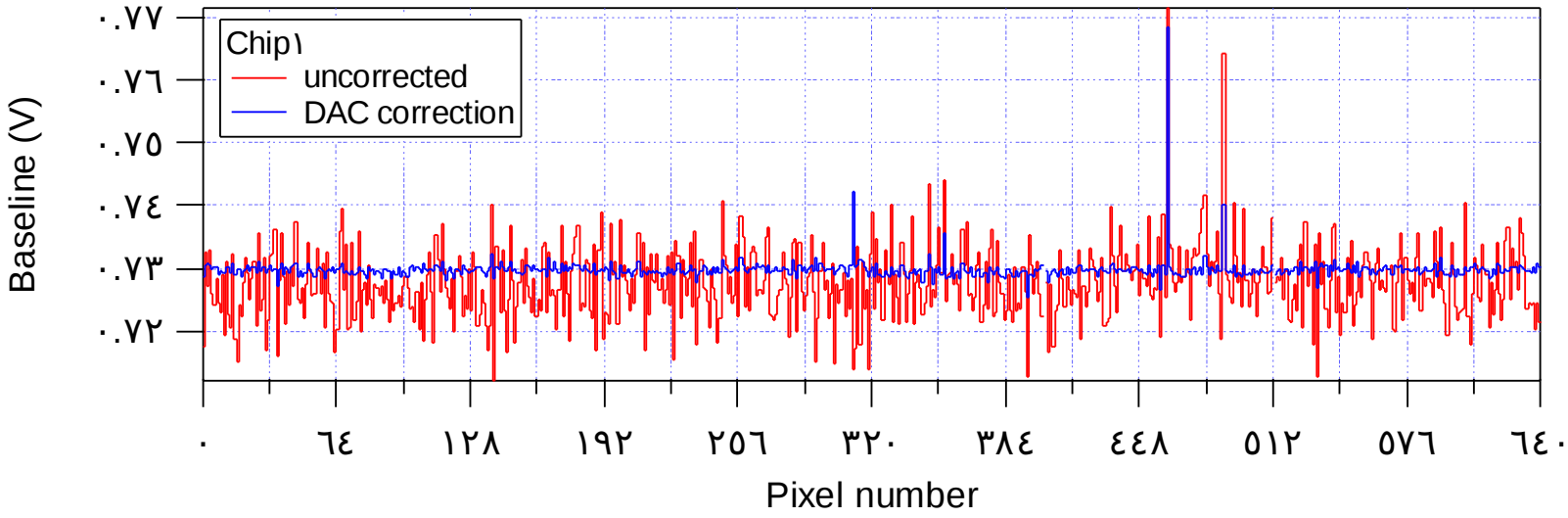


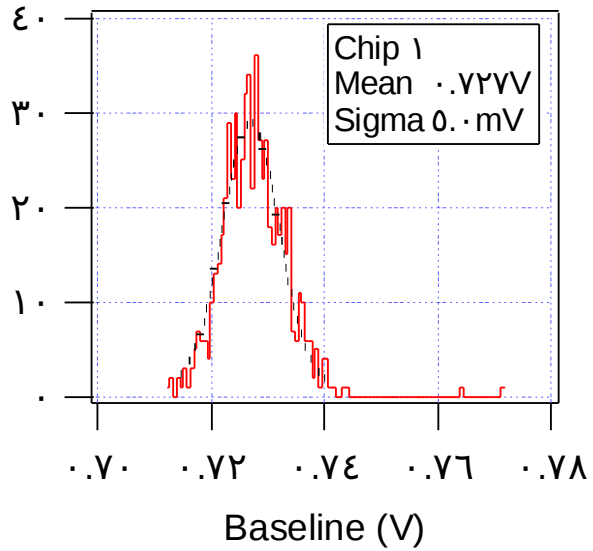


- Gain spread according to Monte Carlo simulations

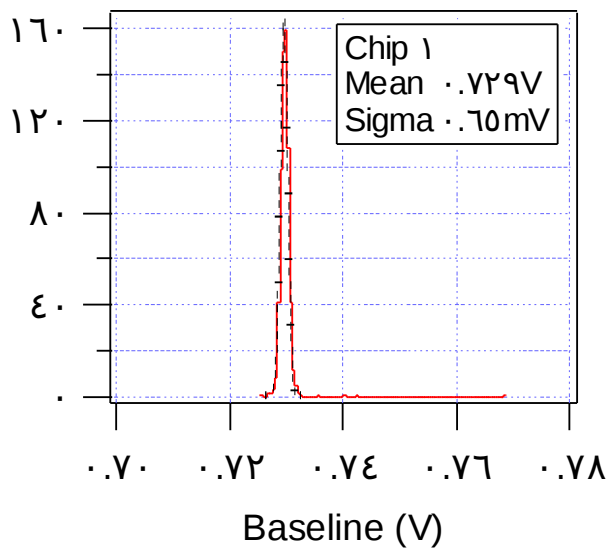
Offset before and after trimming

Baseline distribution and correction



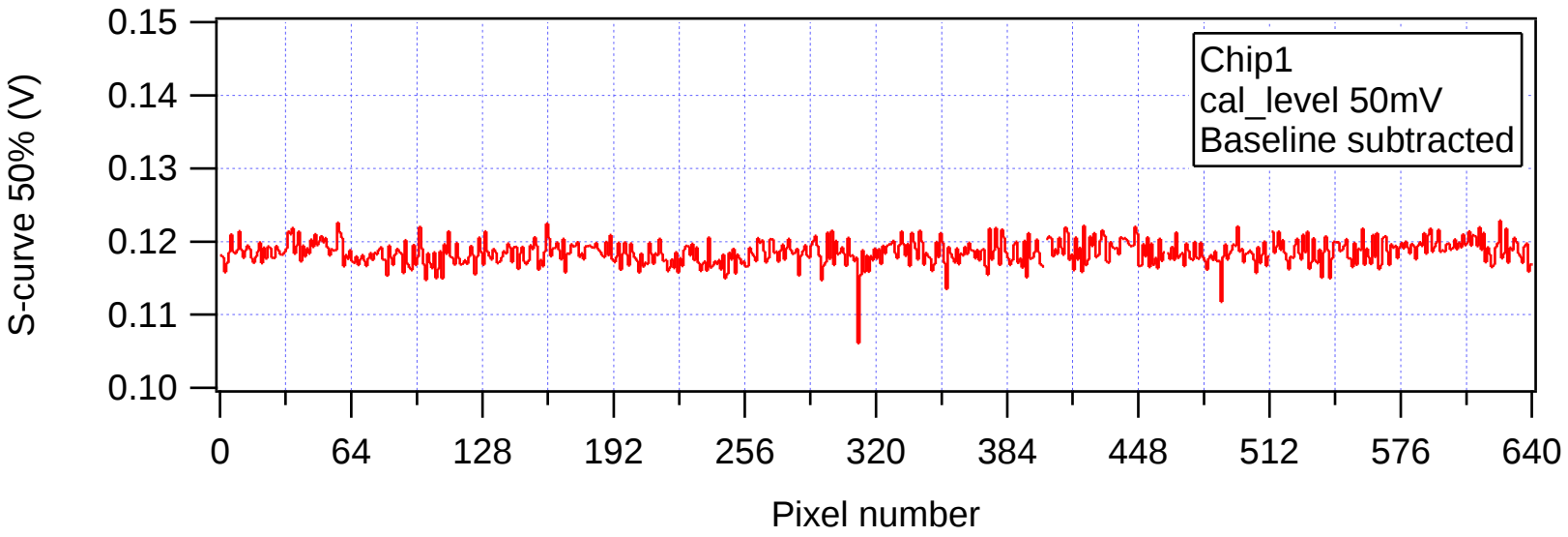


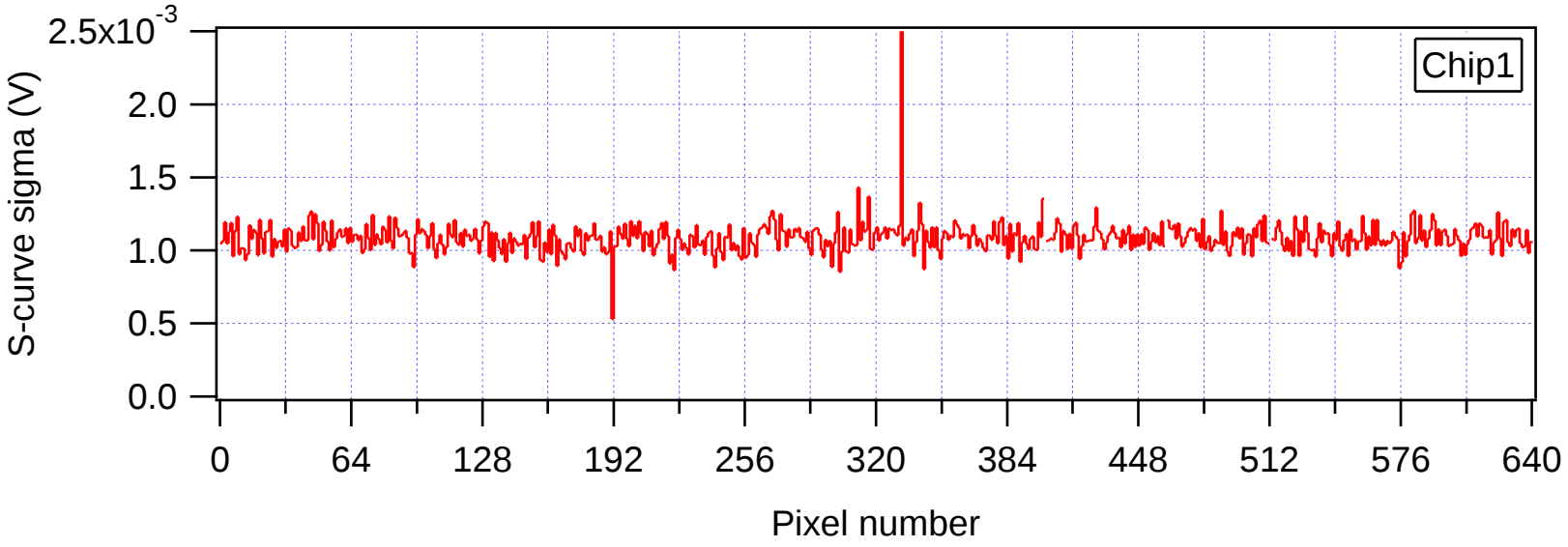
DAC correction



Gain and noise measurement

Noise below 100 rms electrons





Status and perspective

- The design of the PANDA HPS is well advanced.
- A reduced scale prototype of the HPS front-end embedding all the critical blocks has been implemented and is under test.
- First electrical test match the expectations, more detailed investigation in progress.
- Minor issues indentified and easy to correct in a future version.
- Assemblies with chip bump bonded to sensors expected soon.
- Results with full assemblies expected before the end of the year.