Contribution ID: **18** Type: **not specified**

DISAGGREGATING SYSTEM ARCHITECTURES (e.g. MEMORY SYSTEMS) FOR FUTURE HPC AND ARTIFICIAL INTELLIGENCE WORKLOAD

Tuesday 9 September 2025 09:40 (50 minutes)

With staff experience averaging more than 20 years, our seasoned team of design engineers and manufacturing professionals have solid expertise in high-density, low-power products. They work in deep submicron nodes with a keen eye for cost-size-weight reduction and design sustainability. They have created sensors, FPGAs, SerDes, memory chips (DRAM, MRAM, and RRAM), ASICs, AI systems, and many other ingenious devices.

As pioneers in advanced packaging and heterogeneous integration, our team boasts an admirable record of creating successful state-of-the-art products.

Presenter: PATTI, Robert (CeO NHanced-Semiconductors, USA)

Session Classification: POST MOORE, POST EXASCALE HIGH PERFORMANCE COMPUTING ERA