3D interconnects for readout electronics

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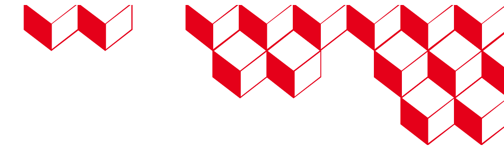
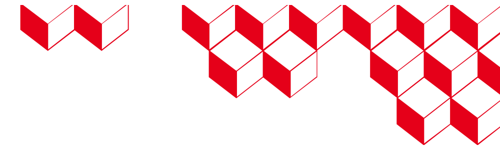
AIDAinnova Course on Quantum Applications – 23-24 January 2025, CERN



Outline

- Towards vertical integration ?
- Enabling 3D integration toolbox
- Focus on sensing applications
- Fan-out wafer-level packaging
- Integration challenges



3D integration… not really a new idea !

Three-Dimensional IC Trends

YOICHI AKASAKA

Invited Paper

VLSI will be reaching to the limit of minimization in the 1990s, and after that, further increase of packing density or functions might depend on the vertical integration technology.

Three-dimensional (3-D) integration is expected to provide several advantages, such as 1) parallel processing, 2) high-speed operation, 3) high packing density, and 4) multifunctional operation.

Basic technologies of 3-D IC are to fabricate SOI layers and to stack them monolithically. Crystallinity of the recrystallized layer in SOI has increasingly become better, and very recently crystal-axis controlled, defect-free single-crystal area has been obtained in chip size level by laser recystallization technology.

Some basic functional medels showing the concept or image of a future 3-D IC were fabricated in two or three stacked active layers.

Some other proposals of subsystems in the application of 3-D structure, and the technical issues for realizing practical 3-D IC, i.e., the technology for fabricating high-quality SOI crystal on complicated surface topology, crosstalk of the signals between the stacked layers, total power consumption and cooling of the chip, will also be discussed in this paper.

INTRODUCTION

The ultimate IC structure of the future is thought to consist of stacked active IC layers sandwiched by insulating materials.

Various devices or circuit functions, such as photosensors, logic circuits, memories, and CPUs, will be arranged in each active layer and, as a result, a remarkable improvement in packing density and functional performance will be realized.

In 1979, it was reported that polysilicon deposited on insulator can be melted and recrystallized by laser irradiation [1] and that the crystal perfection of the layer can be adequate to allow the fabrication of devices.

The quality of the recrystallized layer can be characterized by carrier mobility. As shown in Fig. 1, the electron mobility reported so far has increased year by year and has attained a value comparable to bulk crystals. This improvement was a trigger for starting research and development of 3-D ICs.

A partial 3-D structure has already been tried for a dynamic memory (DRAM) cell [2], [3]. For high-density RAMs,

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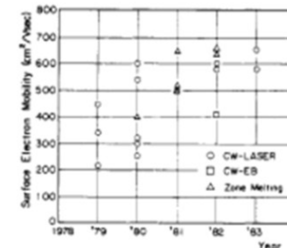


Fig. 1. Progress of surface carrier mobility of MOSFET fabricated on SOI layer. ○—CW laser; □—electron beam; △—carbon strip heater.

such as the 4-Mbit DRAM, the area of the memory cell capacitor is limited, so in order to increase the cell capacitance, a 3-D structure, i.e., a trench cell or a stacked capacitor cell, has been tried. This partial 3-D structure will be used in 2-D VLSIs within a few years.

To achieve a breakthrough in the packing density of advanced VLSIs, it is reasonable to consider a 3-D structure, containing either partially or completely stacked active layers. Fig. 2 shows a forecast of the development of 3-D ICs schematically, as 3-D technology progresses. This figure was obtained from the 3-D IC Research Committee of the 3-D

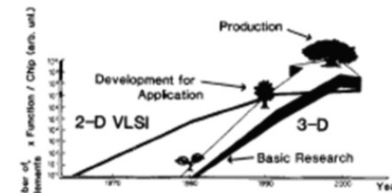
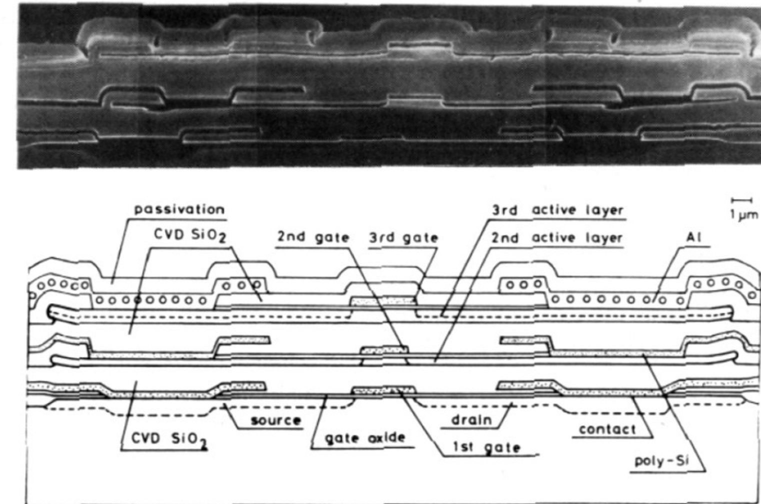


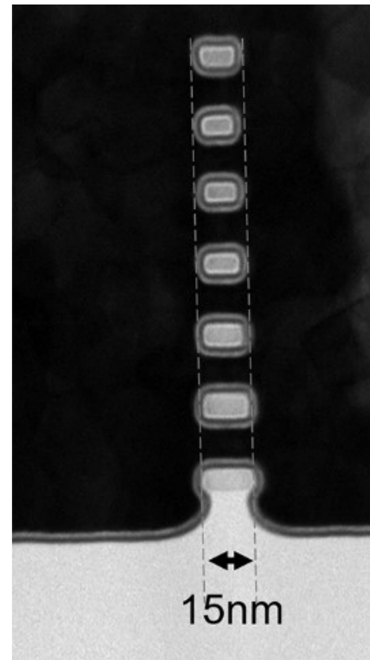
Fig. 2. Forecast of progress of 3-D technology.



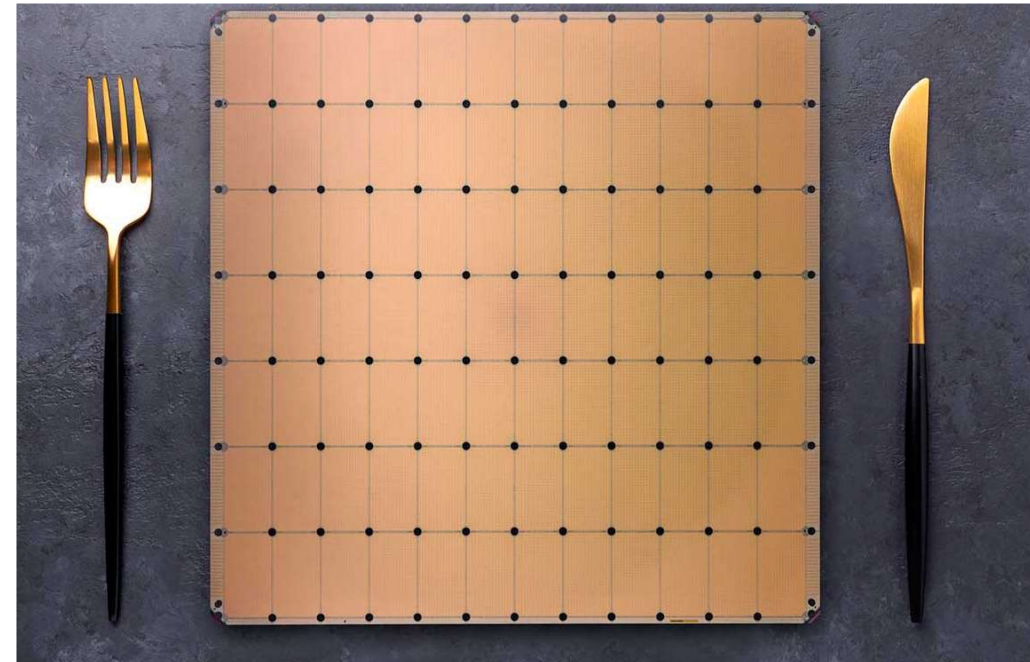
Akasaka expected 3D-IC mass production around 2000…

[1] Y. Akasaka, Proceedings of the IEEE, Vol. 74, NO. 12, Dec. 1986

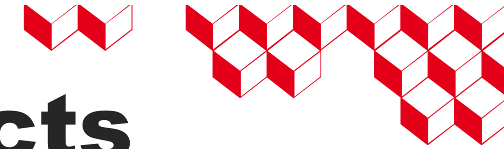
But Moore's law has taken up a lot of space...



7-level stacked “Nanosheet” gate all around transistor, CEA-Leti 2020

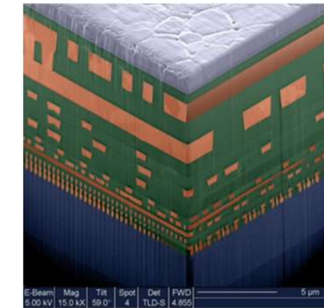


Cerebras WSE-2, 2.6 Trillion transistors, 7nm TSMC
© Elizaveta Elesina / Cerebras



Moore's law puts pressure on interconnects

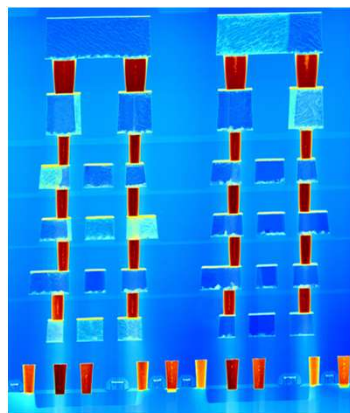
- **Consequences of miniaturization**
  Dramatic R.C product increase → interconnect delay
- **Countermeasures to reduce R.C**
  Switch from Al to Cu & low-k dielectrics, air gaps



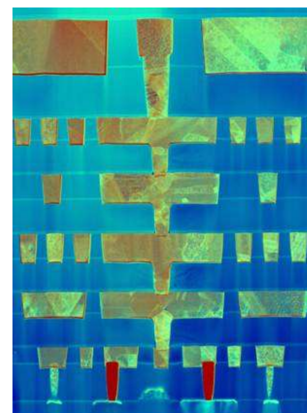
Circuit cross section

CMOS node	130 nm	32 nm
Interco. layers	6	9
M1 min. pitch	350 nm	112,5 nm
M4 min. pitch	756 nm	168,8 nm
M6 min. pitch	1204 nm	337 nm

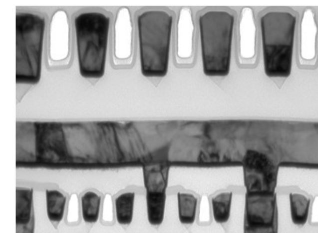
Back end of line design rules (Intel)



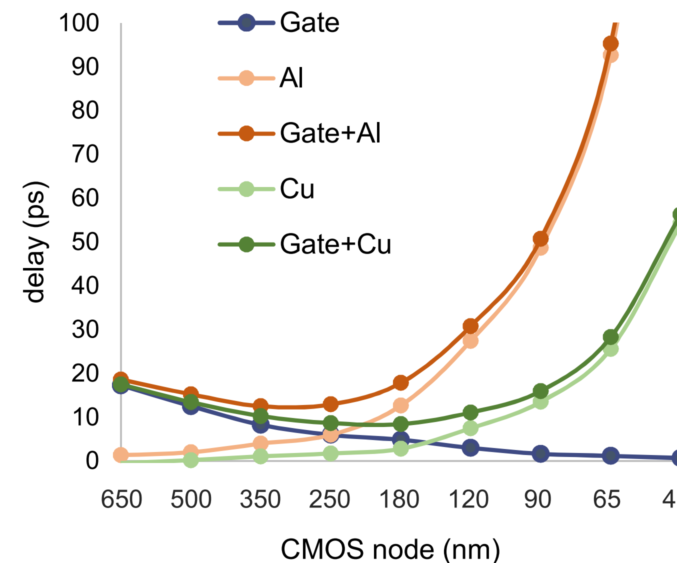
Al lines / W vias
SiO_2 dielectric



Cu line & via
Low-k dielectric



Intel 14nm CMOS BEOL

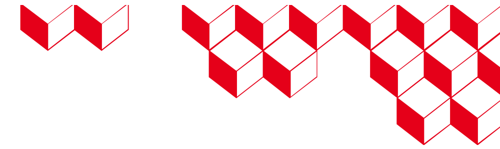


$$I_{ON} = \frac{1}{2}\mu_0 . C_{ox} . \frac{W}{L} . (VG - VTh)^2$$

$$\tau_{gate} = \frac{C_G \, V_{DD}}{I_{ON}}$$

$$\tau_{interconnect} \propto RxC$$

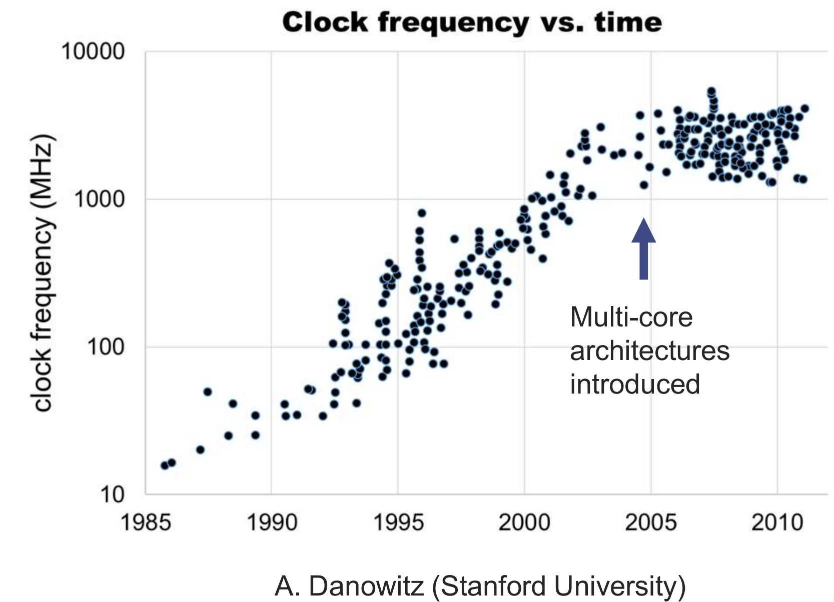
- **R.C delay has become a major performance issue**



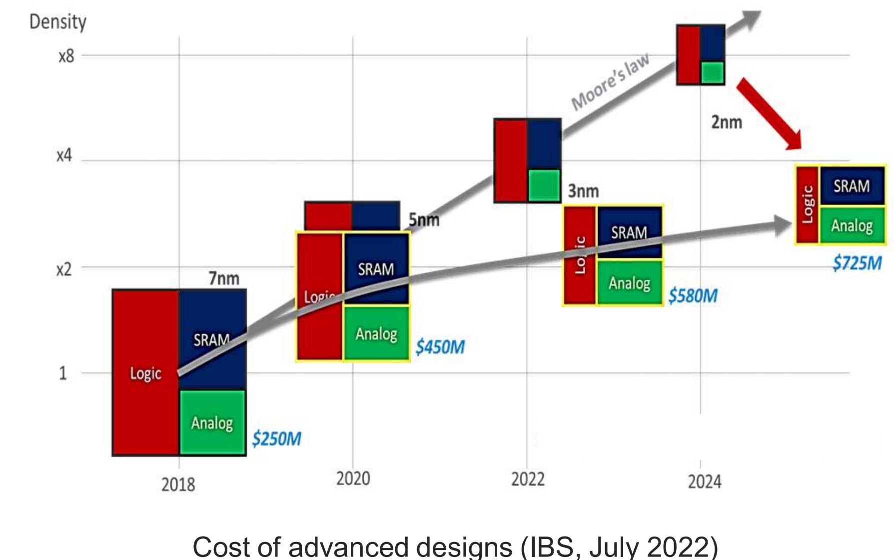
New paradigms emerged

- **Interconnects Bottleneck**
  Circuit frequencies limited
  Limited bandwidth between chips
- **Scaling becomes costly**
  High manufacturing cost, low yield with large die
  High development cost: masks, IP porting, verif…
- **Heterogeneous architectures needed**
  More processing: AI, perception accelerators…
  More data to handle: memory capacity, fusion…
  More modularity, scalability & sustainability

How to reach them ?

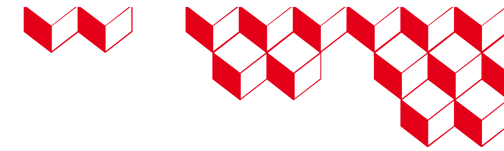


A. Danowitz (Stanford University)

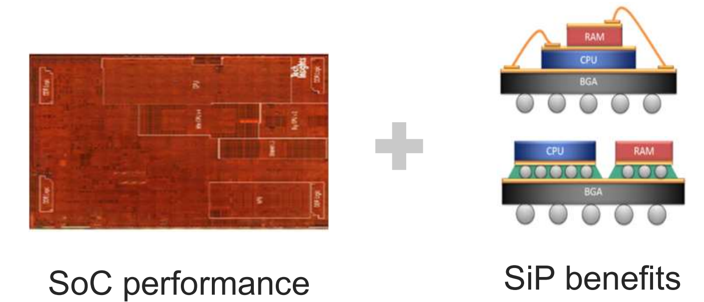


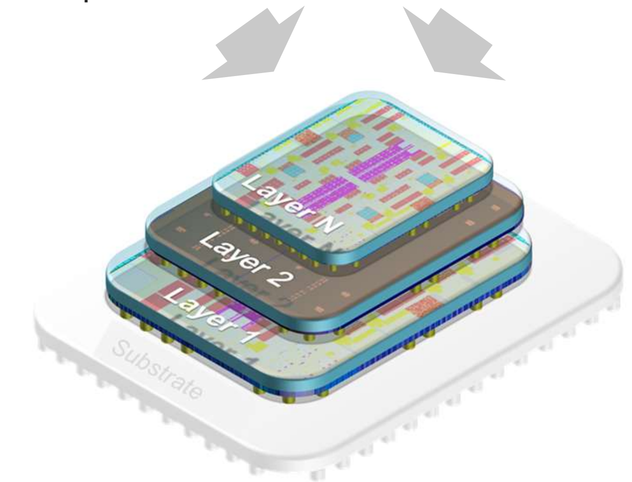
Cost of advanced designs (IBS, July 2022)

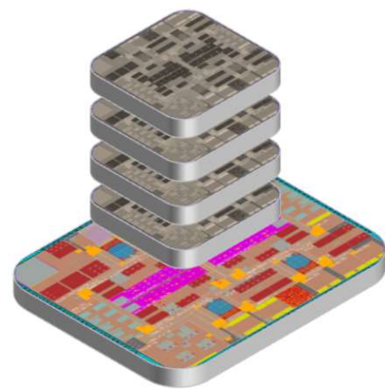
3D benefits for advanced systems



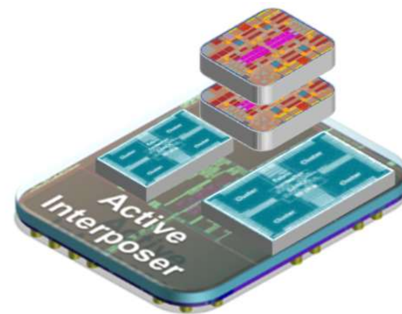
- **Best of all trends: Moore + more than Moore**
  System on Chip performance + System in Package diversity
- **High-performance interconnections**
  Low R, L, C + massively parallel vertical processing
- **Modern answers to design needs**
  Partitioning, IP reuse, scalability & density, heterogeneity

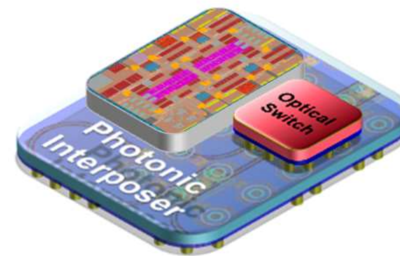




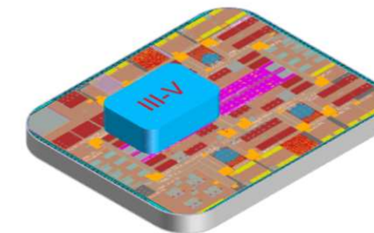


Memory on Logic

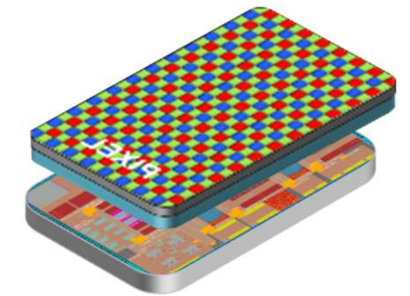




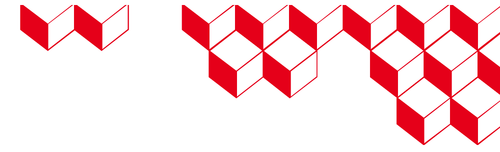
Chiplet-based integrations



III-V on Logic

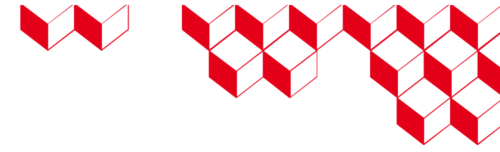


Sensor on logic



1.

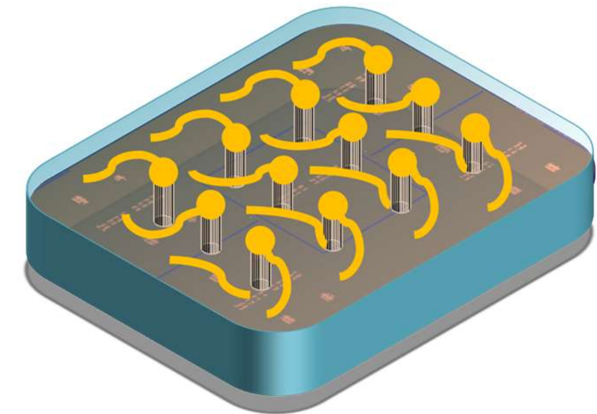
Enabling 3D integration toolbox

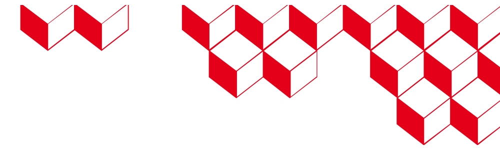


Morphology of a 3D circuit

- **<u>Thin</u> stacked layers**
  Layer 1 (# bottom die) / (…) / Layer N (# top die)
- **Layer-to-layer vertical interconnects**
  Miniaturization trend: pillars, hybrid bonding …

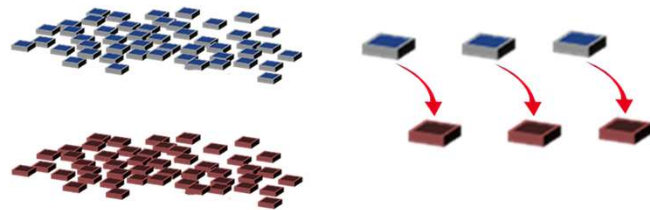
- **Intra-layer vertical interconnects**
  Communication between frontside and backside of each layers
  Through silicon vias (TSV), Through glass vias (TGV)…
- **Intra-layer in-plane interconnects (2D)**
  ReDistribution Layers (RDL)





Assembly configurations

Die to die

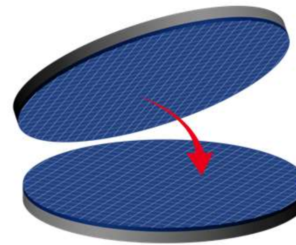


(+)
- Known Good Dies → yield
- Heterogeneous integration
- Flexible design

(−)
- Low assembly throughput
- Low alignment accuracy
- Very high cost

Pure packaging operation

Wafer to wafer

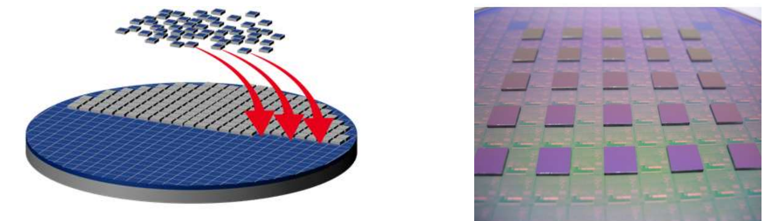


(+)
- Collective process
- High assembly throughput
- High alignment accuracy

(−)
- Yield loss
- Strong design limitation

Mass production for image sensors and memories

Die to wafer



(+)
- Known Good Dies → yield
- Heterogeneous integration
- Flexible design

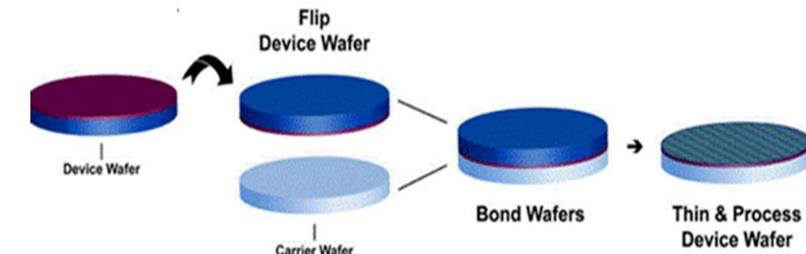
(−)
- Low assembly throughput
- Low alignment accuracy

Breakthrough processes needed

Wafer bonding techniques

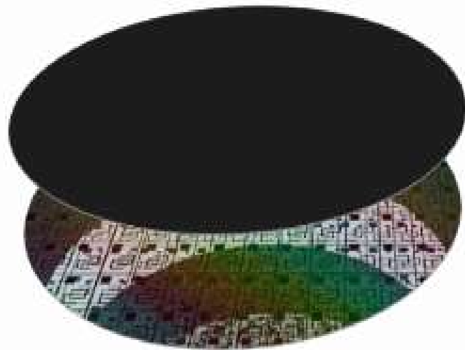
- **Why & how ?**
  Thin wafer processing (<300µm)
  Wafer-to-wafer 3D stacking
  Temporary or permanent bonding

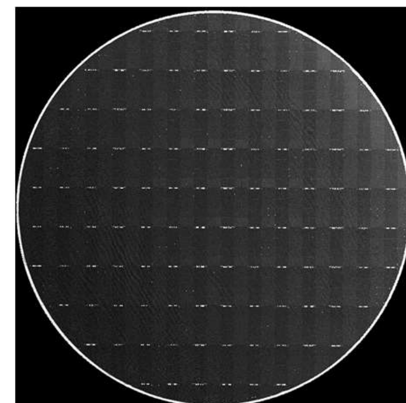
50 µm thin silicon wafer

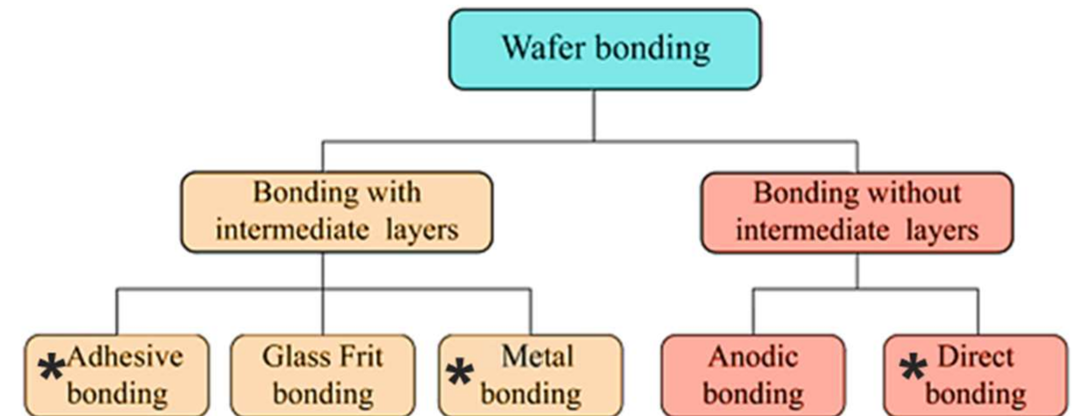


Thin wafer processing on carrier

- **A wide range of processes**
  Each with own strengths and weaknesses




Scanning acoustic microscopy



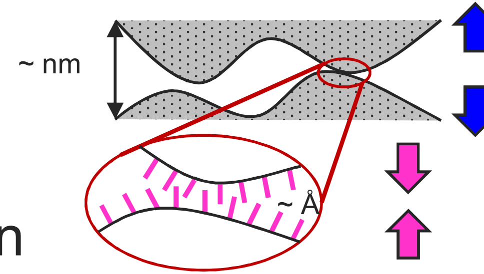
*** most used processes**

Direct bonding process

- **Bonding without added material**

  Based on attraction of very smooth surfaces

  Flatness & cleanliness at all scales → planarization



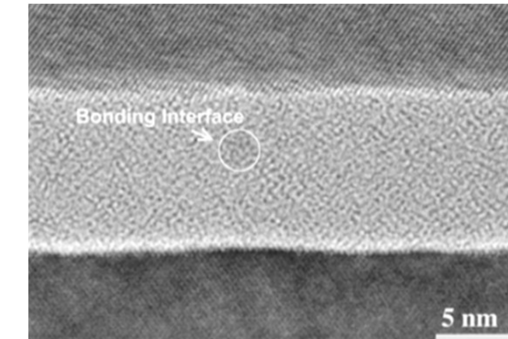
Bonding wave: glass to Si & Si to Si bonding

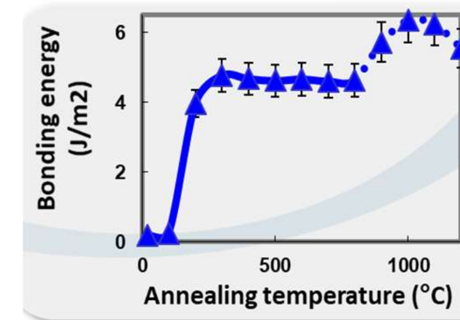
- **SiO_2/SiO_2 bonding**

  Required roughness < 0,65nm rms [2]

  Van der Waals interaction at T_{amb}

  Covalent bonds formed after annealing



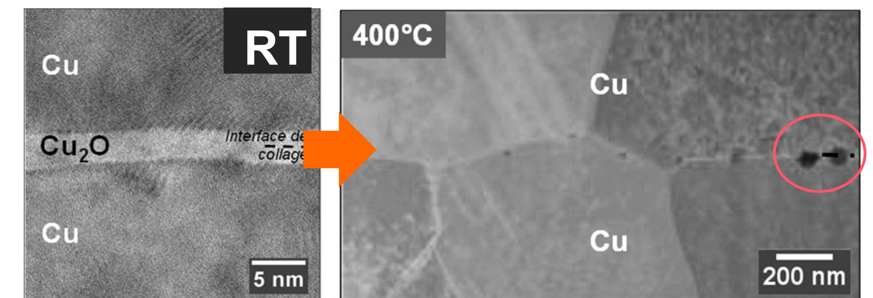


SiO_2/SiO_2 interface after annealing

- **Cu/Cu bonding**

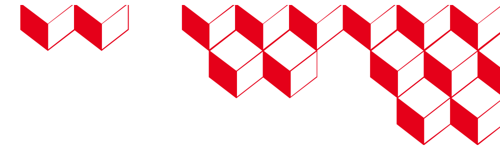
  Required roughness < 0,5nm rms [3]

  Cu recrystallization during annealing > 200°C [4]

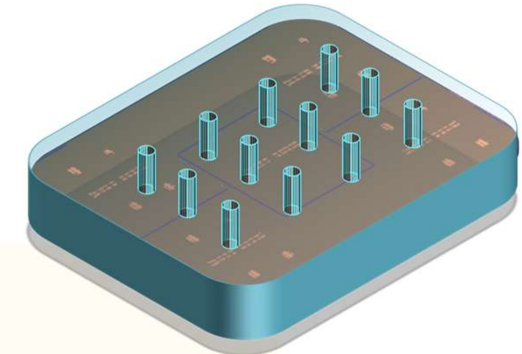


Cu/Cu interface before/after annealing

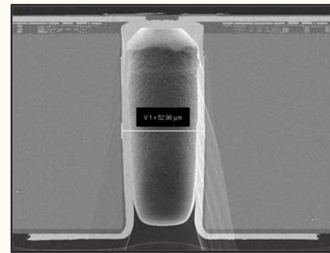
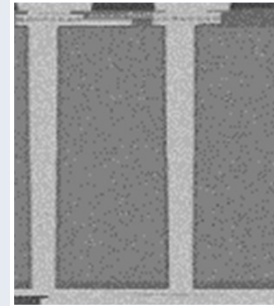
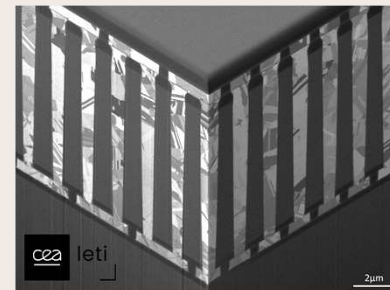
[2] F. Rieutord, et al. *ECS Trans.*, vol. 3, no. 6, pp. 205–215, 2006
[3] H. Moriceau, *Microelectronics Reliability*, vol. 52, no. 2, pp. 331–341, 2012
[4] L. Di Cioccio, et al., *J. Electrochem. Soc.*, vol. 158, no. 6, pp. P81–P86, 2011



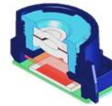
Intra-layer “through silicon via” (TSV)

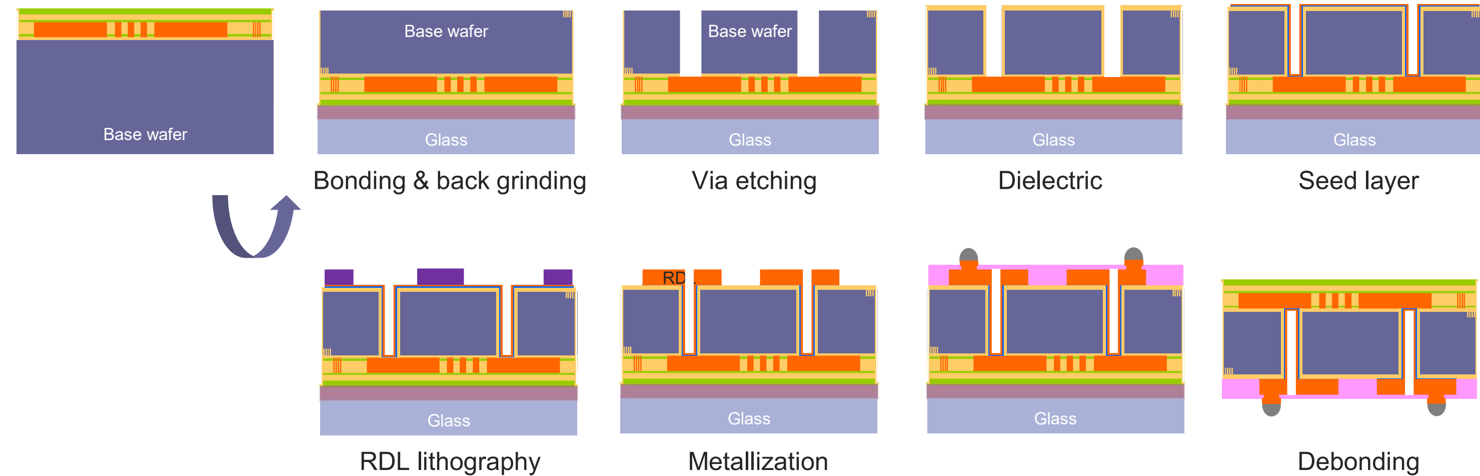


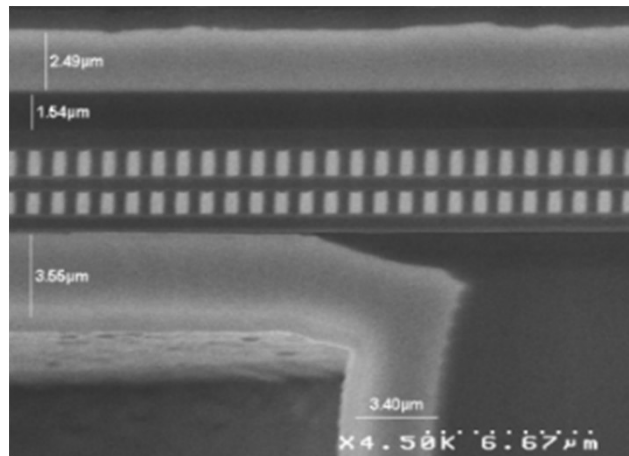
TSV pitch

TSV pitch	Type	Image	Density	Applications
100-500µm Ø 40-100µm R_{TSV} = 2-10 mΩ C_{TSV} = 2 pF	**TSV last low density**		100 TSV/mm^2 ➔ I/O level	**CMOS Image Sensors** **X-Ray focal plane arrays** **IR sensors**
20-50 µm Ø 2-15 µm R_{TSV} = 20 mΩ C_{TSV} = 0.1 pF	**TSV middle**		1 000 TSV/mm^2 ➔ core level	**System in Package** **Interposers / Chiplets**
1-10 µm Ø <2 µm R_{TSV} = 0,5-1 Ω	**High density TSV**		100 000 TSV/mm^2 ➔ logic bloc level	**3D Imagers** **Displays** **Power Delivery Network**

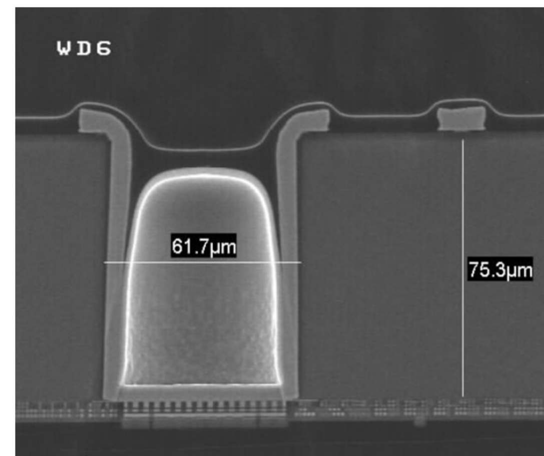
“TSV last” low density process

- **Done <u>after</u> full CMOS process [5]**
  Wafer bonding on carrier & low temp. process
  AR (= height/diameter) increased over time
  Keep out zone + alignment → area penalty
- **Industrially mature since 2008**
  CMOS image sensors 

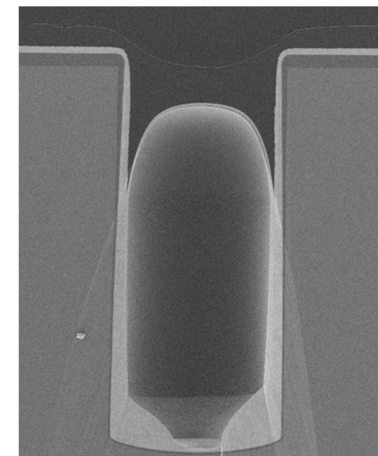


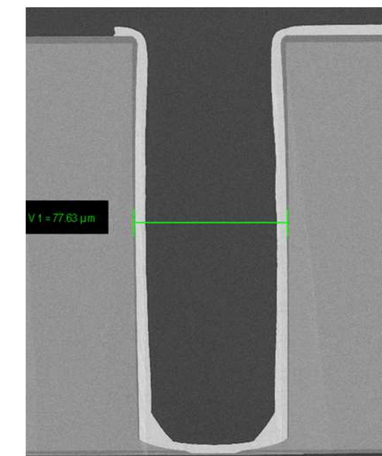


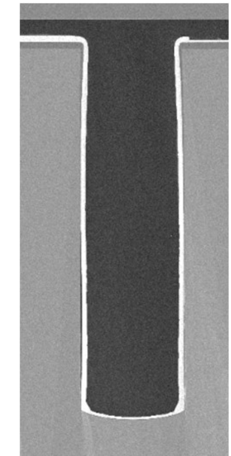
TSV contact on Metal1 layer



AR 1,2 after passivation


AR 2 after passivation

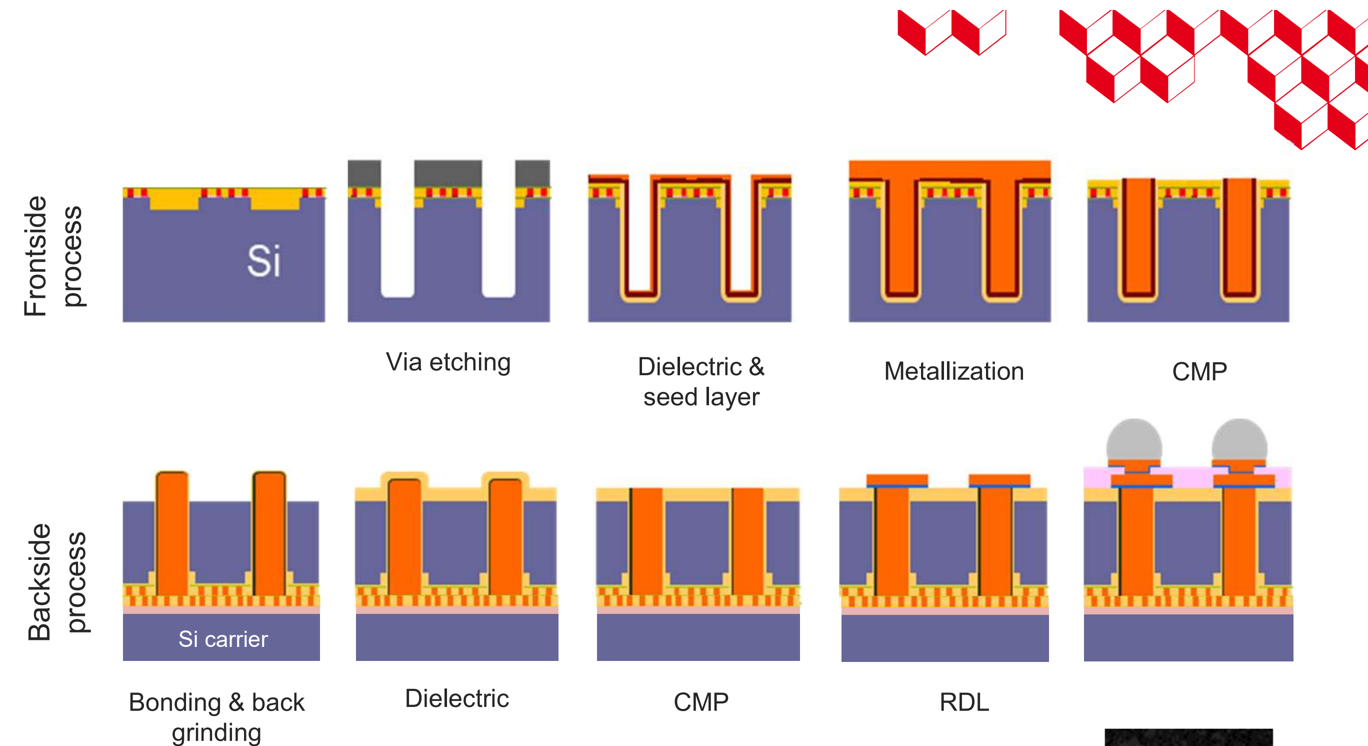

AR 2,5 after RDL

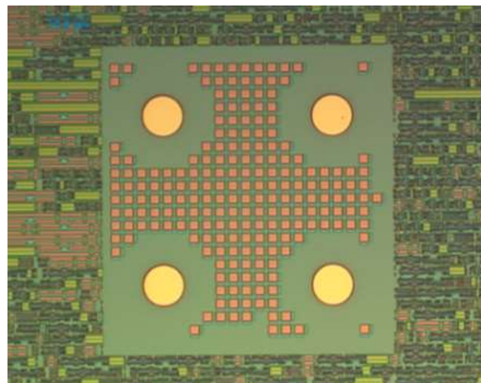

AR 3,7

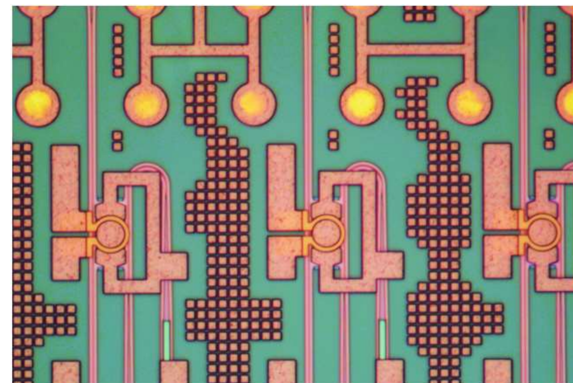
[5] D. Henry et al., Electronic Components and Technology Conference, 2008

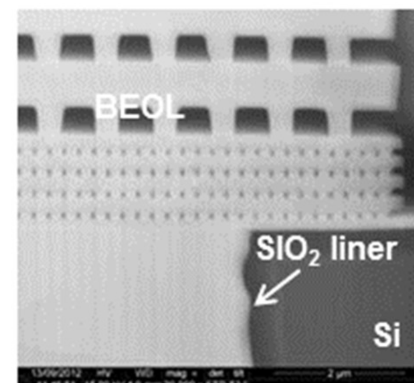
“TSV middle” process

- **Done <u>during</u> CMOS process [6]**
  Aspect ratio usually > 10, Diameter 2-15 µm
  TSV etched & filled with Cu prior to BEOL process
  TSV revealed on backside after Si thinning
  Reduced keep out zone vs. TSV last
- **Industrially mature since 2013**
  FPGA (Xilinx), DRAM stacks

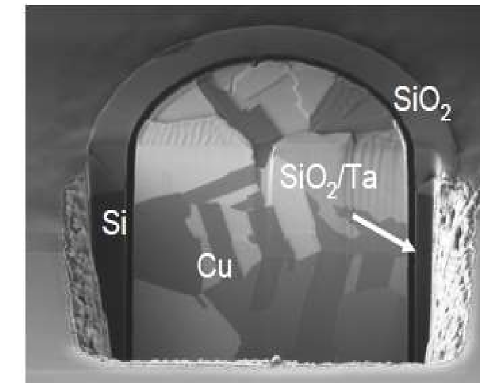



TSV Middle after CMP


TSV co-integrated with microring resonators

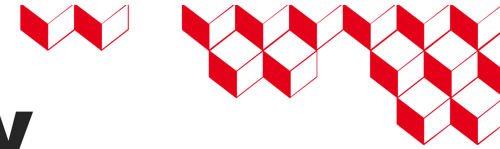


TSV & CMOS BEOL



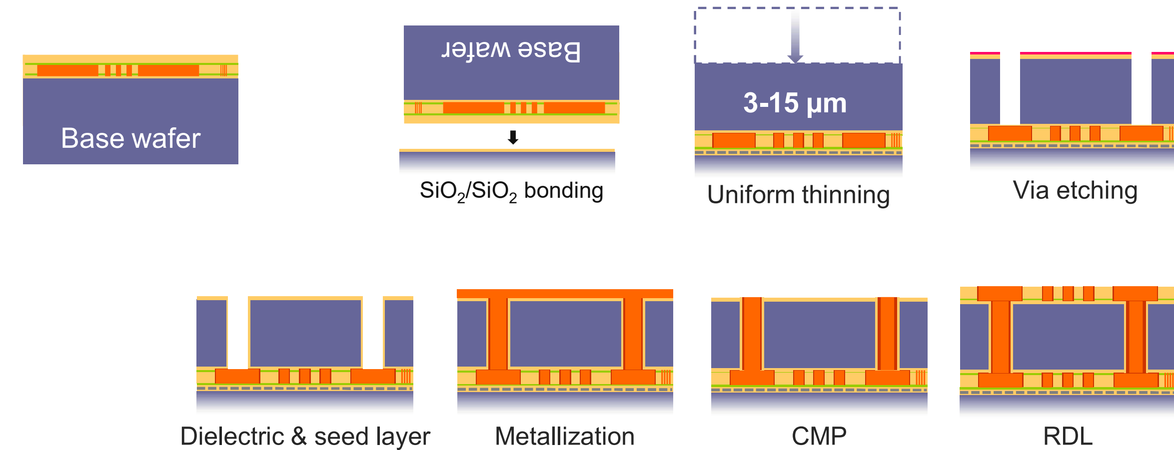
TSV structure

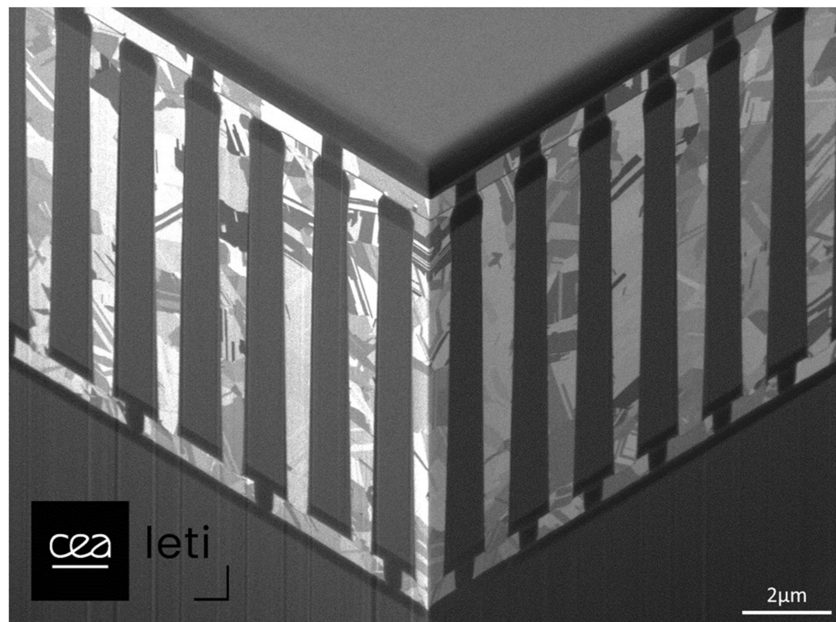
[6] P. Coudrain et al., EPTC 2012

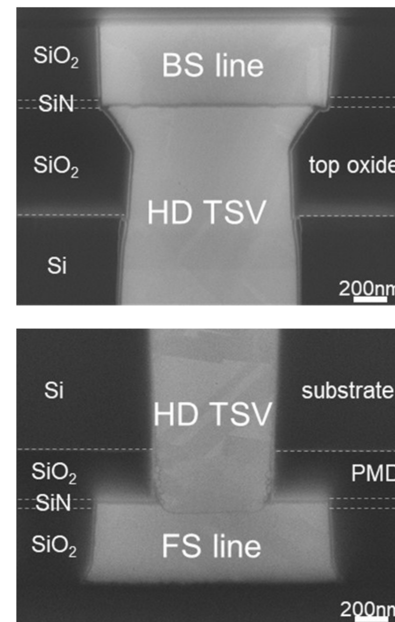


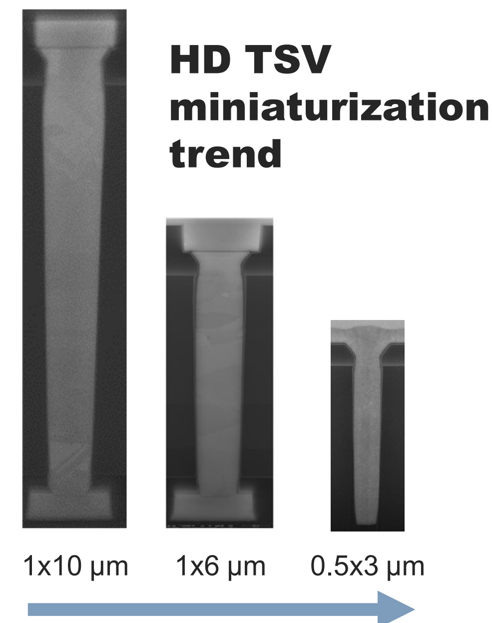
“High density TSV” (HD-TSV) process flow

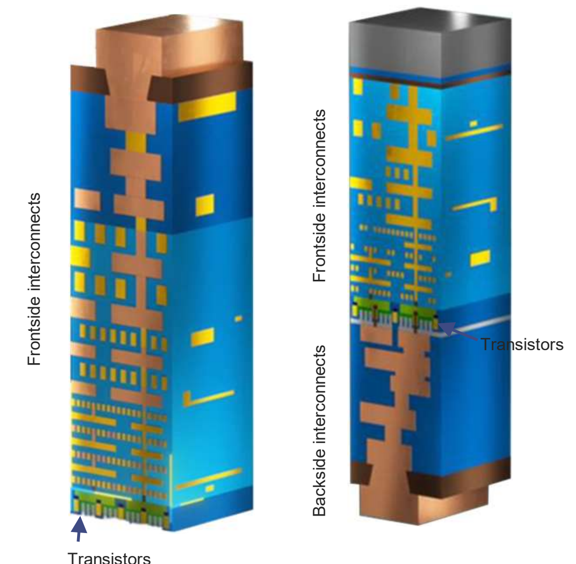
- **Done <u>after</u> circuit processing [7]**
  Diameter typically < 2µm & height <15 µm
  Ultra-uniform Si thinning (TTV < 1µm) → direct bonding
- **R&D activity**
  Power delivery network (PDN), SPAD arrays





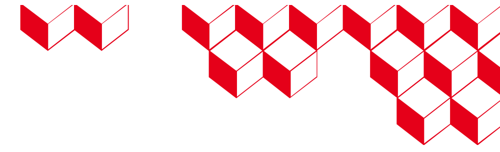






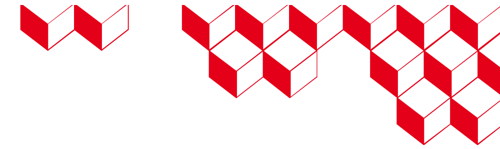
Frontside vs. backside power delivery network, Intel 2022

[7] S. Borel et al., ECTC 2023



Layer-to-layer 3D interconnects

3D pitch				
> 100µm	**Solder-based**		10^3/mm^2 Circuit level	Die to Die Die to Wafer Wafer to Wafer
100nm-10µm	**Hybrid bonding**		10^6/mm^2 Logic-block level	Die to Wafer Wafer to Wafer
<100nm	**Sequential 3D**		10^8/mm^2 Transistor level	Wafer to Wafer



Solder-based interconnects for flip-chip

- **Solder material choice linked to temperature**

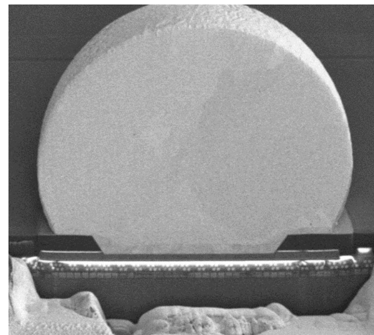
  SnPb (183°C), SnAg (221°C), (…) In (152°C)

- **Interconnects processing**

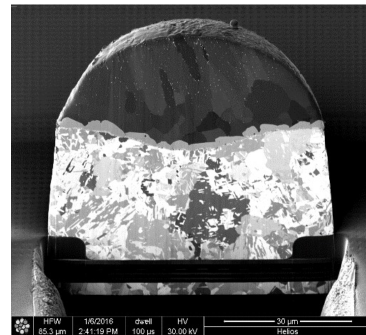
  Paste printing, ball serigraphy for large geometries

  Semi-additive process (ECD) for reduced pitch

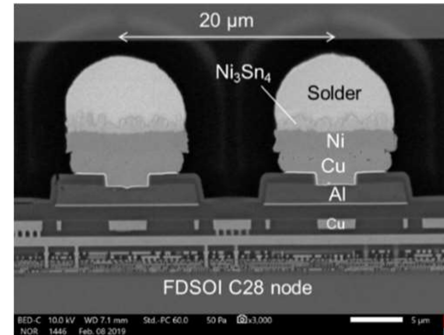
  Polymer underfill systematically added in free space



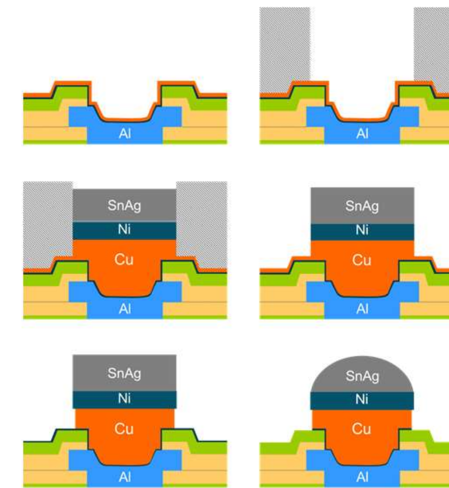
200µm diameter SnAgCu
Paste printing



70µm diameter Cu/SnAg
ECD



10µm diameter Cu/SnAg Pillars
ECD



Semi-additive process

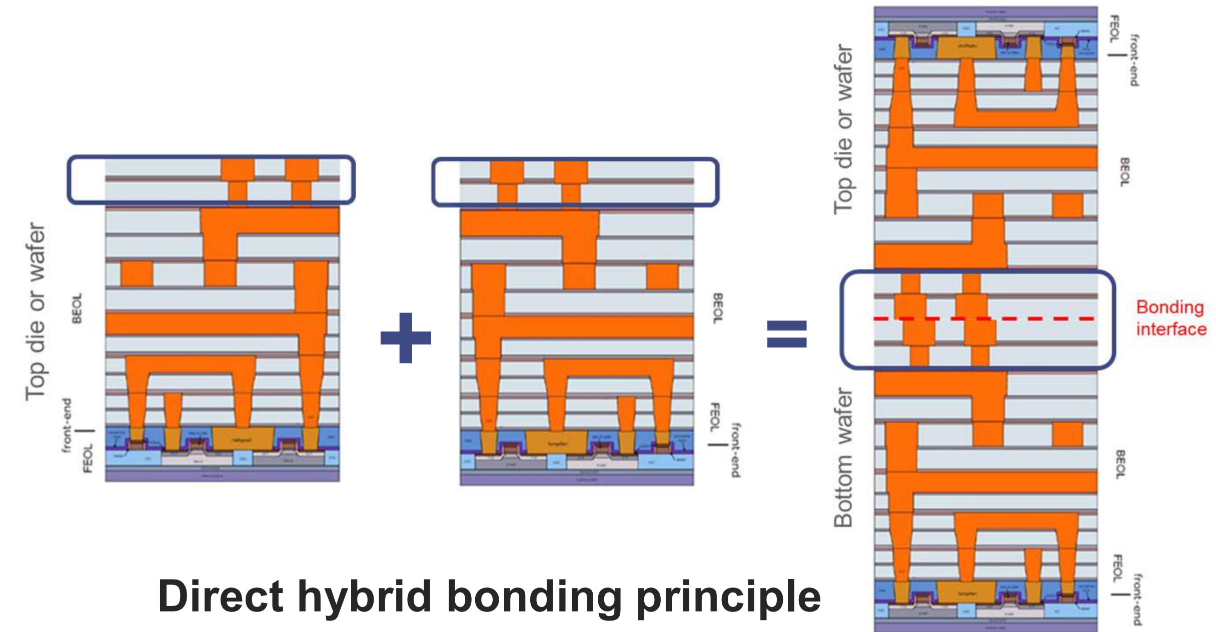
2-layer stack on BGA: 10µm Pillars between top and bottom and 70µm bumps between bottom and BGA [8]

- **Well mature technique, but limited in density**

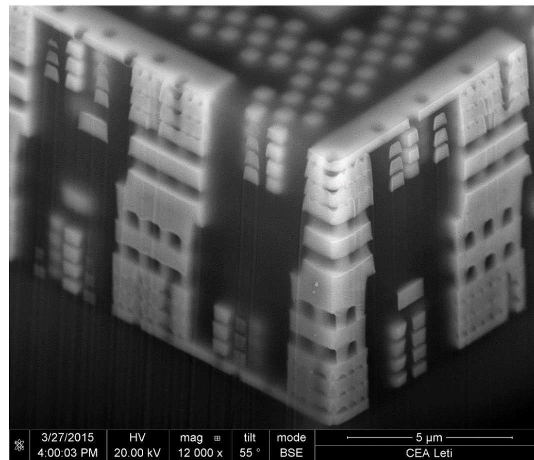
[8] P. Coudrain et al., ECTC 2019

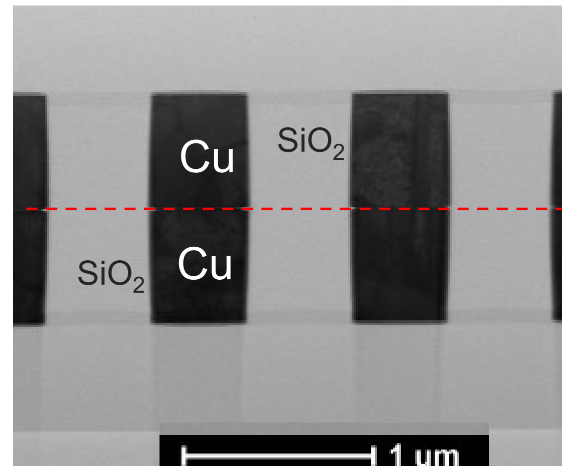
Direct hybrid bonding process: a hot topic !

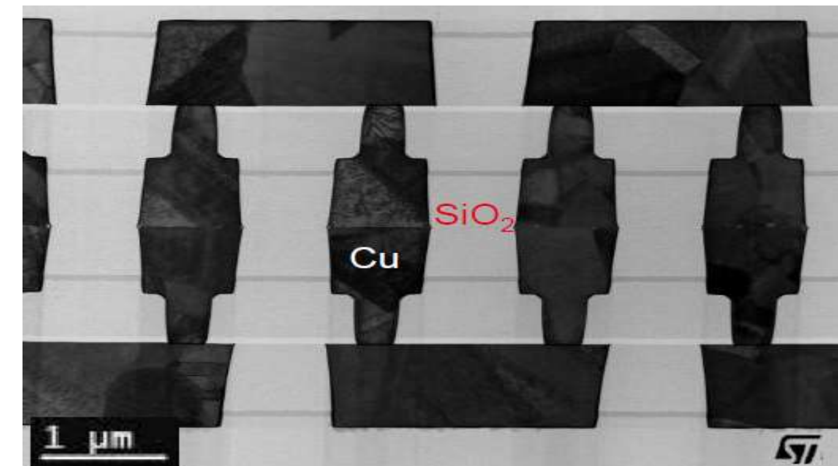
- **Mix SiO_2/SiO_2 & Cu/Cu bonding**
  Precautious chemical mechanical polishing
  Specific design rules to control dishing in Cu
- **Unprecedented interconnect pitch**
  1 µm pitch demonstrated in 2017 [10], 0.4 µm in 2024
  Precision alignment is key: 50nm expected in 2025



Direct hybrid bonding principle

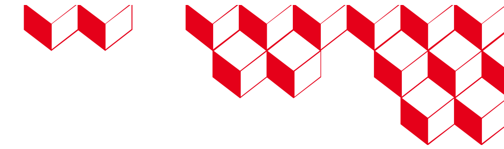






[9] Y. Beilliard, PhD Thesis, Univ. Grenoble Alpes, 2015

[10] J. Jourdon et al., IEDM 2018

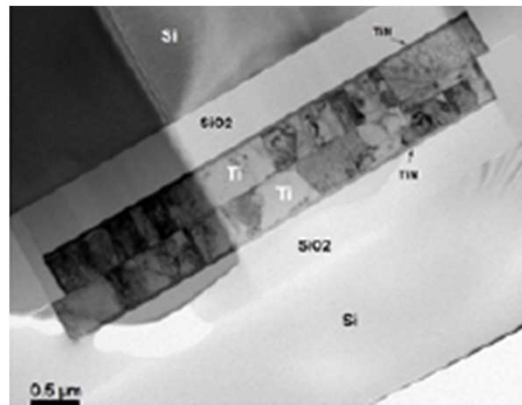


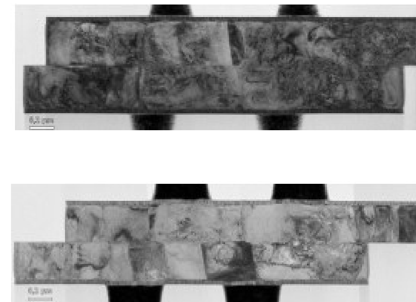
Non Cu-based bonding

• Ti/Ti hybrid bonding [11]

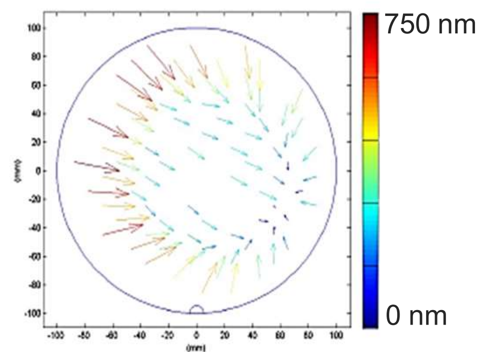
3x3 µm² pad, 7 µm pitch with sub-µm alignment

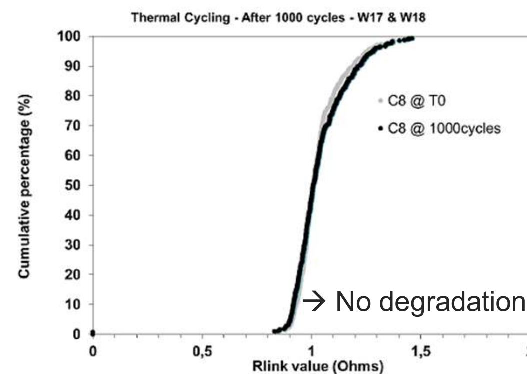
Reliability & RF characterisations up to 40 GHz





Interface after thermal storage (top) and thermal cycling (bottom)

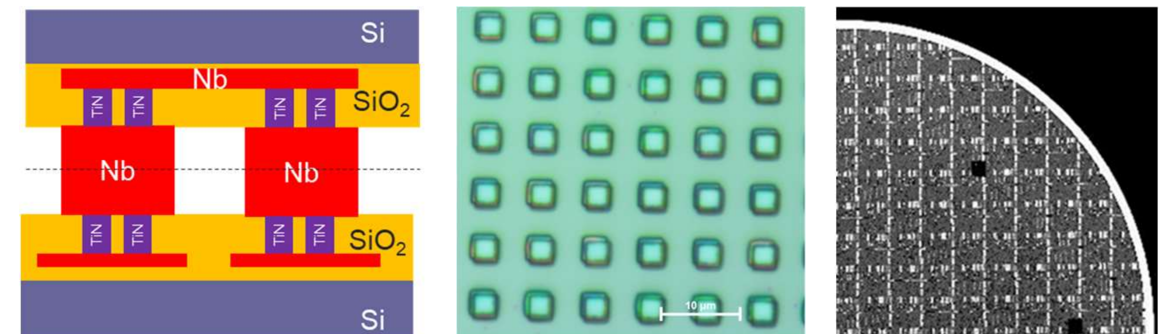


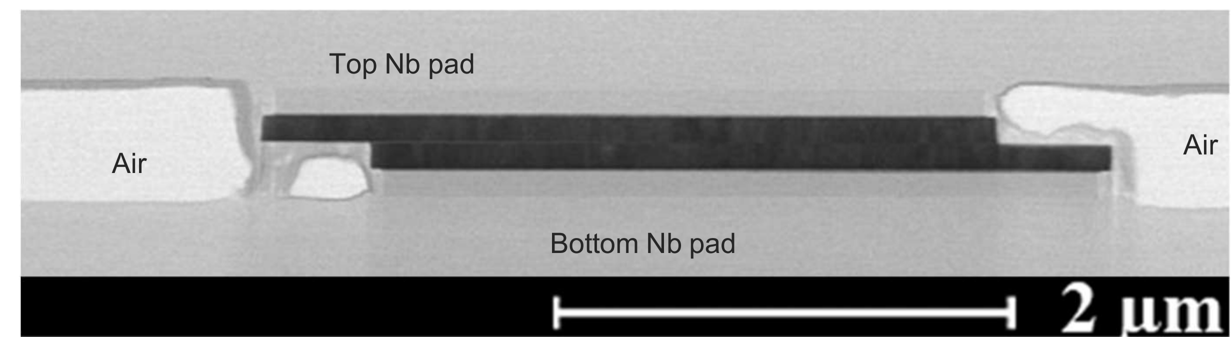


• Nb/Nb bonding [12]

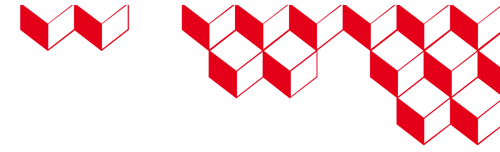
Superconducting interconnects

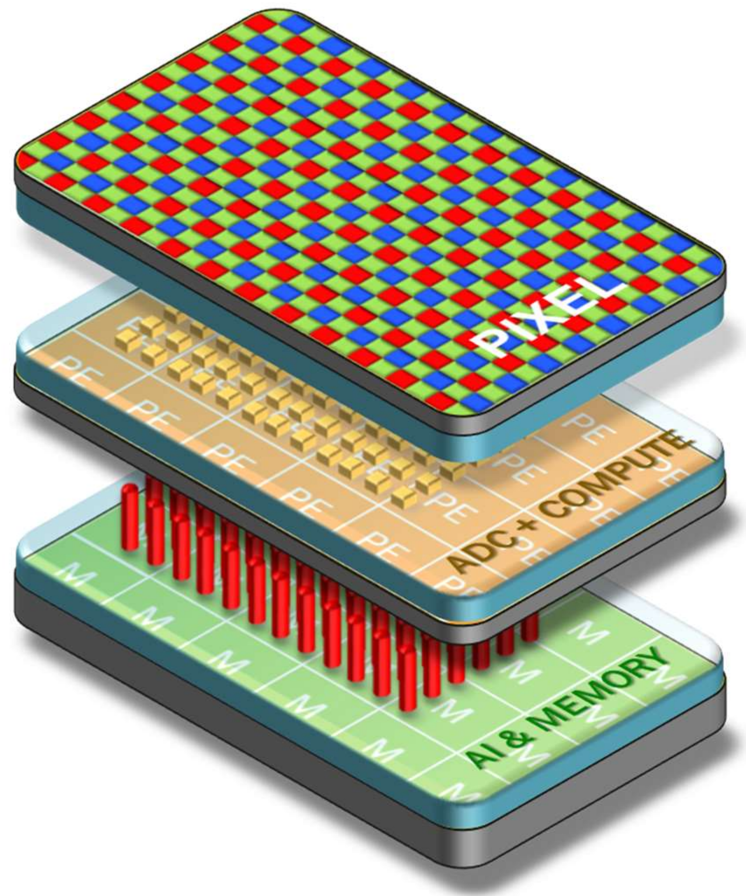
3x3 µm² pad, 7 µm pitch with sub-µm alignment





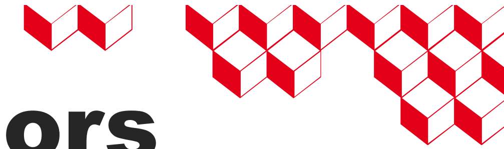
[11] A. Jouve et al., ECTC 2020
[12] P. Renaud et al., ECTC 2024





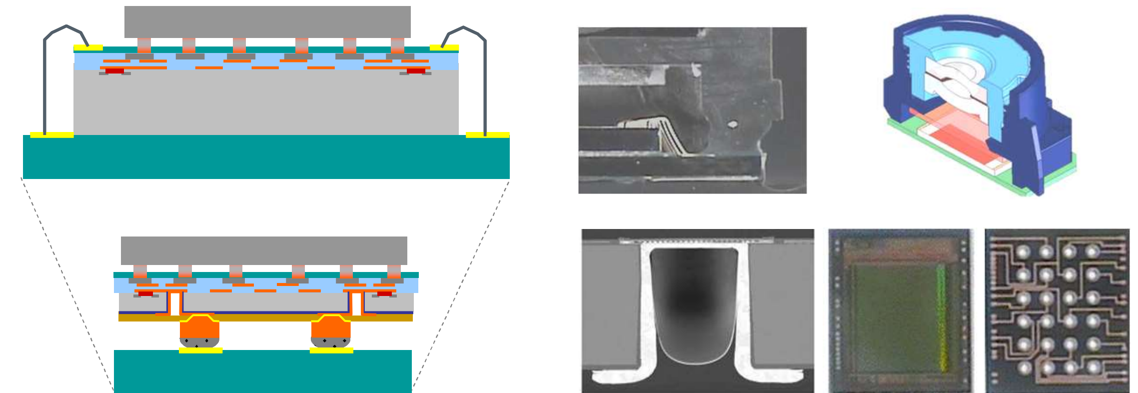
2.

3D integrated sensors

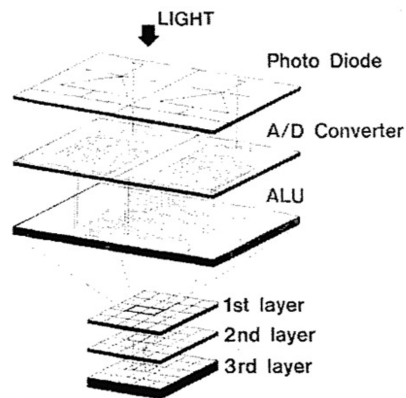


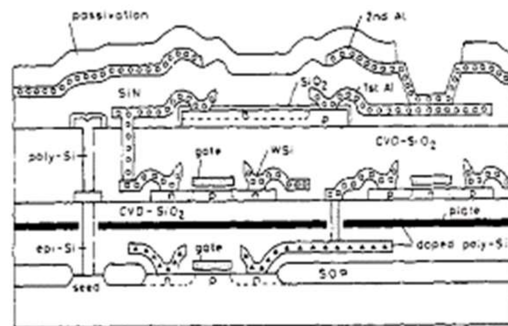
Benefits of 3D Integration for image sensors

- **Dimensional considerations**
  - Reduced form factor (x,y,z)
  - Abuttable sensors
- **Architectures exploration!**
  - Parallel pixel processing
  - Layers functionalization & optimization



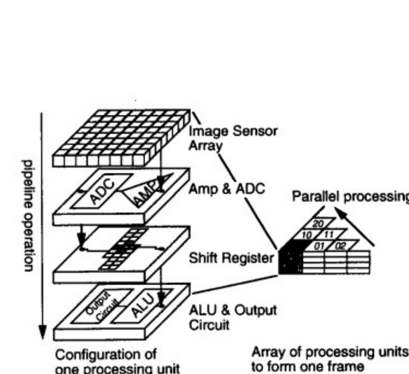
[4] D. Henry et al., Electronic Components & Technology Conference, 2008

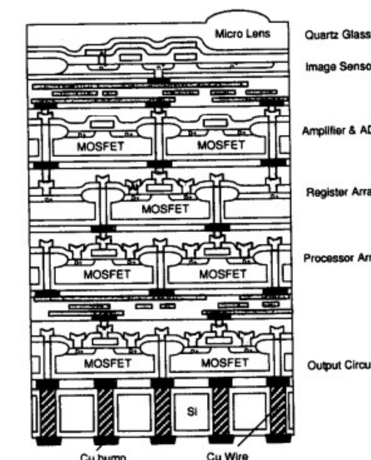


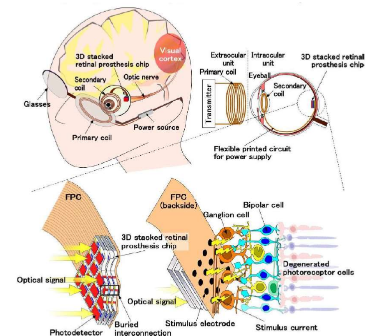


Mitsubishi [13]

[13] T. Nishimura et al., IEDM, 1987



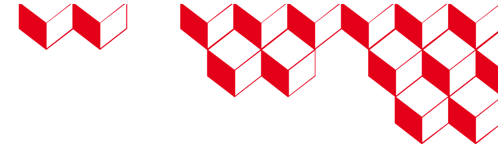




Tohoku University [14,15]

[14] H. Kurino et al., IEDM, 1987

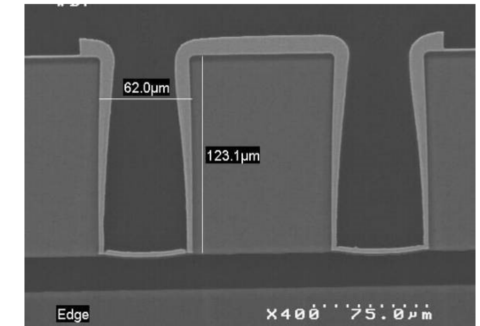
[15] T. Tanaka et al., IEDM, 2007

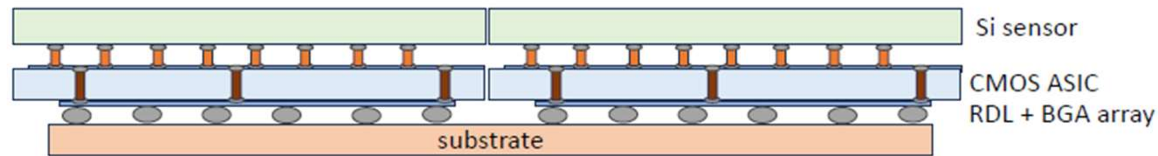


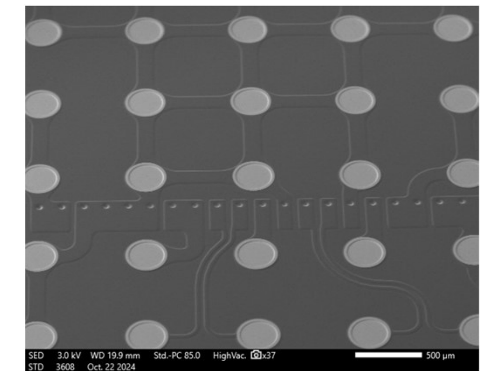
Medipix / Timepix hybrid pixel detectors

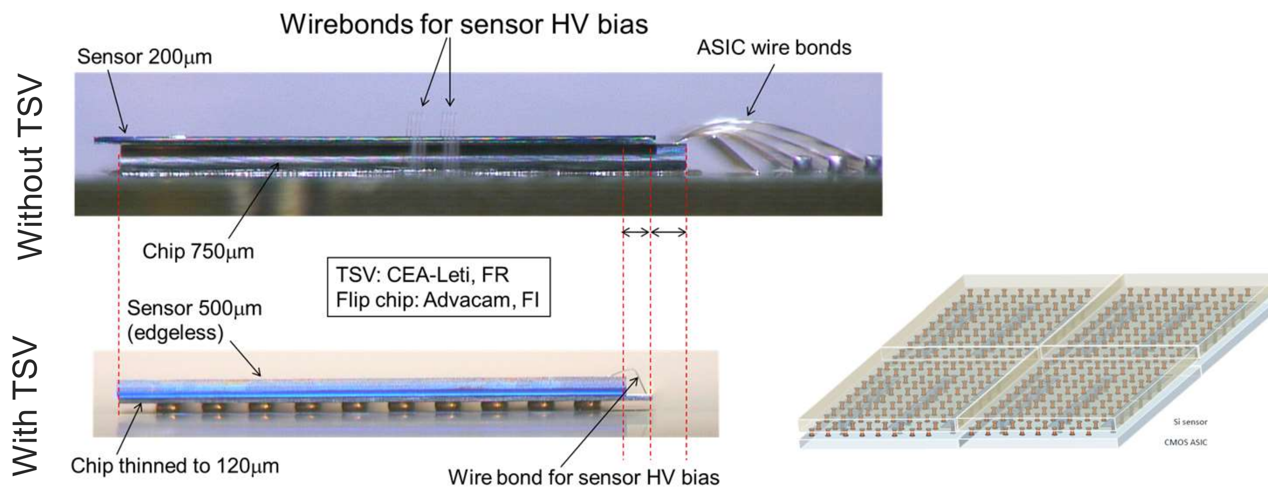
- **Abuttable detector on ROIC**
  Abuttable sensors assembly with no dead zone
  TSV last integration, 100 TSV per chip [16]
  200 mm process with 120 µm height & 60 µm diameter
  Transfer on 300 mm process targeted with 180 µm height

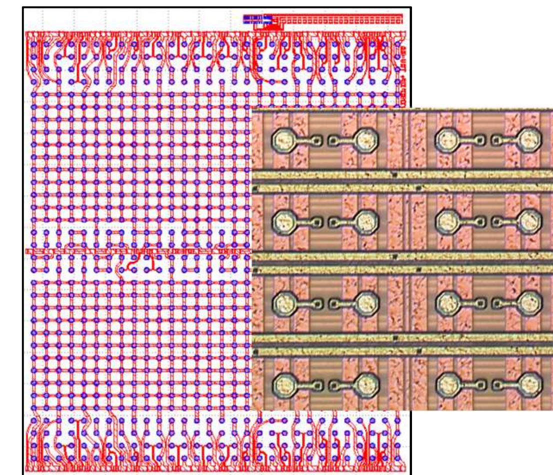
LHCb Vertex Locator



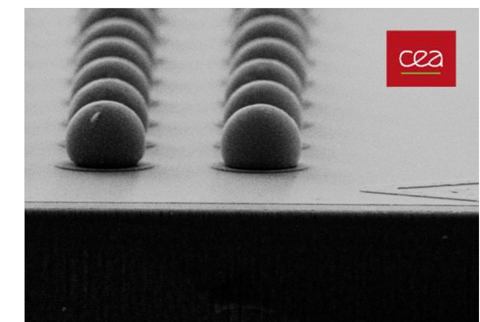








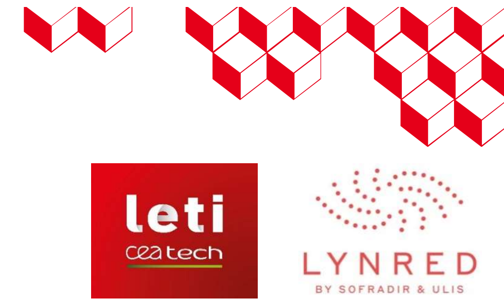
Timepix4 die 24x30mm



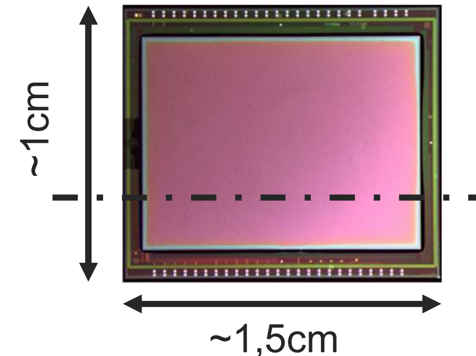
TSV & backside SEM views

[16] D. Henry et al., ECTC 2013

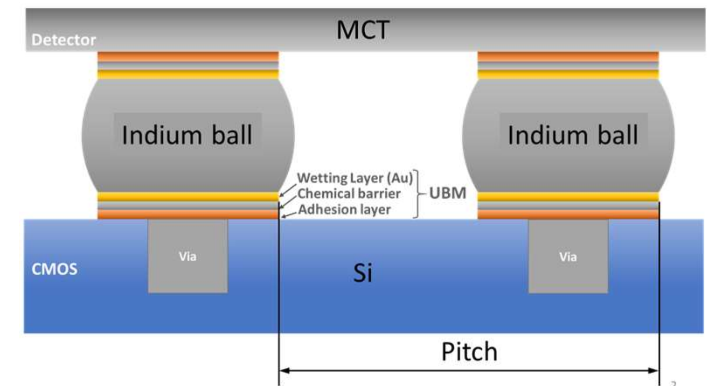
Infrared focal plane arrays integration

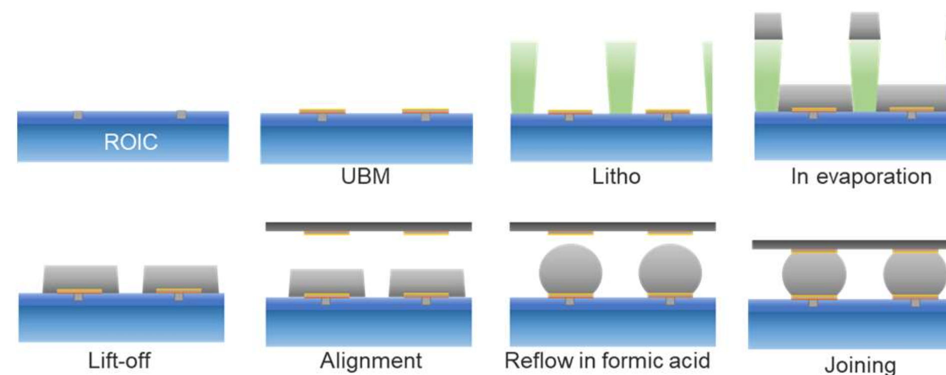


- **Infrared Focal Plane Arrays (IRFPA)**
  - II-VI or III-V detector (ex: Mercury-Cadmium-Telluride)
  - Hybridization on Read-out IC (ROIC)
  - Electrical & mechanical interconnection needed
- **In bumps interconnects**
  - Low melting point (157°C)
  - CTE mismatch accommodation
- **Miniaturization challenges [17]**
  - UBM: critical dimensions
  - Indium: cavity filling & shortcuts
  - Hybridization: misalignment
  - Hybridization: intermetallic compounds

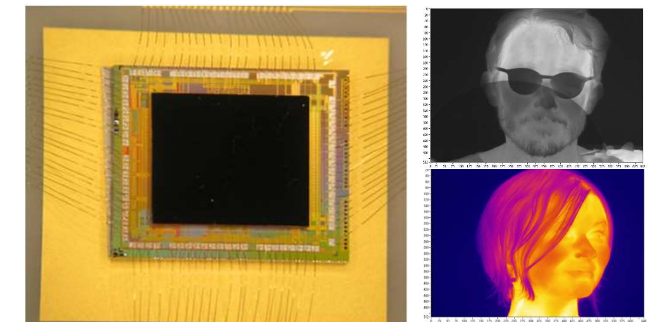


XGA (1024x768) detector at 10µm pitch





10-15µm pitch hybridization process

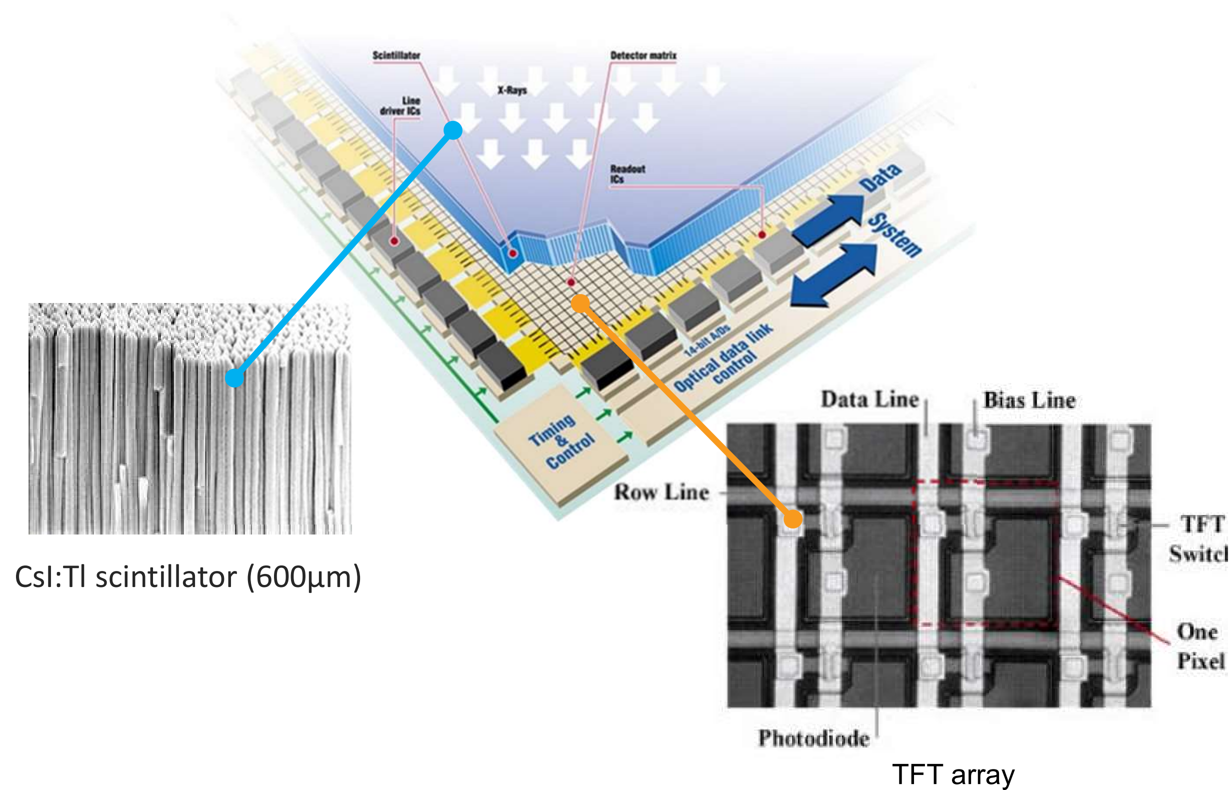


VGA (640x512) detector processed with 7.5 µm pitch [17]

[17] O. Mailliart et al., EMPC 2019

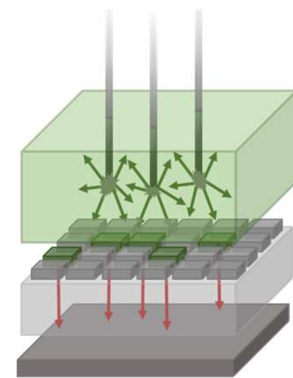
Large-area X-ray imaging

- **Flat panel**
  Scintillator: CsI:Tl scintillator (600µm)
  Active matrix with a-Si thin film transistors (TFT)
- **Challenges**
  SNR enhancement, spatial resolution improvement
  Large area (43x43 cm²), stability under irradiation
- **Directions**
  Direct detection with semiconductor instead of scintillator

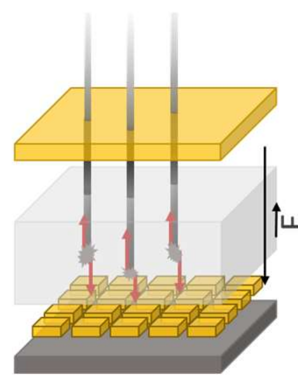


CsI:Tl scintillator (600µm)

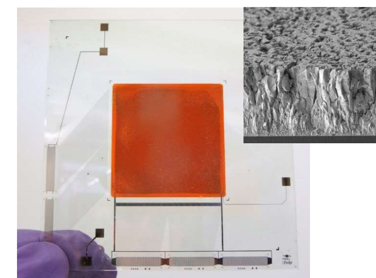
TFT array

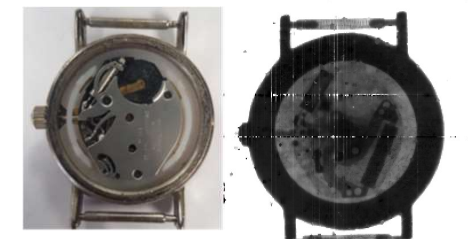


Indirect detection



Direct detection

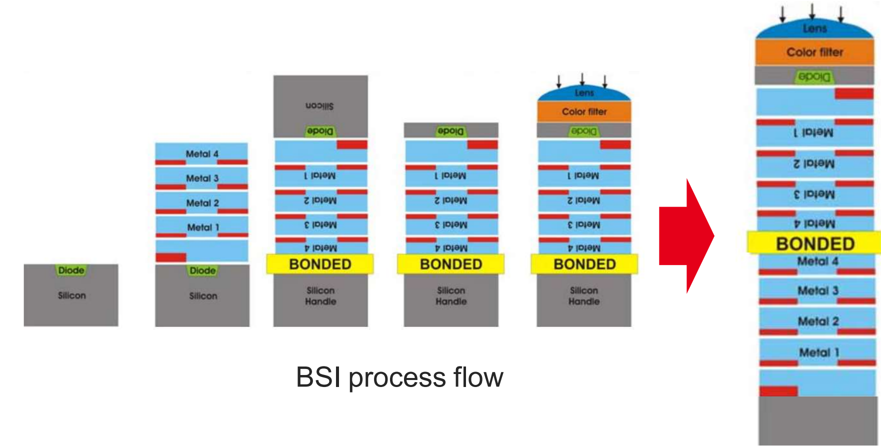




Development of low temp. perovskite-based detectors

Backside illumination as an enabler for 3D CIS

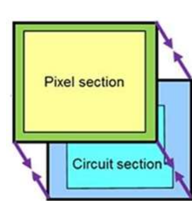
- **Backside illumination process requires wafer bonding on a carrier. There's just one step to 3D integration: replace carrier by a functional wafer!**

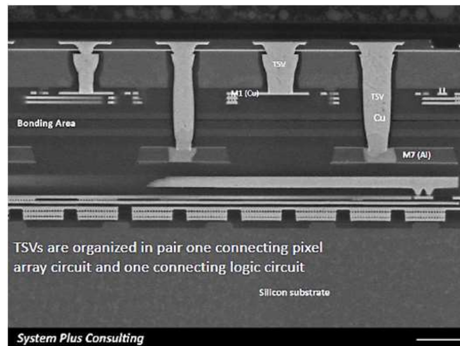


BSI process flow

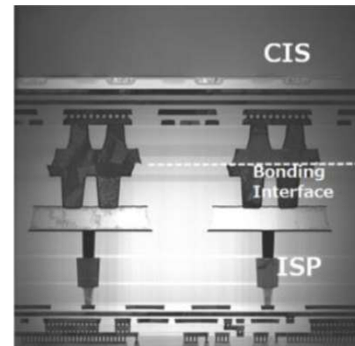
- **2-layer CIS (2013)**

Oxide bonding [18] followed by hybrid bonding [19]





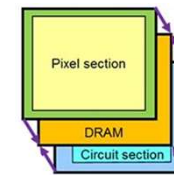
SiO2/SiO2 bonding

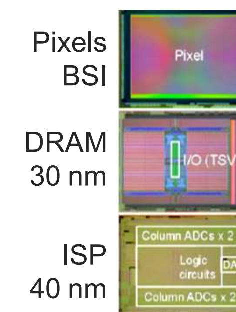


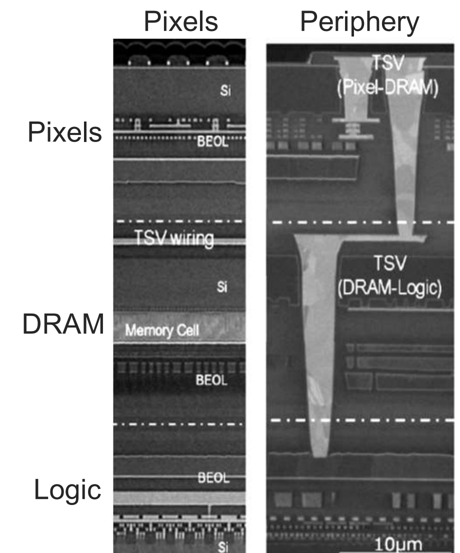
Hybrid bonding

- **3-layer CIS (2017)**

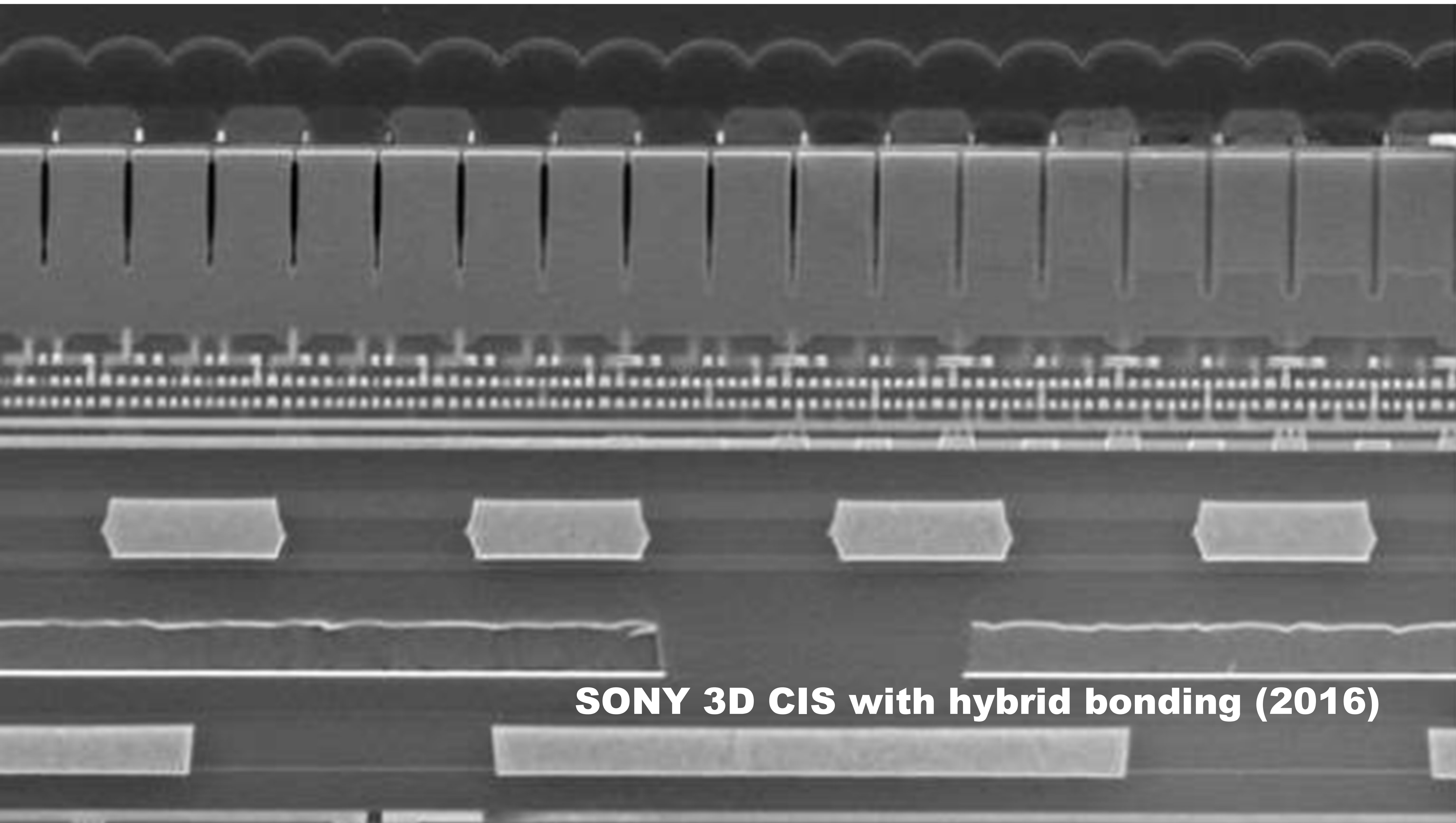
Intermediate DRAM layer [20]

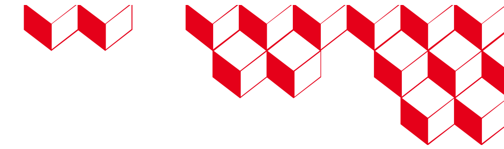






[18] Sony ISX014 1/4 Inch 8 MP, 1.12 µm Pixel Size Exmor RS Stacked Back Illuminated CIS Imager Process Review
[19] Y. Kagawa et al., IEDM, 2016
[20] H. Tsugawa et al., IEDM, 2017

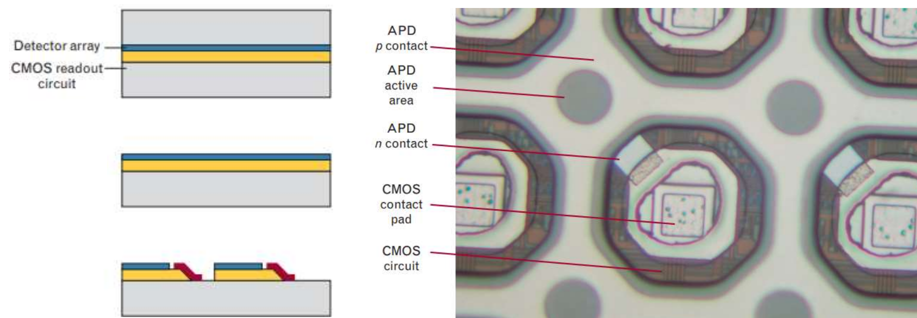

SONY 3D CIS with hybrid bonding (2016)



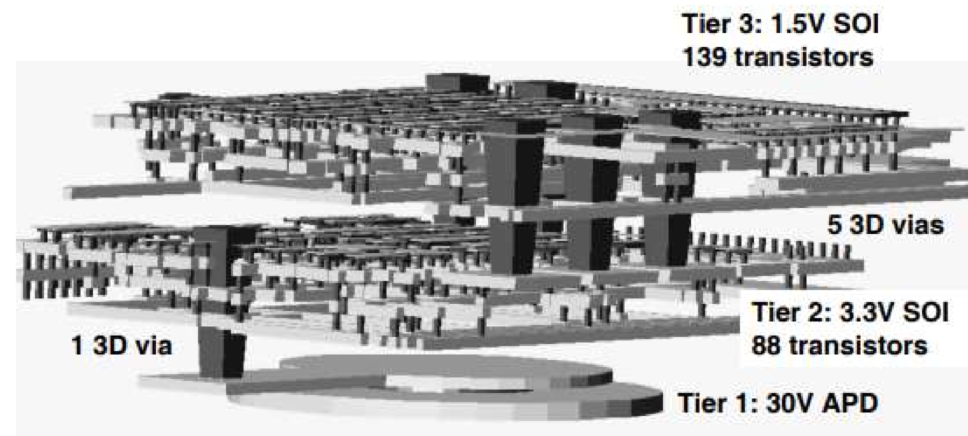
3D integration for SPAD sensors

- **Separating detection & readout**
  Layer optimization: CIS (90nm) & CMOS (22nm)
  Better sensitivity, high FF, low DCR, functionality

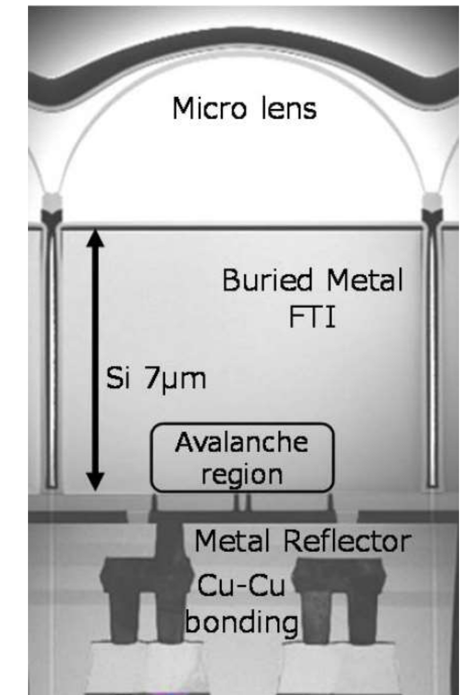
- **3D technology largely evolved over time**
  Bridges [21], oxide bonding with metal vias [22]
  Bumping, hybrid bonding [23]



32 × 32 array "bridge-bonded" APD/CMOS [21]



3D Geiger-Mode APD with Two SOI Timing Circuit Layers [22]

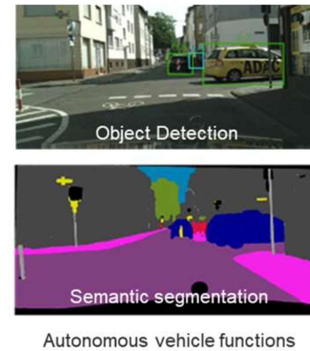


BSI 10 μm SPAD pixel with FTI & Cu-Cu bonding [23]

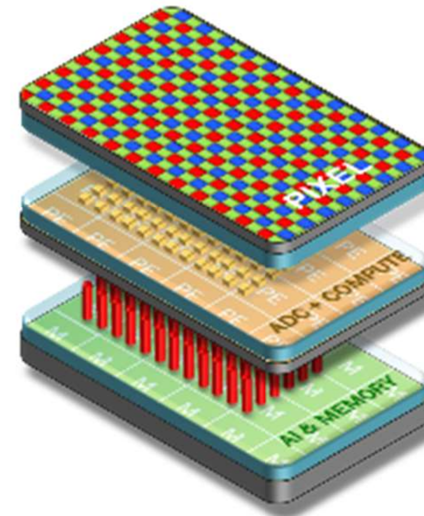
[21] B. Aull et al., Lincol Lab J.; Vol 13, no. 2, pp. 335-350, 2002
[22] B. Aull et al., ISSCC 2006
[23] K. Ito et al., IEDM 2020

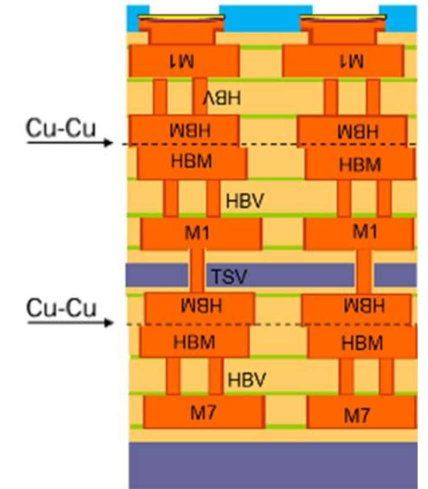
Smart imager developments

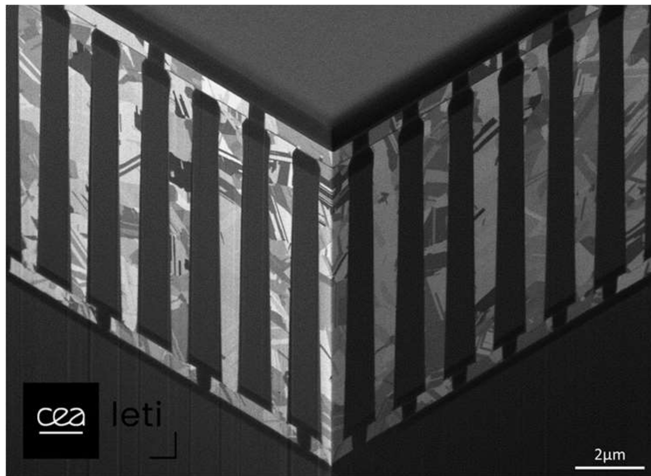
- **From imagers to vision sensors**
  Edge-AI applications for autonomous vehicle
- **3-layer scheme [24]**
  Pixel array / Readout IC / AI & memory layer
  2 hybrid bonding with 1x10µm HD-TSV



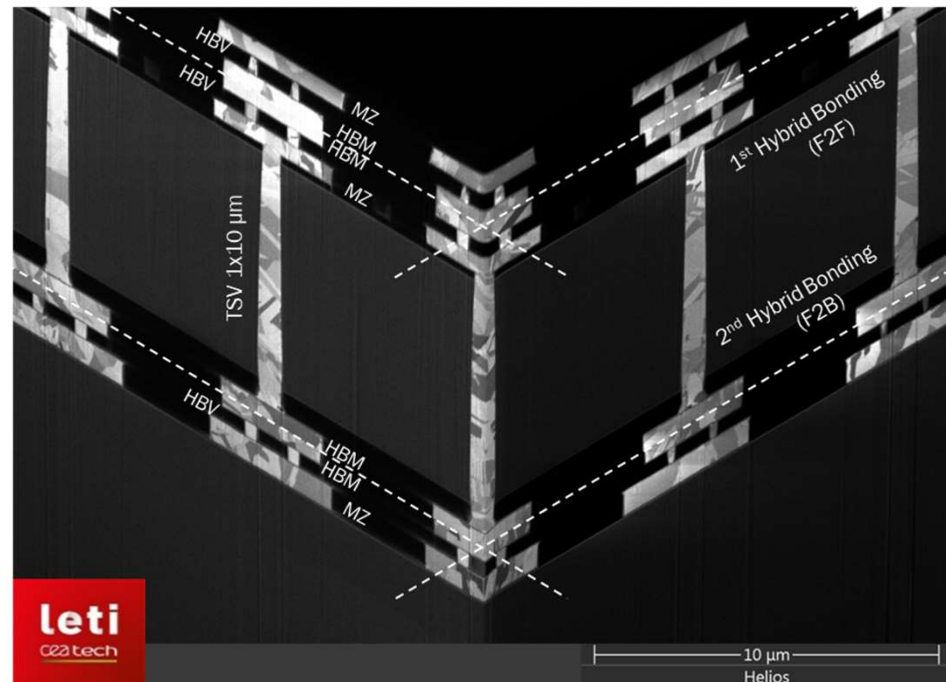
Autonomous vehicle functions



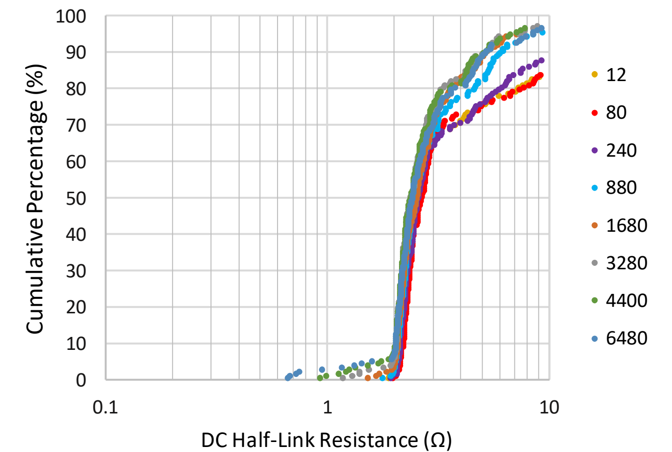




1x10µm TSV (2µm pitch), R_{TSV} = 500mΩ
Misalignment HB2: max. 1 µm (avg 200 nm)
Misalignment HB1: max. 350 nm (avg 100 nm)



Complete structure with 2 hybrid bonding and 1x10µm HD TSV [24]

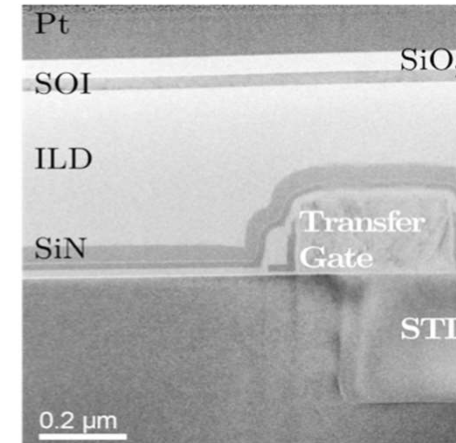


Electrical characterization of hybrid bonding/HD TSV transitions

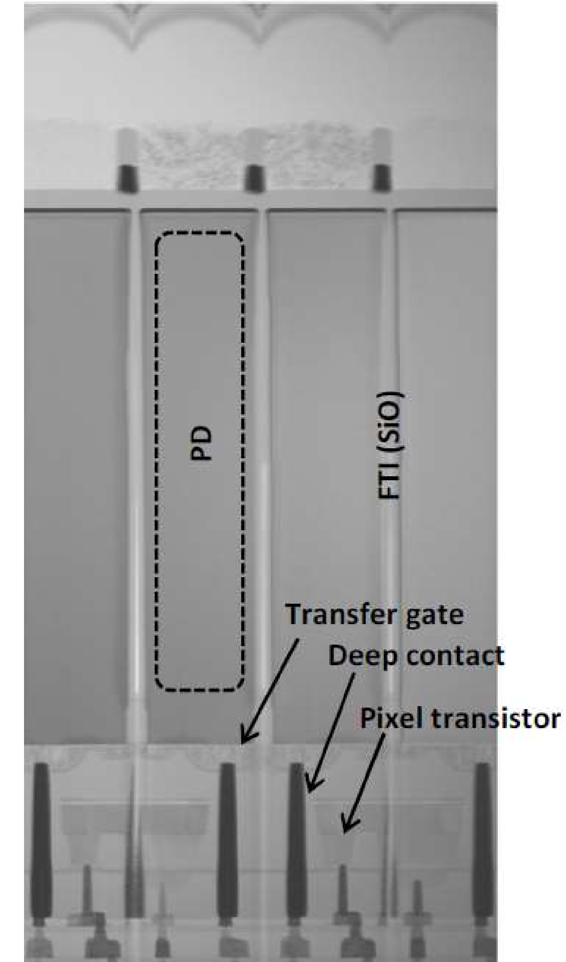
[24] S. Nicolas et al., ECTC 2024

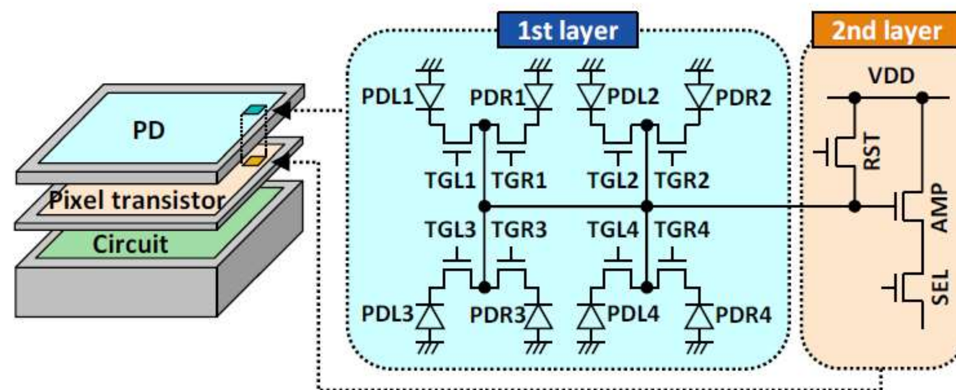
2-layer stacked 4T pixels CMOS Image Sensors

- **Pixel split for full well increase [34]**
  BSI pinned photodiode + transfer gate on layer 1
  RST, source follower & read transistors on layer 2
- **Sequential integration mandatory**
  Misalignment between layer << 1 µm
  Mono. Si transfer + low temp. CMOS process

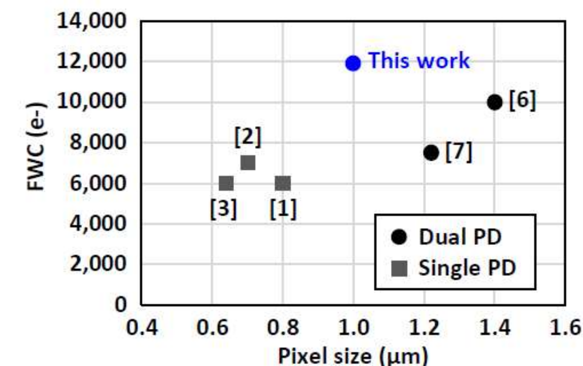


Monocristalline Si layer transfer [1]



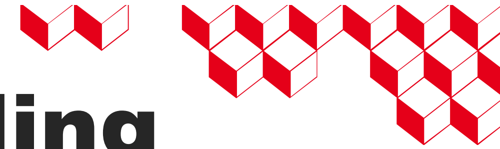


2-layer pixel schematics based on 3D sequential integration

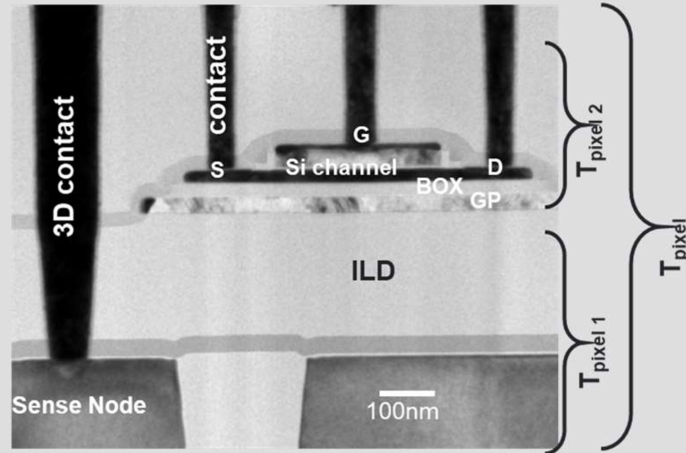


Deep photodiodes, oxide-based full trench isolation (FTI), 1µm dual photodiodes [35]

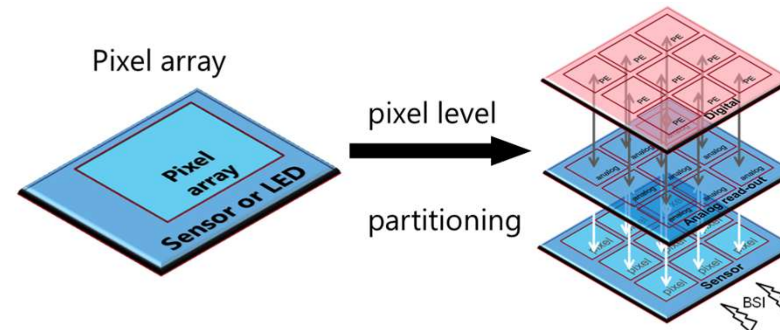
[34] P. Coudrain, IISW 2009
[35] K. Zaitsu et al., VLSI symp. on technology & circuits, 2022



Sequential 3D combined with hybrid bonding



- Sequential CMOS process
- Low temperature top level
- Nm-scale alignment between gate levels
- Applicable to heterogeneous and CMOS 3D



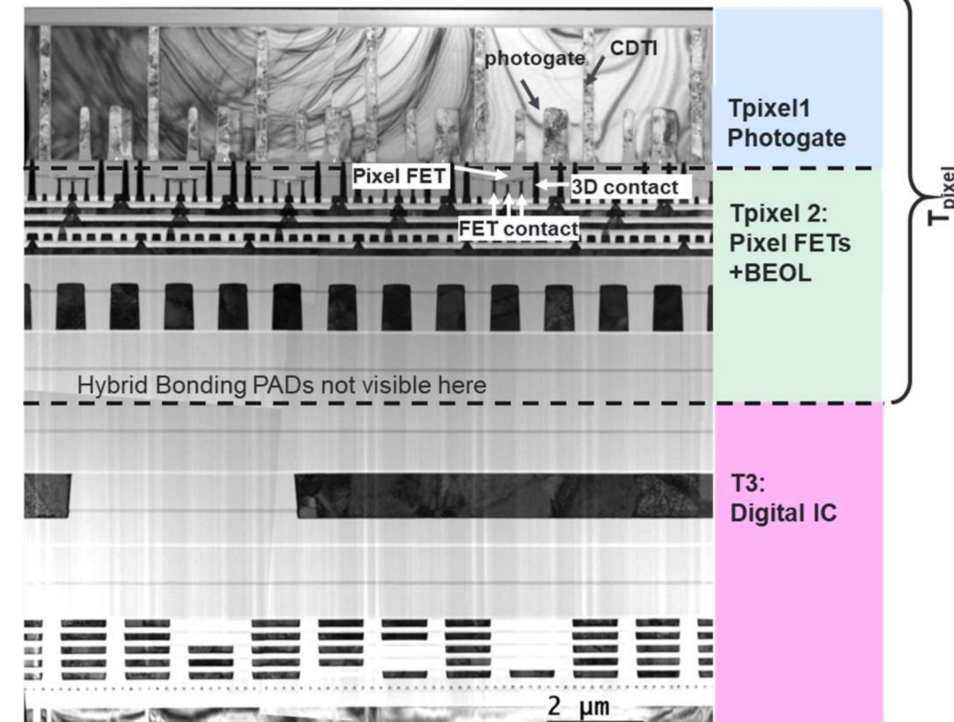
Increased diode area

44% for 1.4µm pitch

Smart pixel

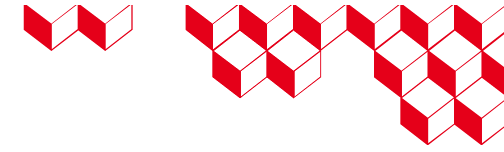
Adaptation, calibration

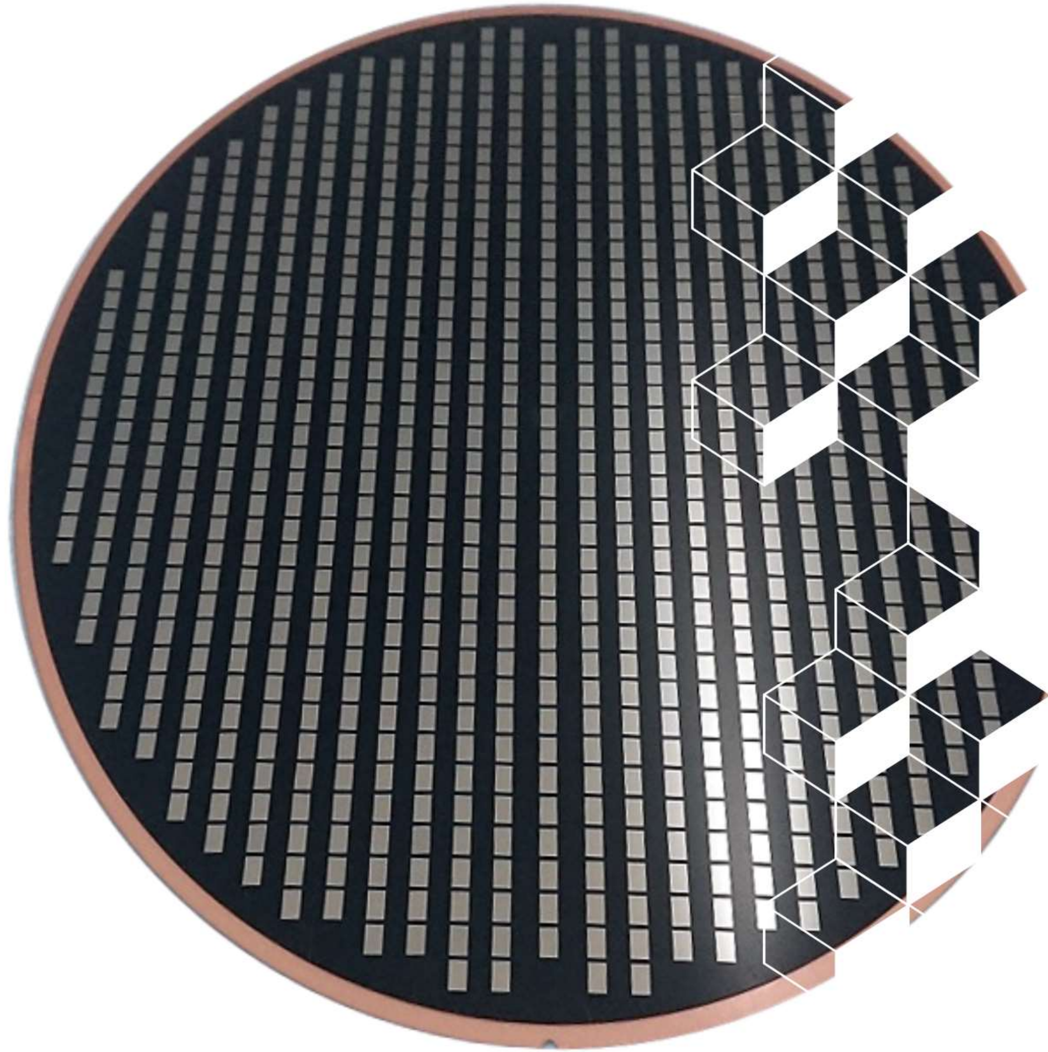
Pre-processing



Opportunity for pixel partitioning with pitch in the µm range and distributive computing for high efficiency [36]

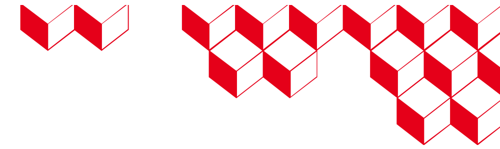
[36] F. Guayder et al., IEDM 2022





3.

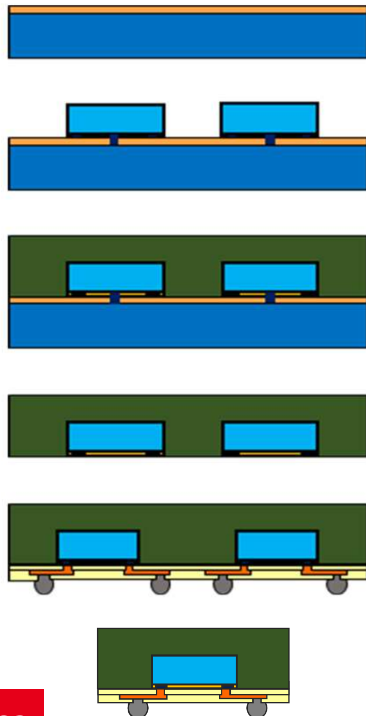
Heterogeneity with fan-out wafer level packaging (FOWLP)



FOWLP process in a nutshell

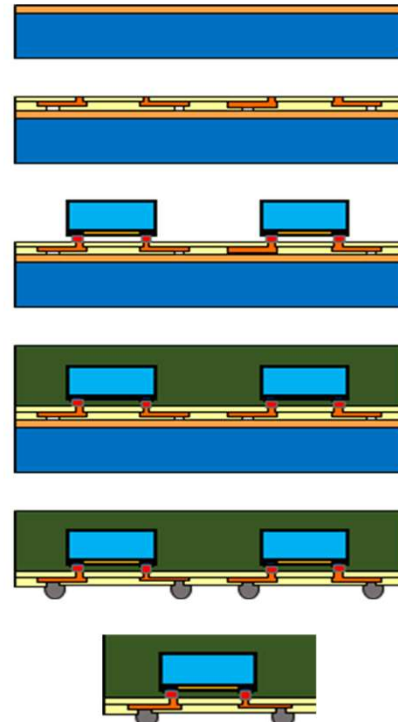
- **A multitude of integration schemes, based on <u>wafer reconstruction form individual dies</u>**

« Chip 1st »

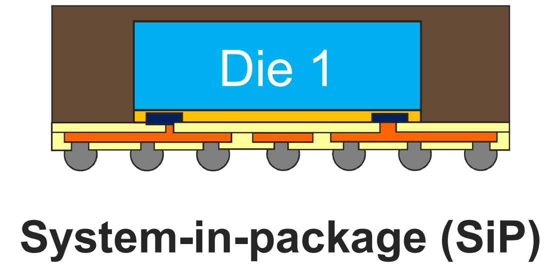


or

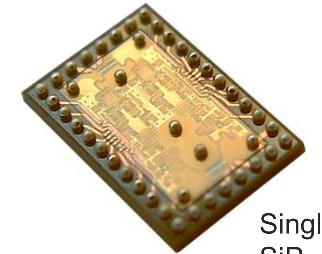
« RDL 1st »



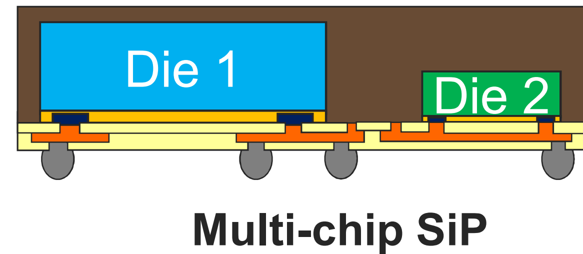
Architecture complexity



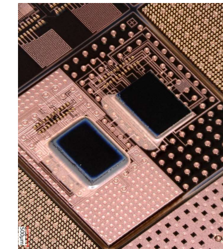
System-in-package (SiP)



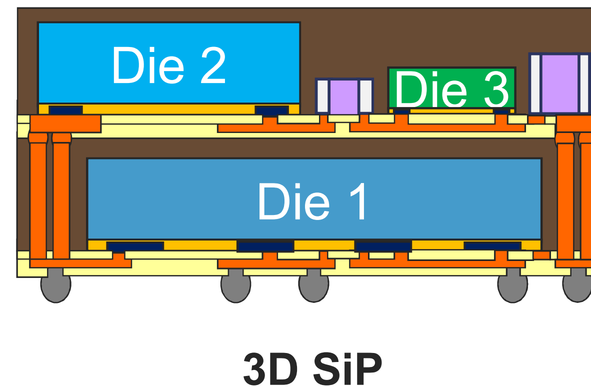
Single die SiP



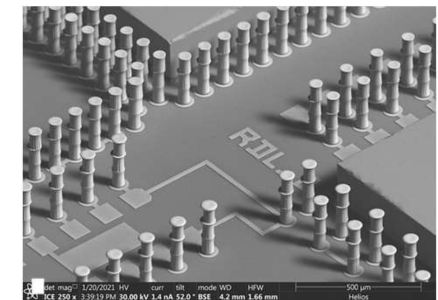
Multi-chip SiP



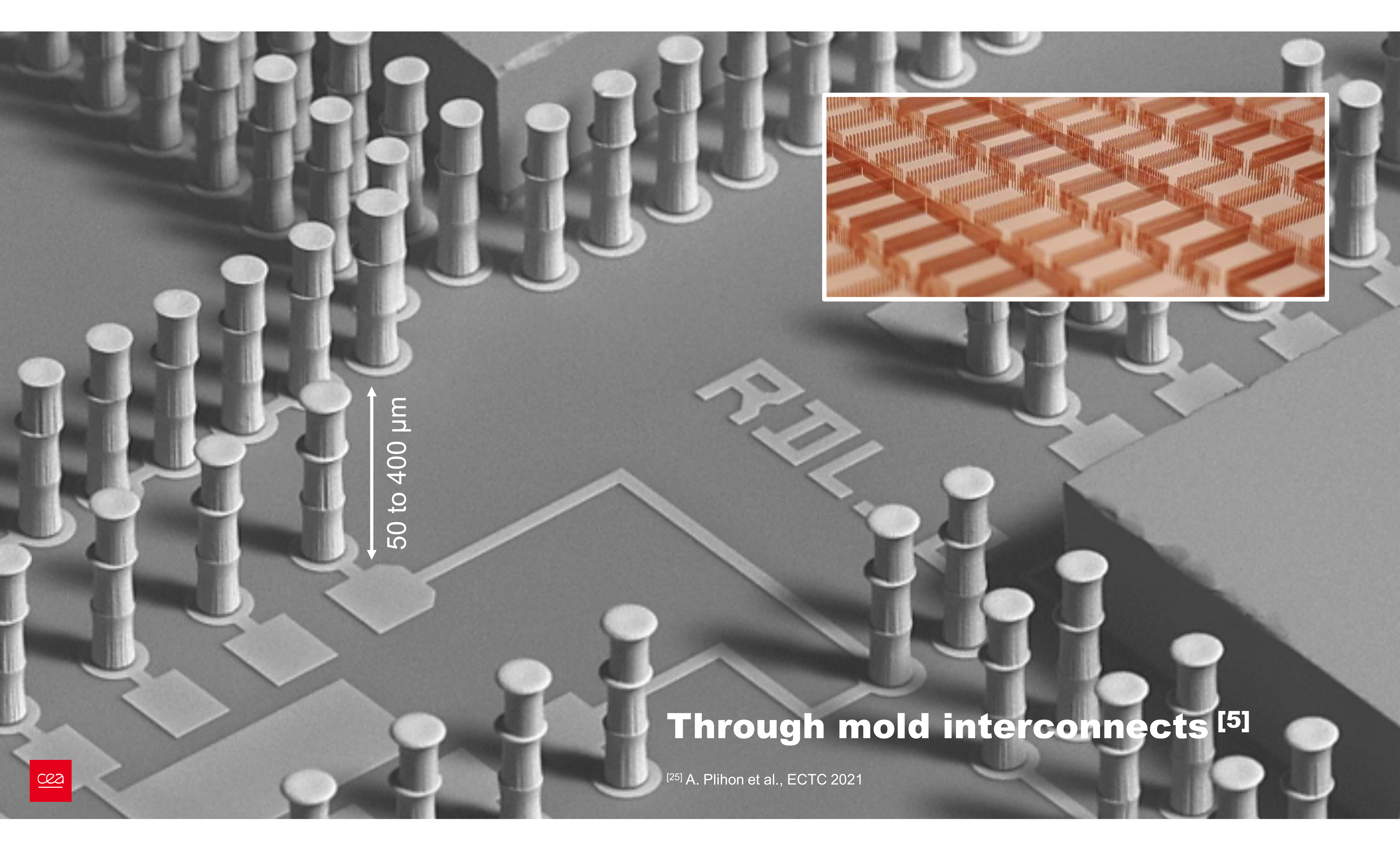
Multi-chip SiP

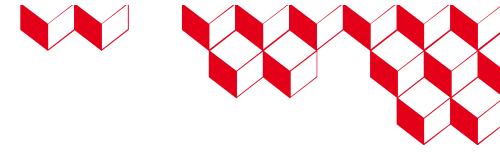


3D SiP

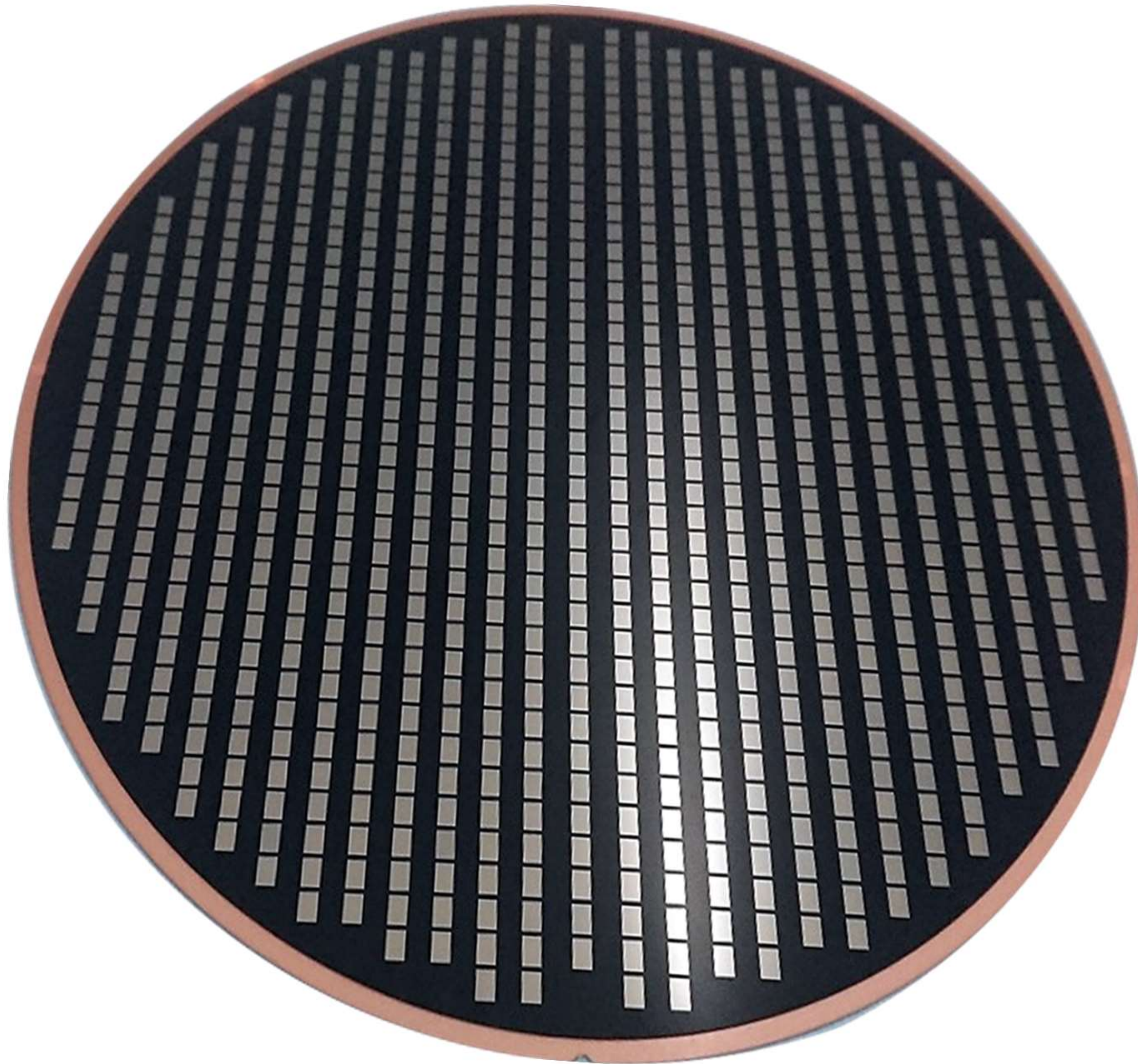


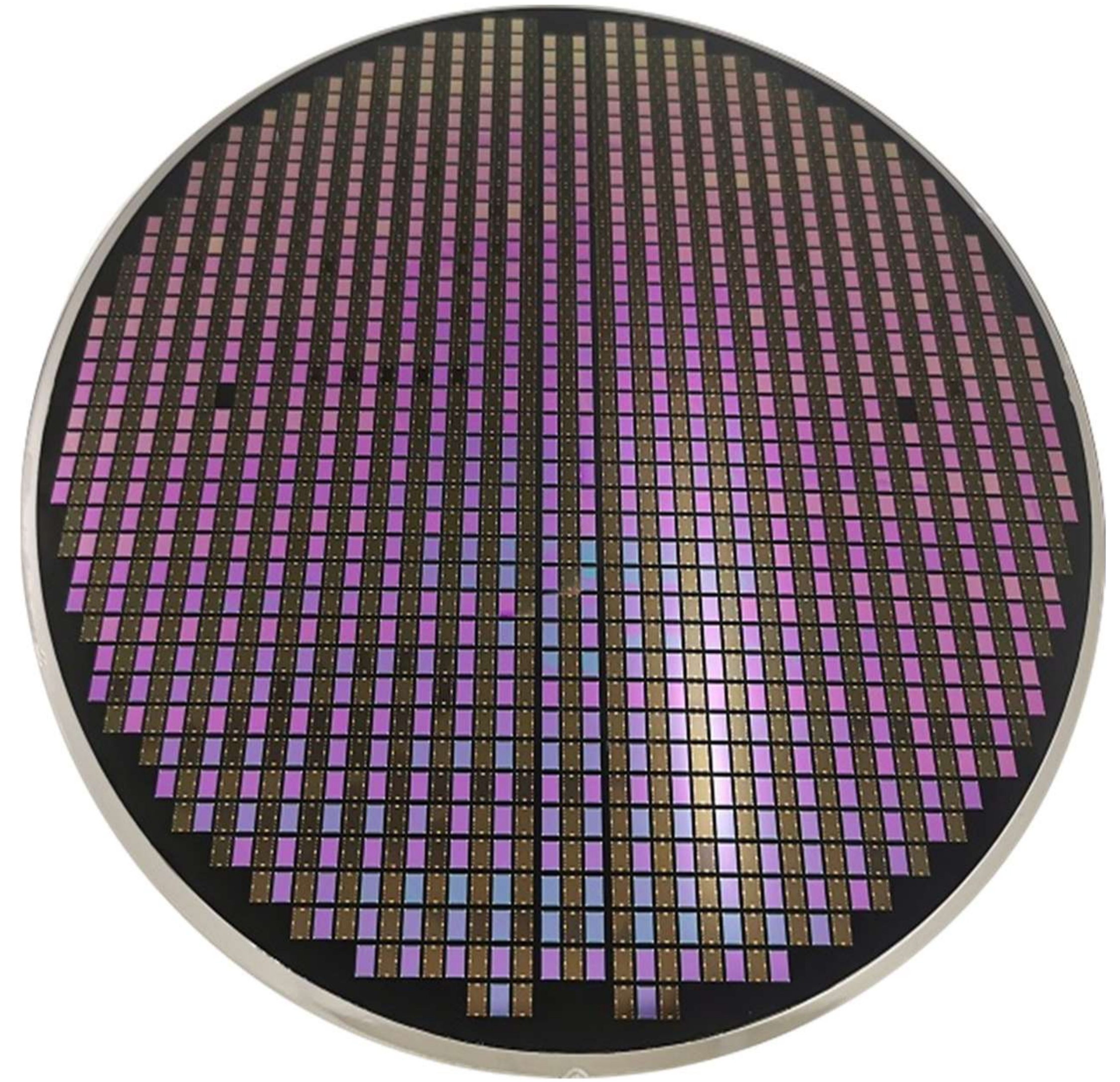
Through Mold Interconnnects

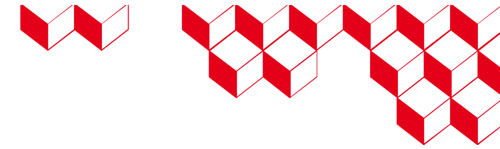

50 to 400 µm
RDL
Through mold interconnects [5]
[25] A. Plihon et al., ECTC 2021
cea



FOWLP rebuilt wafers



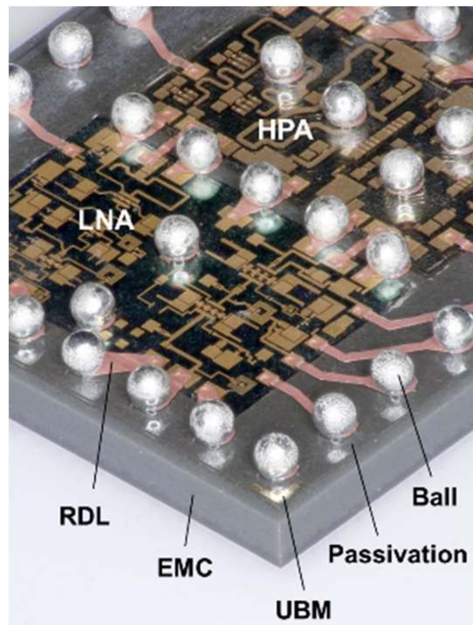


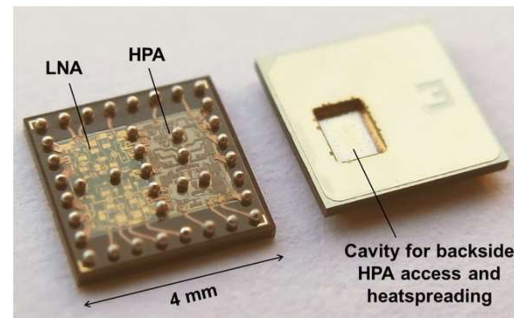


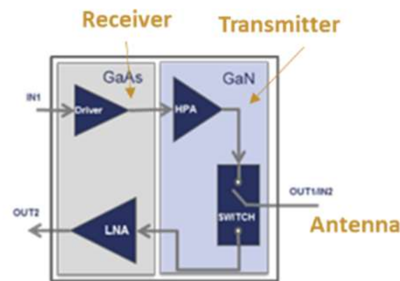
FOWLP high frequency applications

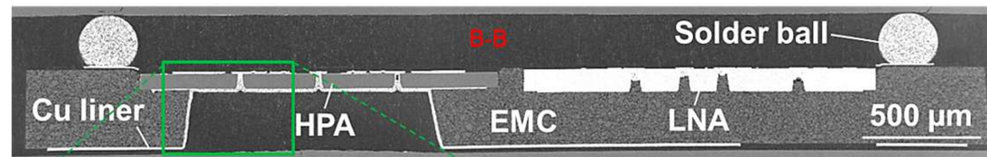
- **5G Front-End modules [26]**

GaAs (LNA) & GaN (HPA) co-integration



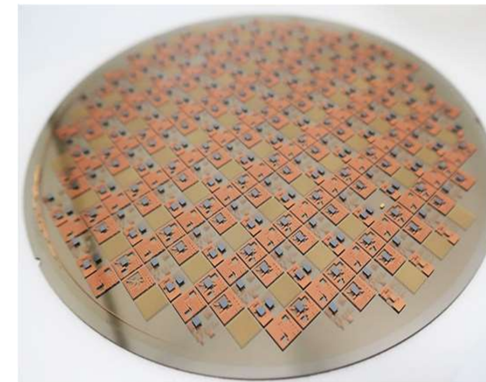


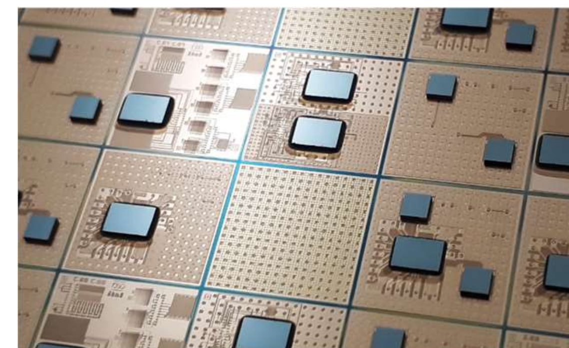




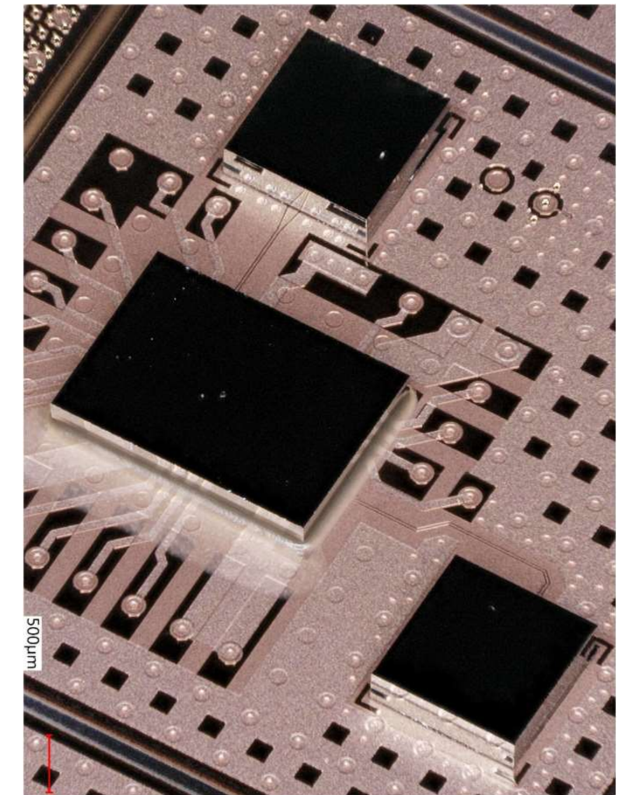
- **60 GHz radar systems**

Vital signal detection, Antenna in package



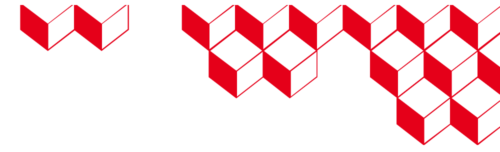


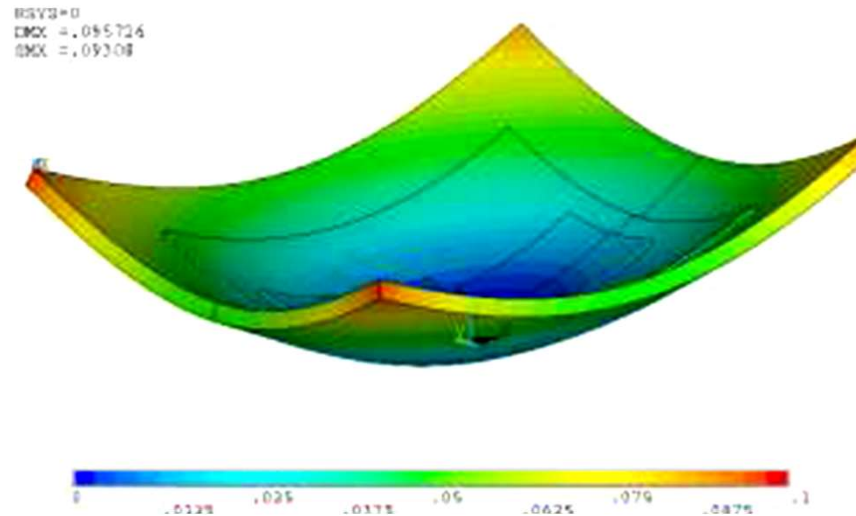
RDL 1st rebuilt wafer



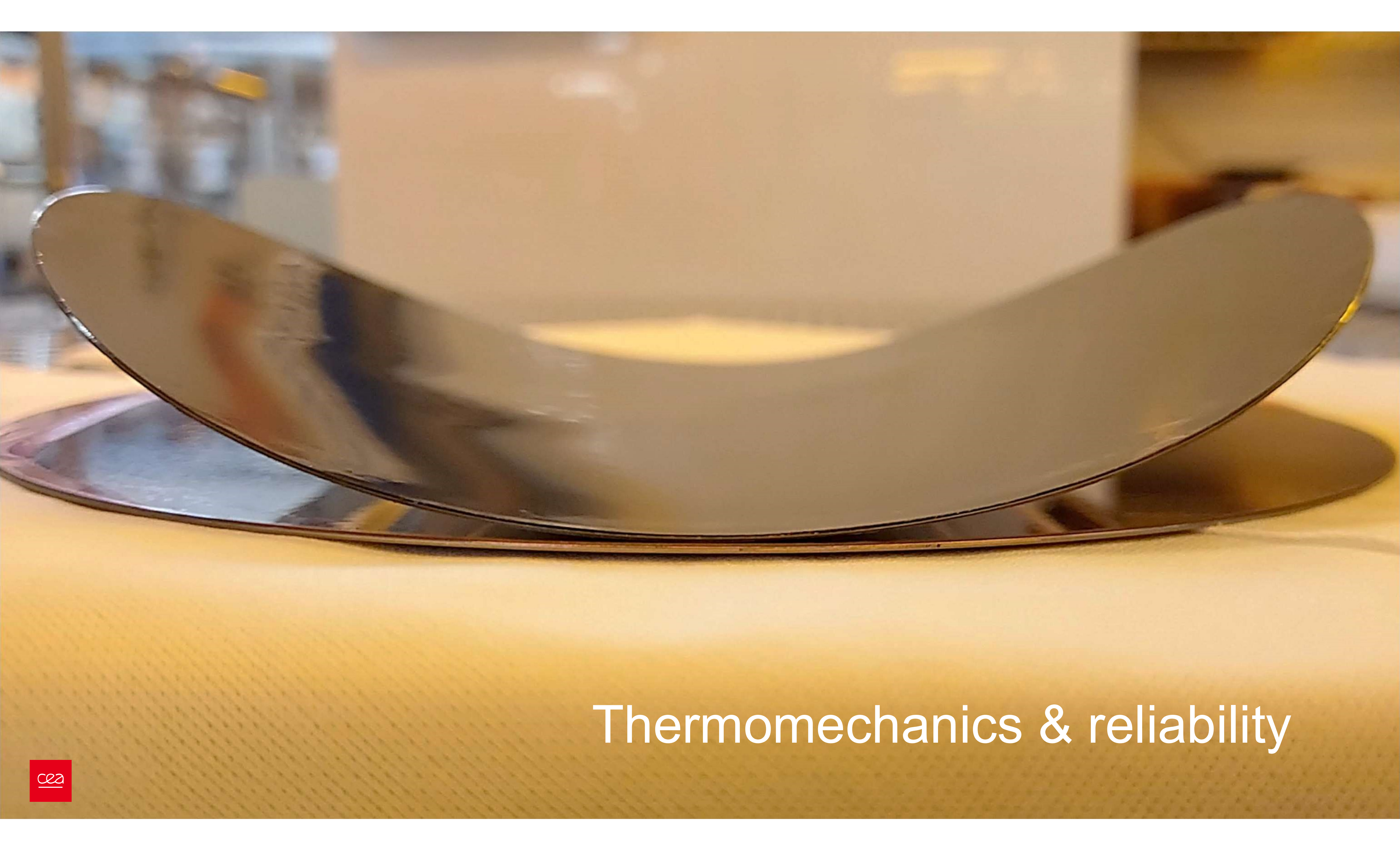
45 nm CMOS radar with dielectric radiating antennas

[26] A. Garnier et al., ECTC 2021



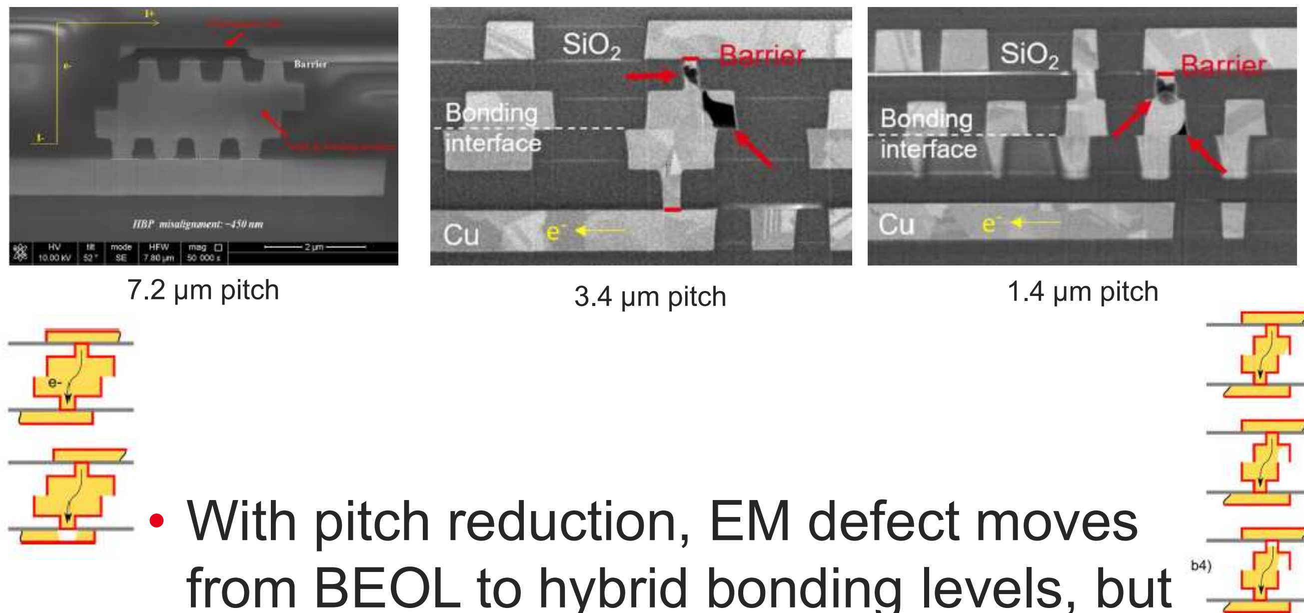


Integration challenges
(a few words)


Thermomechanics & reliability
cea

Extensive reliability studies on hybrid bonding

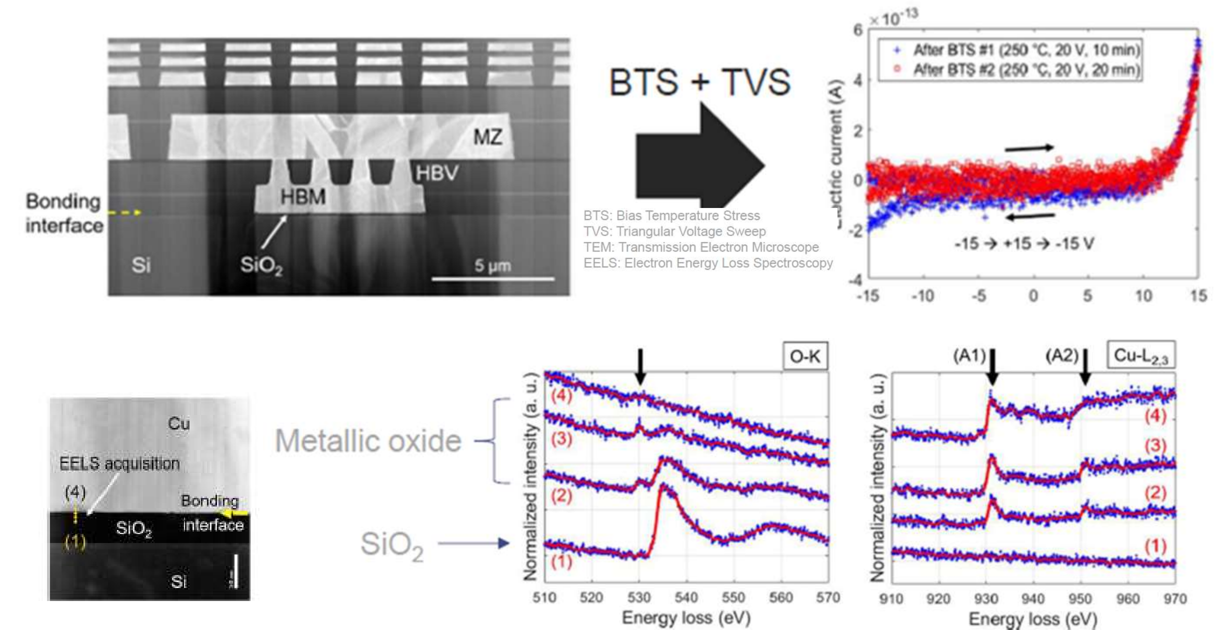
Electromigration performance vs. pitch reduction



- With pitch reduction, EM defect moves from BEOL to hybrid bonding levels, but **extrapolated lifetimes are not affected at use conditions [27]**

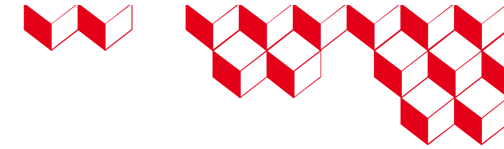
[27] S. Moreau et al., IRPS 2023

Susceptibility to Cu diffusion ?

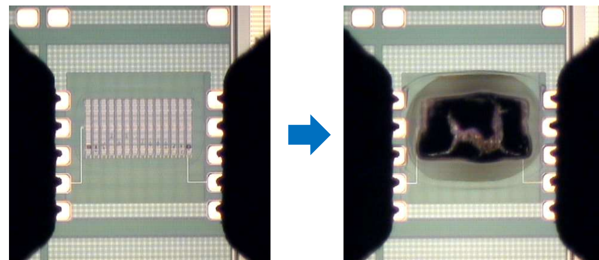


- **No diffusion identified**, thanks to the presence of 3 nm Cu_2O layer barrier, stable with time and temperature [28]

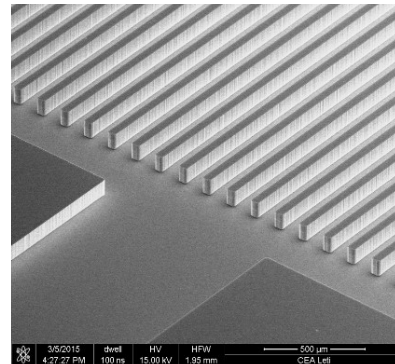
[28] Ayoub et al., Micro rel. 2023

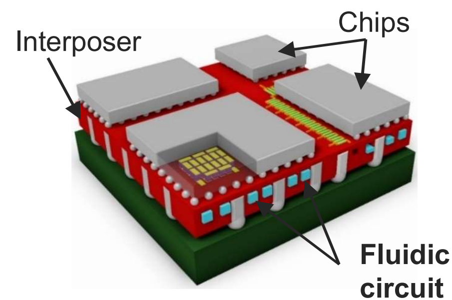


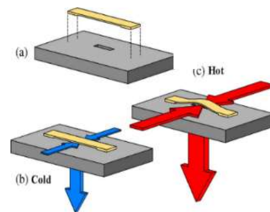
Thermal dissipation

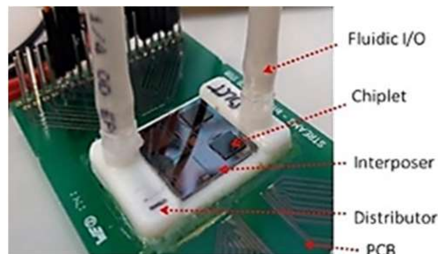


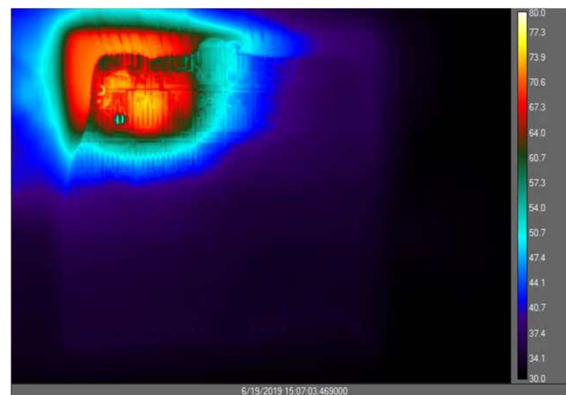
RF switch on SOI





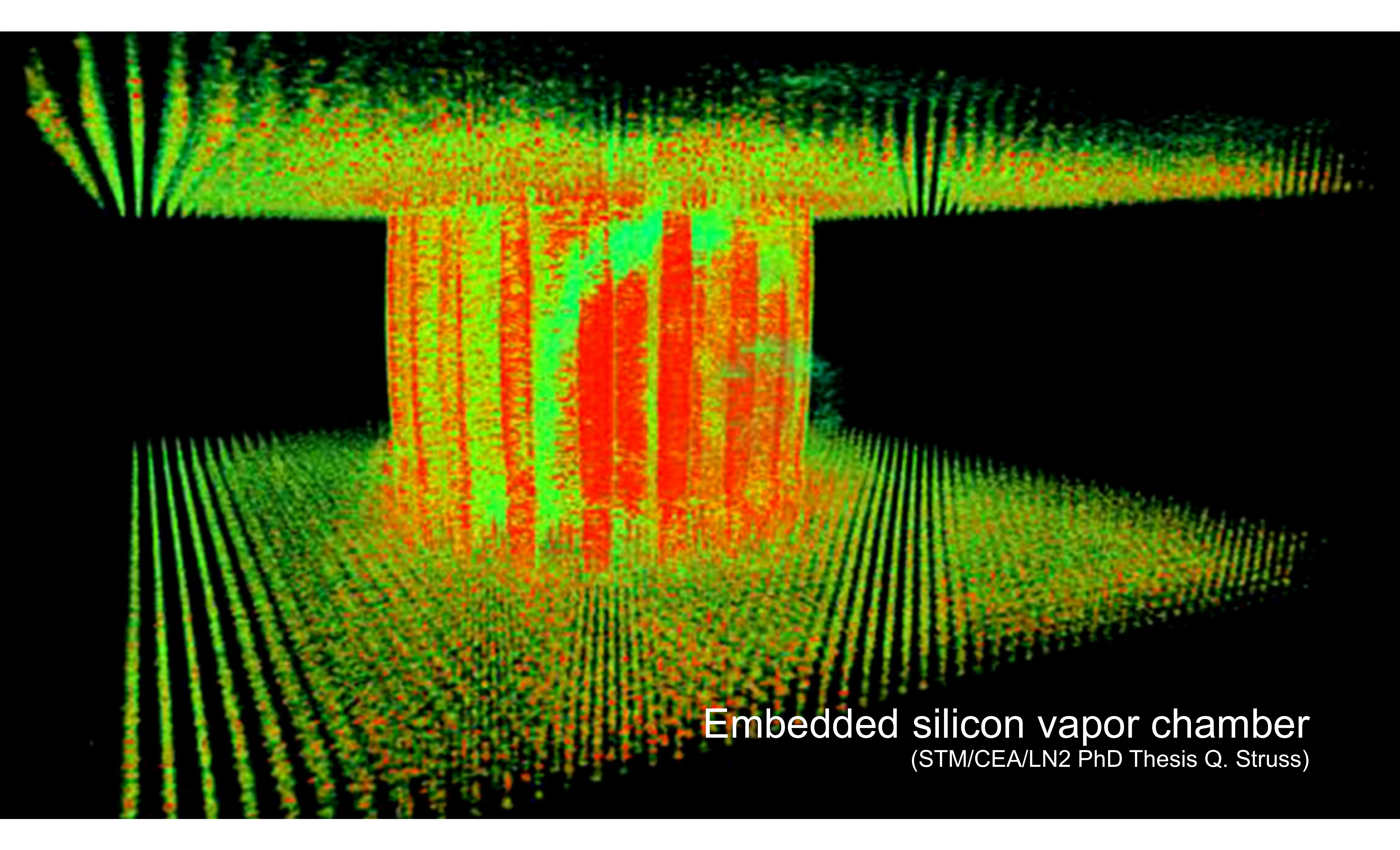






Microfluidics cooling with self-adaptive network for efficient high performance cooling (CEA, Sherbrooke University, ST)

- **Dense integration at all scales brings real challenges in terms of heat dissipation**
- **Thermal modelling essential from the earliest design phases for IC & SiP**
- **Efficient heat extraction methods become a necessity**
- **Integration at wafer scale will become a key objective**


Embedded silicon vapor chamber
(STM/CEA/LN2 PhD Thesis Q. Struss)

Take-home messages

- **3D integration & advanced packaging have become strong drivers of innovation in electronics**

  3D & advanced packaging approaches were able to overcome some of Moore's law issues and answer design needs

  Image sensors clearly played a pioneering role in the advent of 3D integration

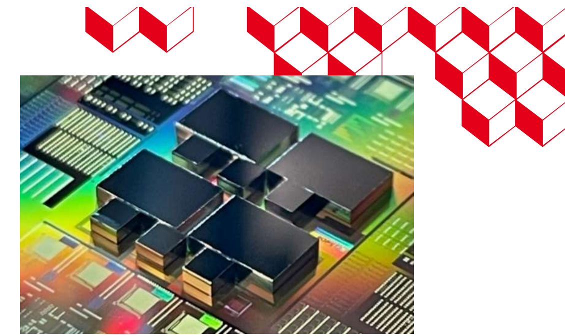
- **It is conceivable that any heterogeneous architecture can now be realized in one way or another, but…**

  Cost-performance trade-off, timely development

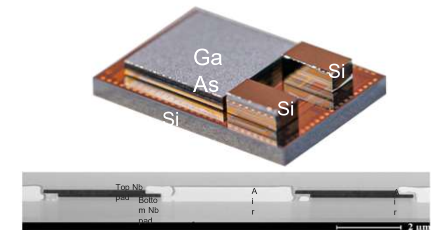
  Standardization & efficiency, ecological impact !

  → still very much in the spotlight

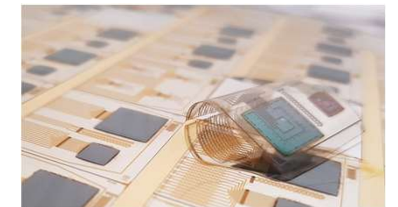
- **Designers are often not fully aware of the 3D toolbox capability → come & discuss!**



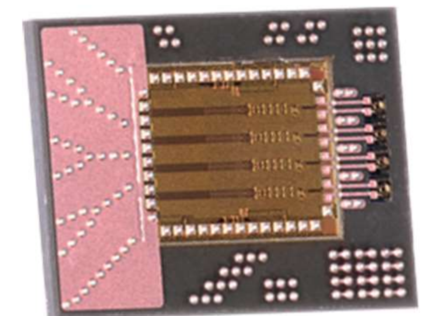
Electronic chiplets on photonic interposer



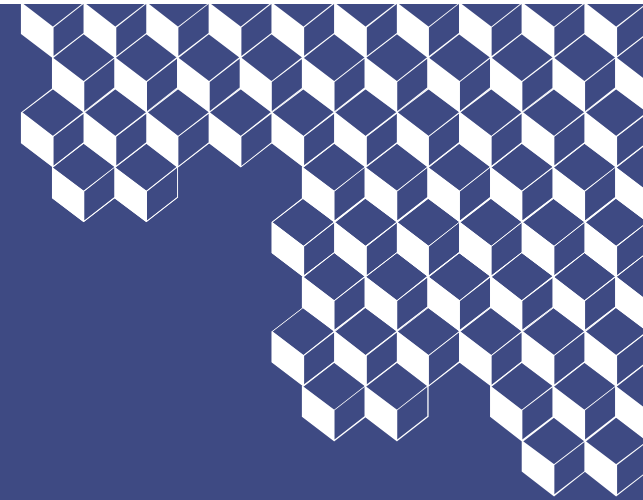
Superconducting Nb/Nb bonding for quantum interposers



Flexible heterogeneous SiP

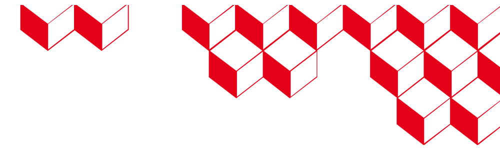


Optical transceiver



Thanks for your attention

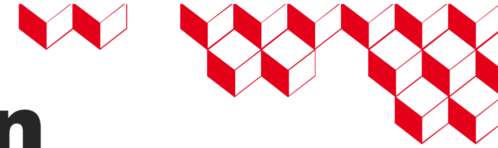
CEA-Leti, Grenoble, France
cea-leti.com
perceval.coudrain@cea.fr



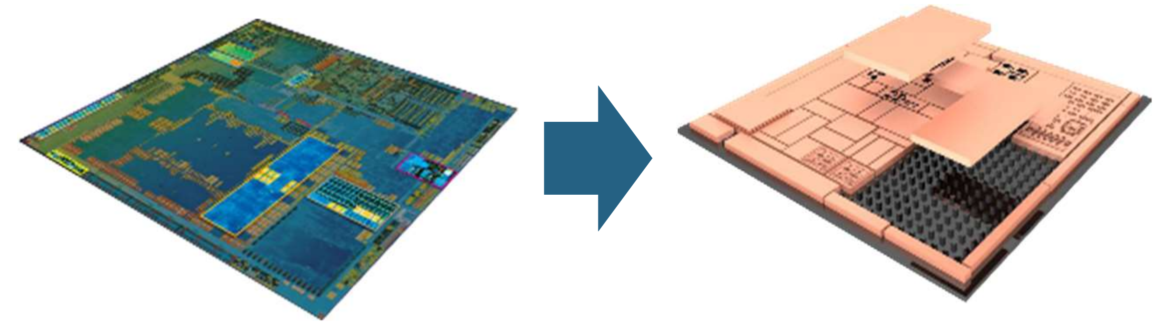
3.

Other fields benefiting from 3D architectures

Chiplet approach: Heterogenous IC design



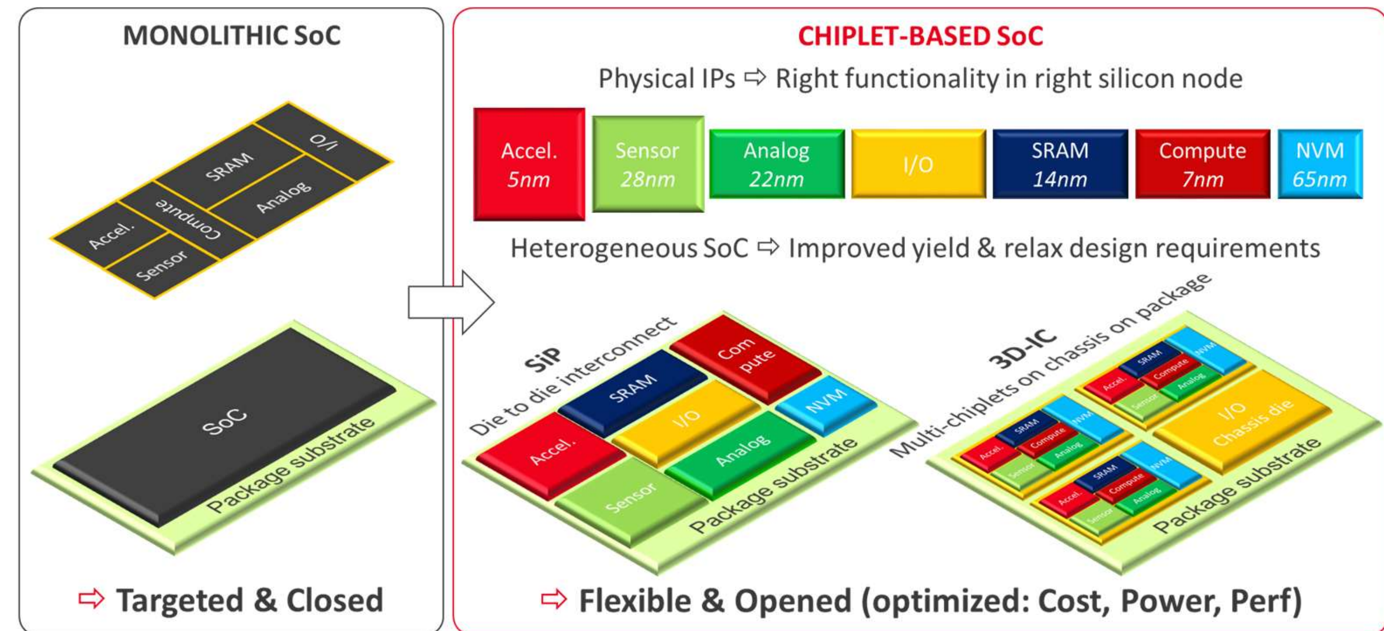
- **Interposer & chiplets**
  Interconnects performance → R.C delay
  Exceeding latency & bandwidth limits
  Cost/form factor advantages

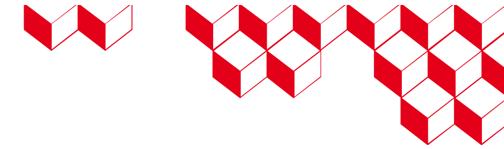


The end of "all for the SoC" paradigm (image from DARPA)

- **Appropriate partitioning**

- **Heterogeneous IC design**
  Optimized technology for each function
  specialization by app.: CPU, GPU, AI (...)
  Standardization (coming soon, hopefully)

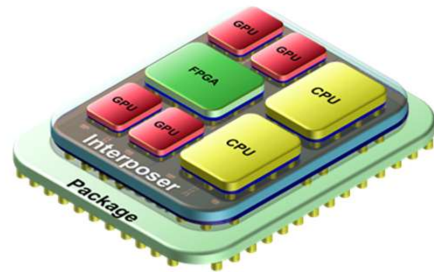




Trendy R&D fields for interposers

- ## Active interposers

Interconnect performance, power management, network on chip…



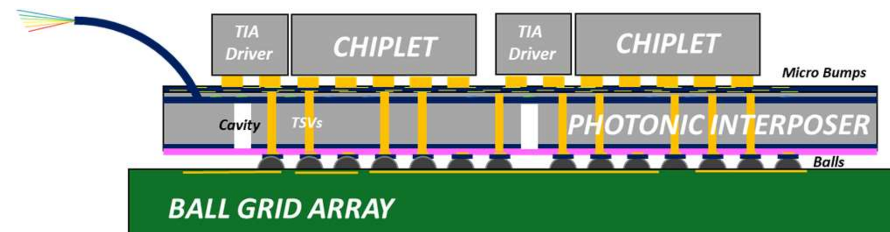
Chiplet on interposer topology

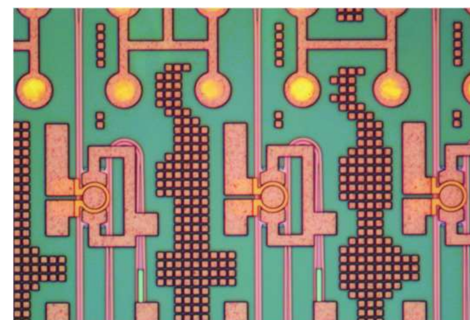
INTACT active interposer [37]

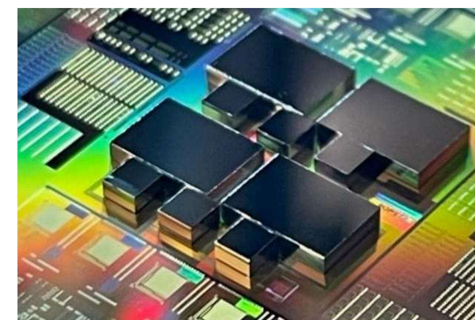
- **Chiplets 28nm FDSOI** 6x22mm²
- **Interposer 65nm** 200mm²

- ## Photonic interposers [38]

Reduced on-chip latencies & energy consumption, increased bandwidth

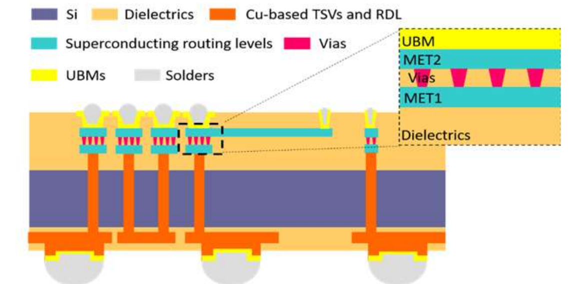


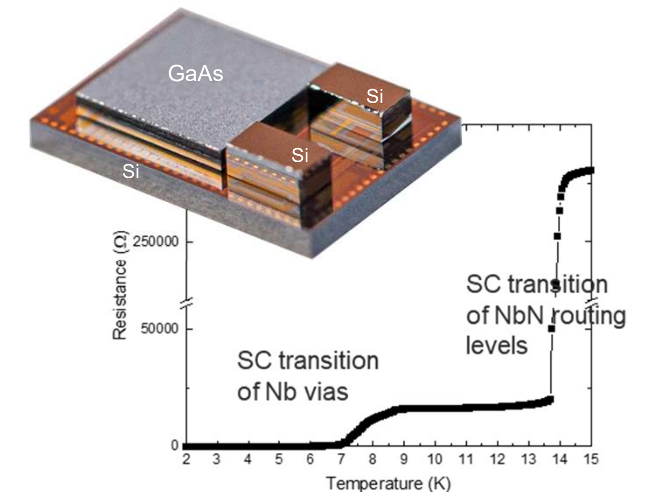

TSV mid (12x100µm) co-integraton with µ-ring resonators after Metal 1


Silicon Photonic Interposer with 4 chiplets and 6 electro-optical drivers in 28nm FD-SOI

- ## Quantum interposers [39]

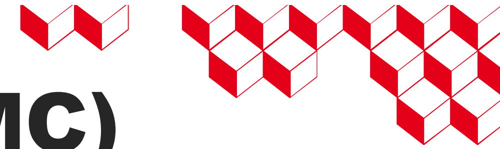
Superconducting routing





Superconducting interconnect assessment

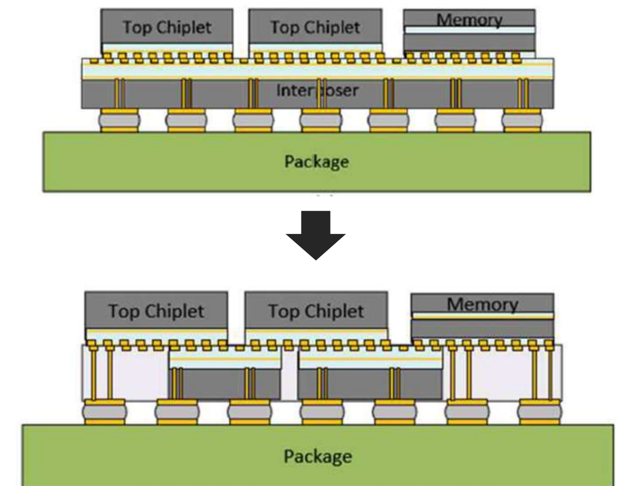
[37] P. Coudrain et al., ECTC 2019
[38] D. Saint-Patrice, ECTC 2023
[39] C. Thomas et al., Materials for Quantum Technology, 2, 3, 035001, (2022)



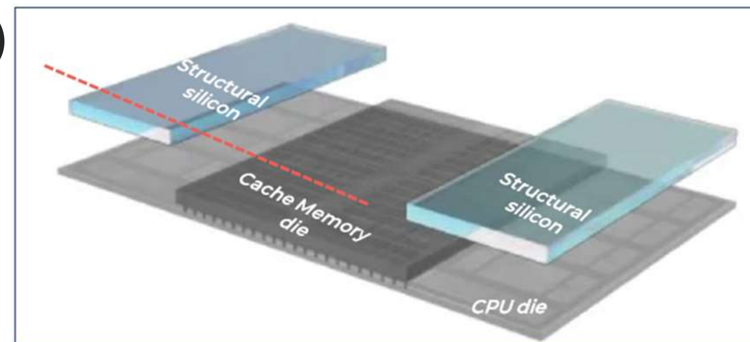
New generation of quasi-monolithic chips (QMC)

- **Flexible combinations of Si process & packaging techniques for ultra-high density 3D architectures to fit future computing & AI needs**

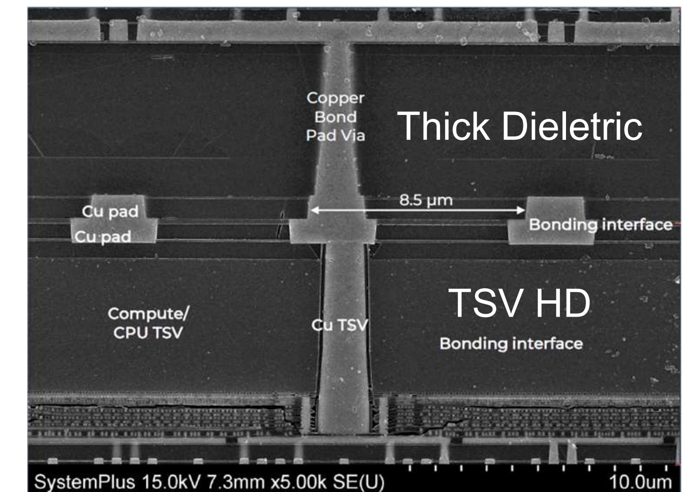
- **Intel (2022) [54]**
  Enabling Next Generation 3D Heterogeneous Integration Architectures on Intel Process
  Interposer replaced by a chiplets layer filled with dielectric
  Through dielectric vias (TDV)



- **AMD Ryzen with v cache (2022)**
  10X interconnect power reduction
  high density back-end compatible



AMD V-Cache components
©2022 by YOLE SystemPlus



[54] A. Elsherbini *et al.*, IEDM 2022