Quantum Computing/Sensing: Are Cryo-CMOS Circuits Essential?

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EPFL

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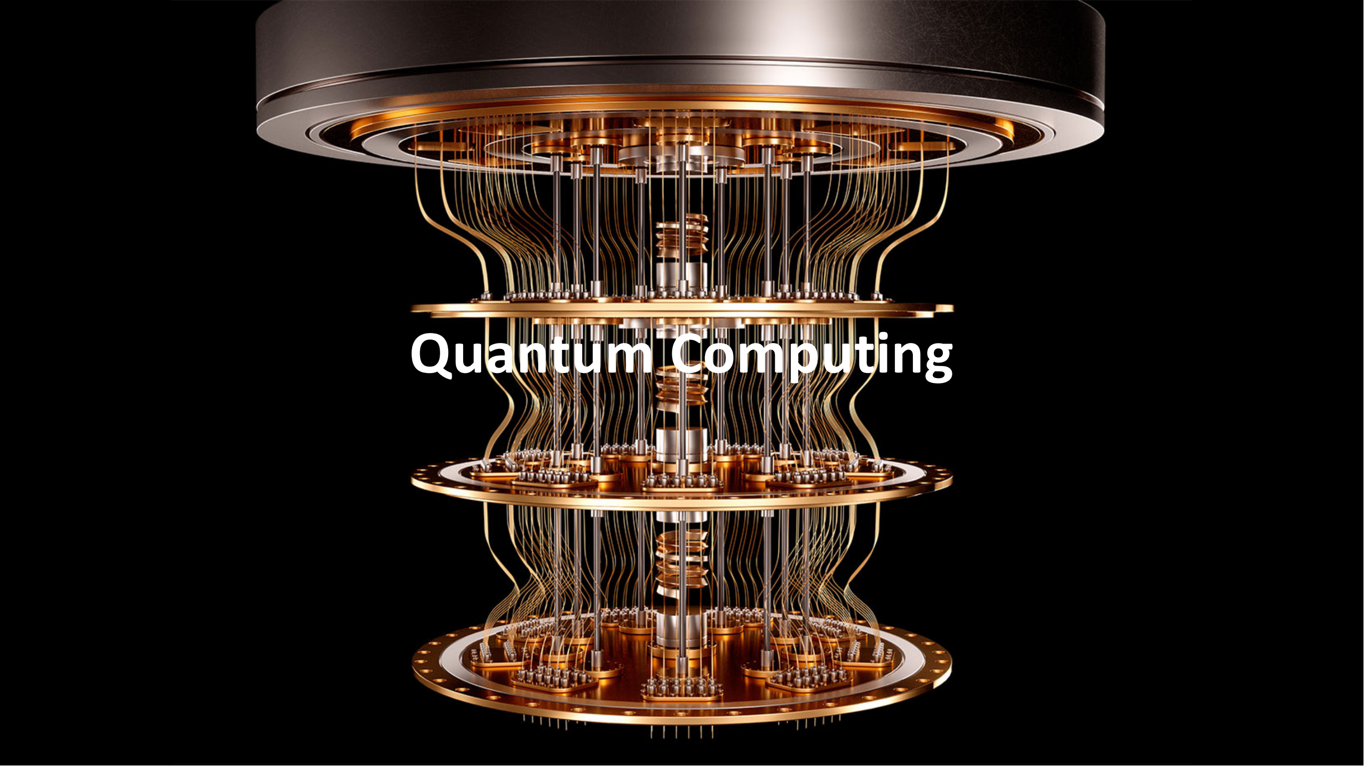
AIDAinnova training course on quantum applications

AIDA innova

Outline

- Quantum computing
- Quantum sensing / quantum imaging
- Why cryogenic electronics?
- The design of a qubit controller
- Perspectives


Quantum Computing

Principle, again

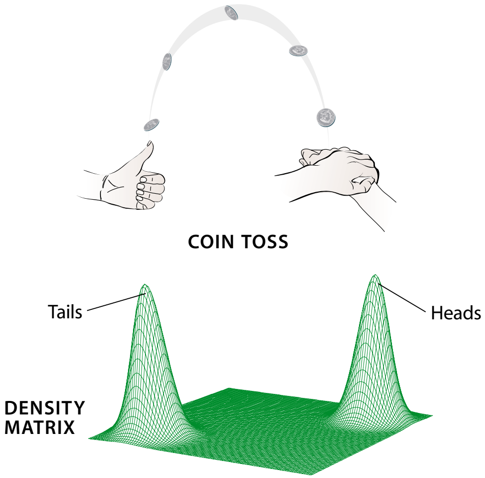
- Proposal to use of **entanglement**, **superposition** and **quantum interference** for computation
- Fundamentals and theory developed in the 1980-2000

There is plenty of space at the bottom

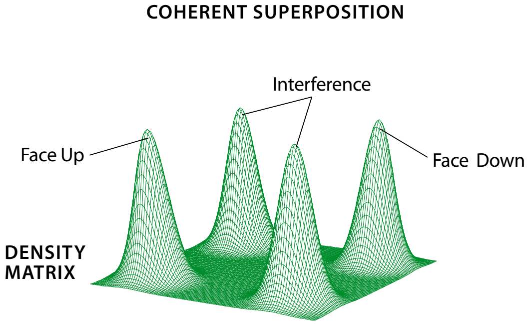
- Richard Feynman

Superposition, again

CLASSICAL UNCERTAINTY



QUANTUM UNCERTAINTY



M. Tegmark & J.A. Wheeler, 2001

The Power of superposition

1 qubit...2 states
2 qubits...4 states

N qubits..2^N states

40 qubits: 10^{12} parallel operations
300 qubits: more than the atoms in the universe

Entanglement, again

Definition: two particles are entangled if the quantum state of one particle cannot be described independently from the quantum state of the other particle.

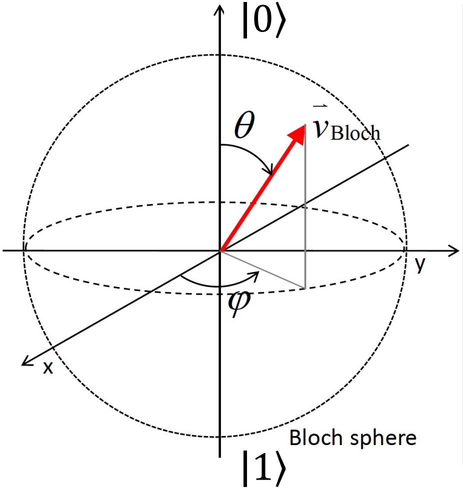
Intuition: measuring the quantum state of one particle implies knowledge of the quantum state (e.g. momentum, spin, polarization, etc.) of the other entangled particle using the same projection.

The qubit, again

$$|\psi\rangle = \alpha_0|0\rangle + \alpha_1|1\rangle$$

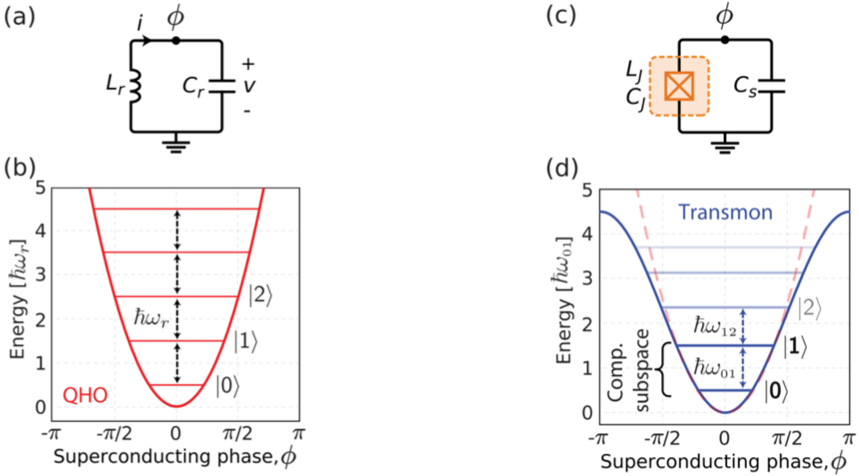
α_0 , α_1 : complex numbers

θ: polar angle
φ: azimuth
δ: global phase (ignored in the Bloch sphere)



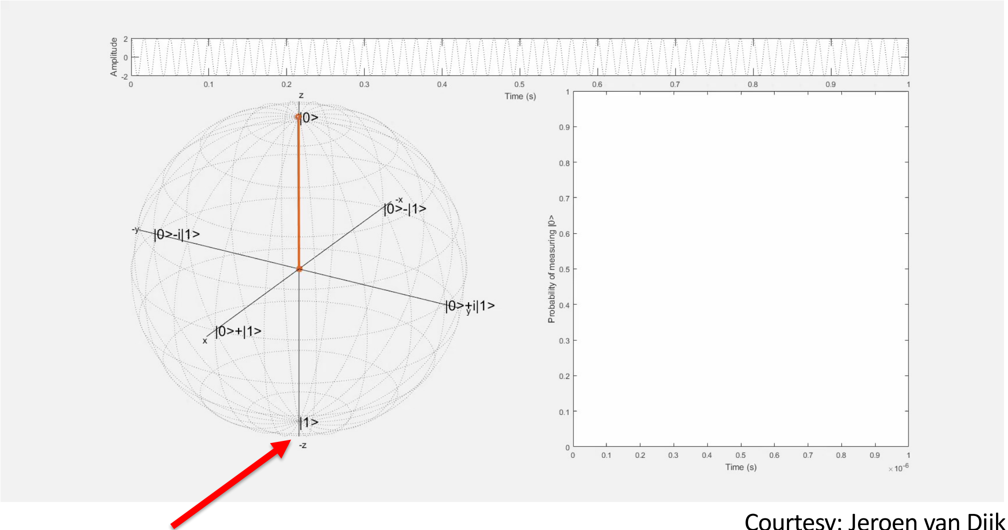
How to build a qubit: the transmon

- Similar to a LC tank with a non-linear load (a double Josephson junction)



P. Krantz et al., A quantum engineer's guide to superconducting qubits, Appl. Phys. Rev. 6, 021318 (2019)

How to control a qubit



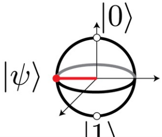
Fidelity

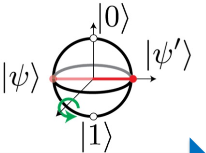
Courtesy: Jeroen van Dijk

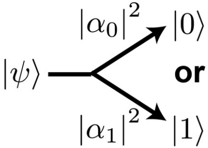
Classical vs. quantum computing

	Information	Processing	Extract Information
Classical	**Bit** "0" or "1"	**Boolean Logic** D → Q D | Q: 1 | 0	**Deterministic Bit** "0" or "1"
Quantum	**Qubit (Quantum state)** $\lvert\psi\rangle = \alpha_0 \lvert 0\rangle + \alpha_1 \lvert 1\rangle$	**Unitary Transform (Rotation)** $\lvert\psi'\rangle = \underbrace{\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}}_{\hat{U}} \underbrace{\begin{bmatrix} \alpha_0 \\ \alpha_1 \end{bmatrix}}_{\lvert\psi\rangle}$	**Probabilistic State Collapse**

Classical: DETERMINISTIC





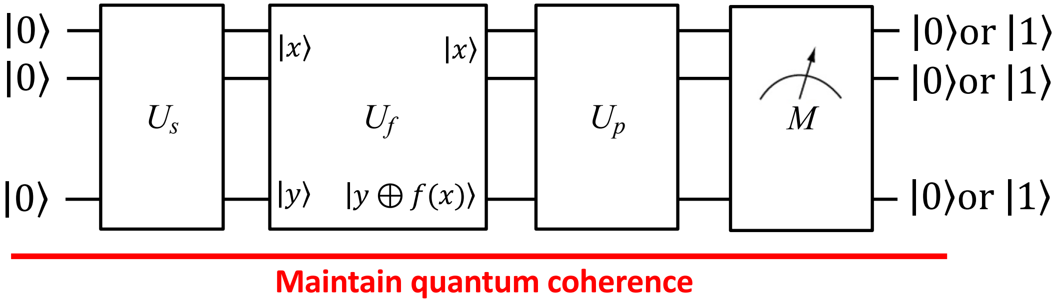


Quantum: DETERMINISTIC → PROBABILISTIC

Courtesy: Joseph Bardin, ISSCC 2022

Multi-qubit quantum algorithm

- Initialize qubits
- Create superposition
- Encode function in unitary
- Process
- Measure



Quantum Sensing / Quantum Imaging

Definitions

- Within quantum technology, a **Quantum Sensor** utilizes properties of quantum mechanics, such as quantum entanglement, quantum interference, and quantum state squeezing, which have optimized precision and beat current limits in sensor technology [...].

- **Quantum Imaging** is a new sub-field of quantum optics that exploits quantum correlations such as quantum entanglement of the electromagnetic field, in order to image objects with a resolution or other imaging criteria that is beyond what is possible in classical optics [...].

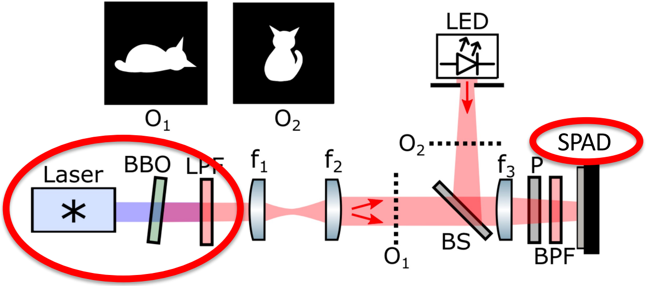
Source: Wikipedia

Quantum imaging

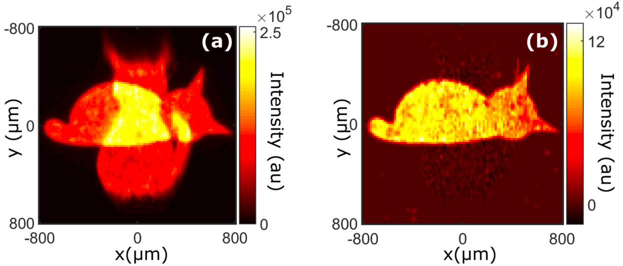
- Quantum LiDAR
- Ghost imaging
- Qua
- Qua
- Qua
- Qua
- Qua
- Quantum super-resolution
- Quantum plenoptic cameras
- Quanta burst photography

[Andrei Nomerotski] Require *either* single-photon granularity *or* picosecond timestamping, sometimes *both*

Quantum distillation

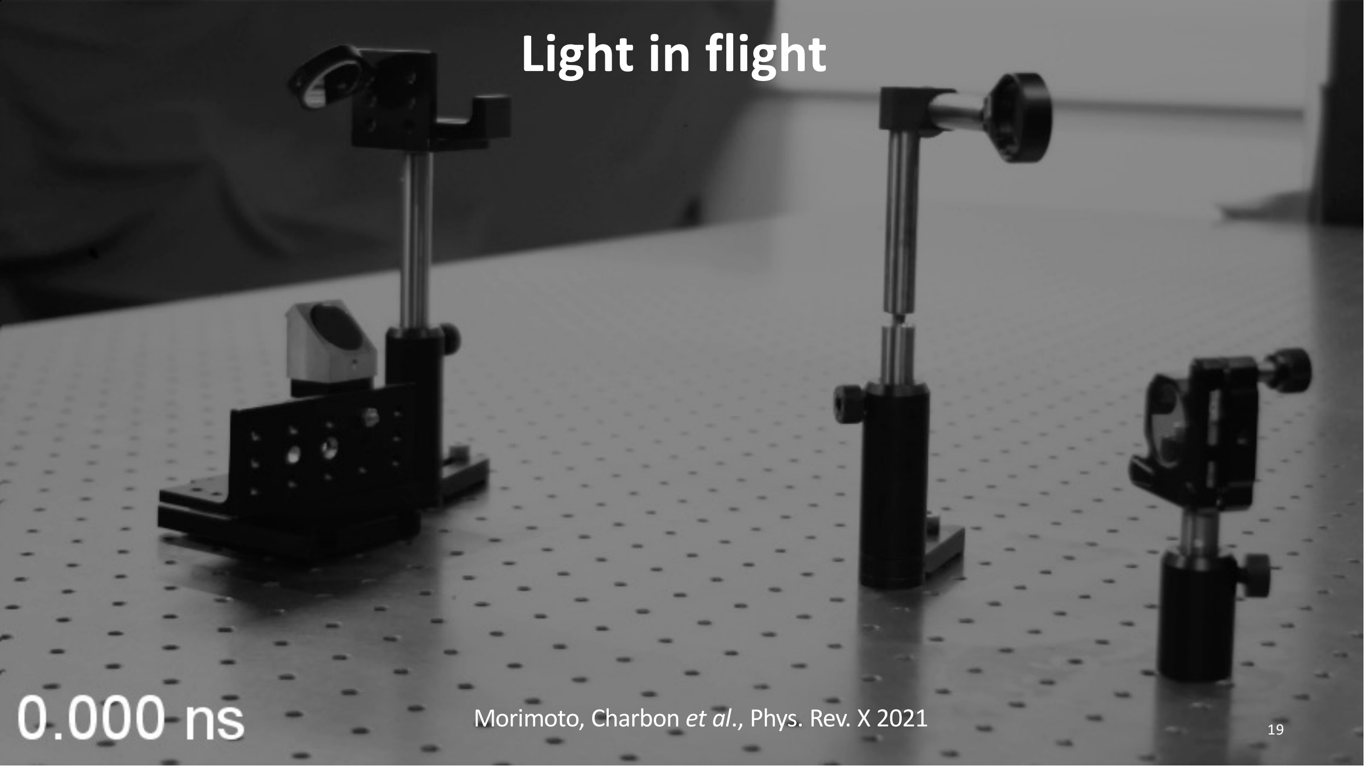


a) Hide quantum image in plain sight
b) Separate quantum image away from classical image



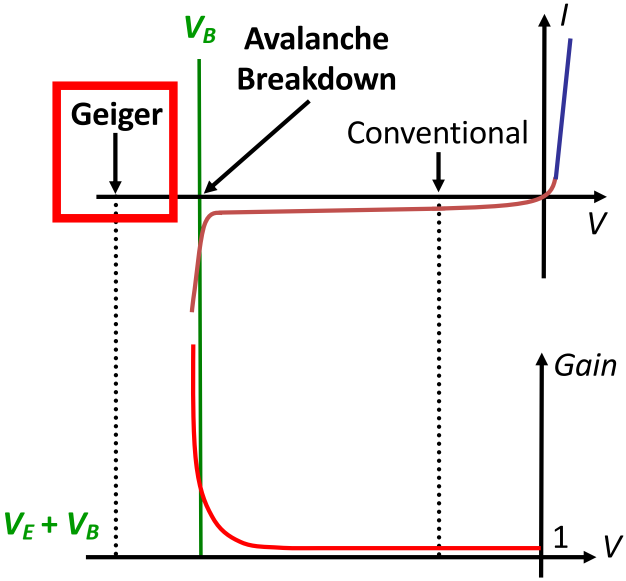
H. Defienne et al., Science Advances 5(10), 2019

Light in flight

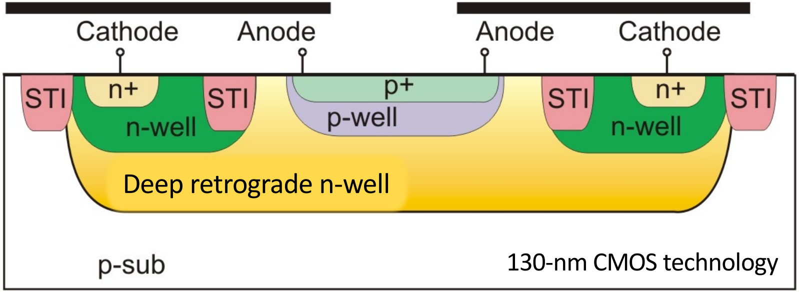


Morimoto, Charbon *et al.*, Phys. Rev. X 2021

Single-photon avalanche diode (SPAD)



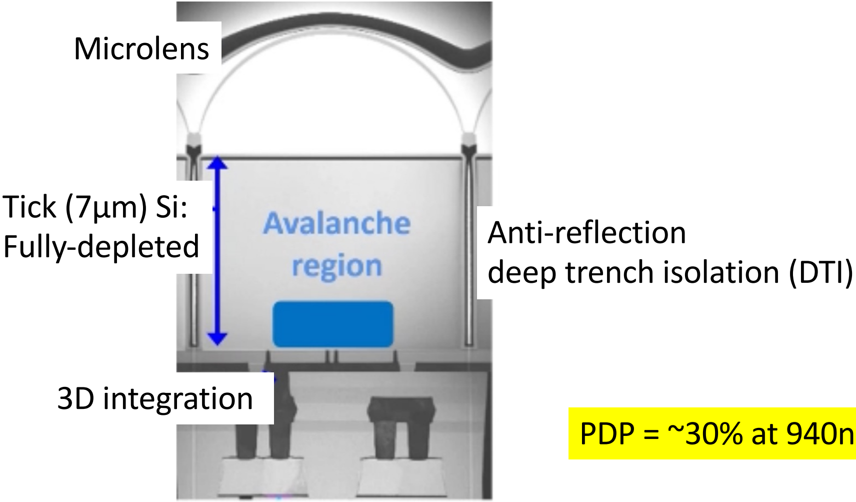
Frontside CMOS SPAD



Niclass et al. 2007 – Richardson et al. – Pellegrini et al.

Reproducible, reliable, miniaturizable

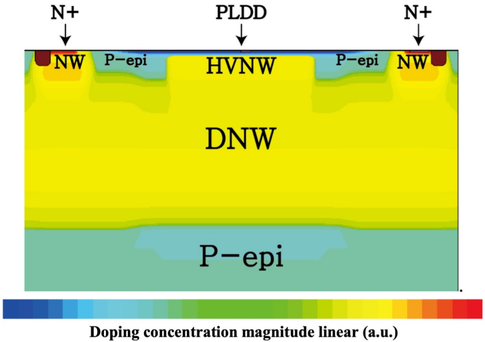
Backside-illuminated SPAD



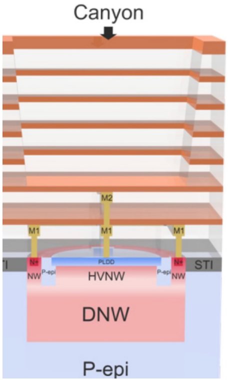
Ito *et al*., 2020 (Sony)

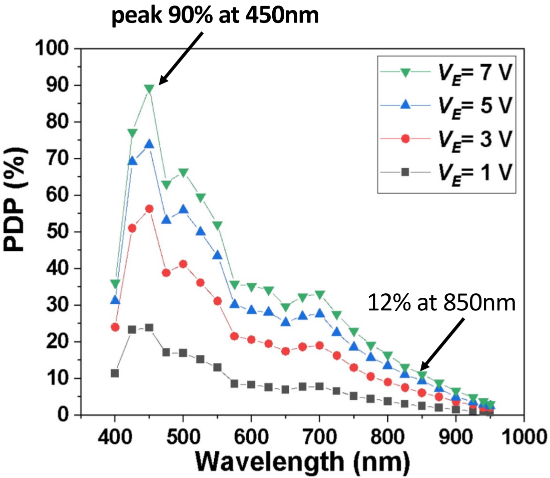
PDP = ~30% at 940nm

Near-ultraviolet CMOS SPADs

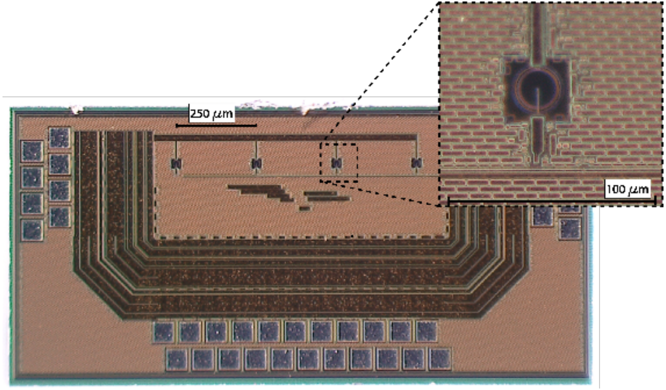


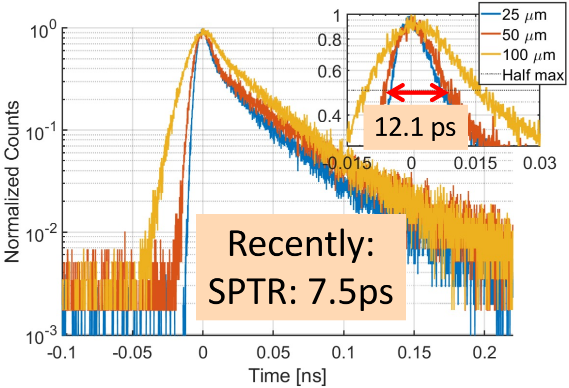
Ha *et al*. 2023





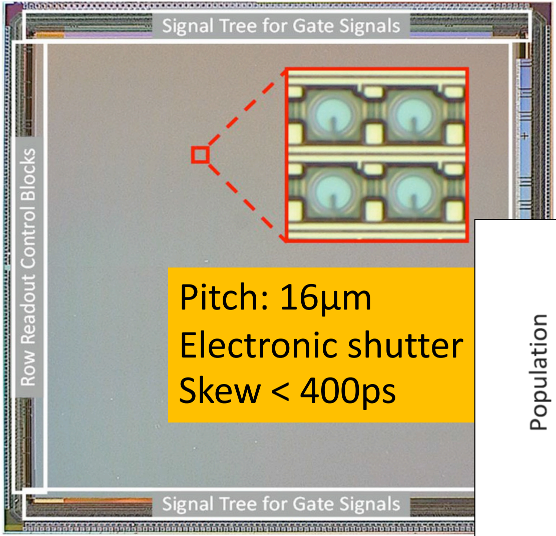
Ultrafast CMOS SPADs

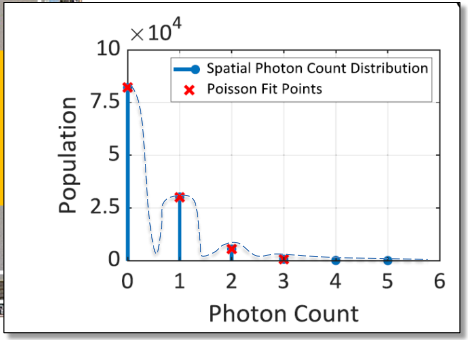




F. Gramuglia et al., JSTQE 2021
F. Gramuglia et al., Frontiers in Physics, 2022

Photon-number resolving SPAD array: SwissSPAD2/3

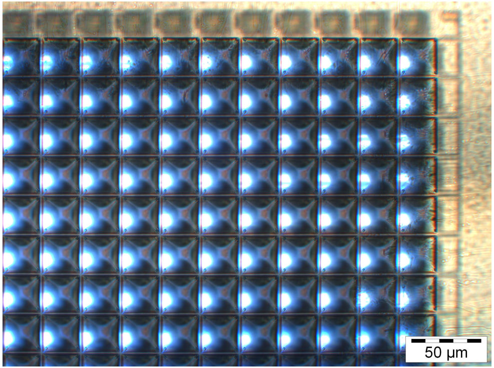




A. Ulku *et al.*, *JSTQE* 2019

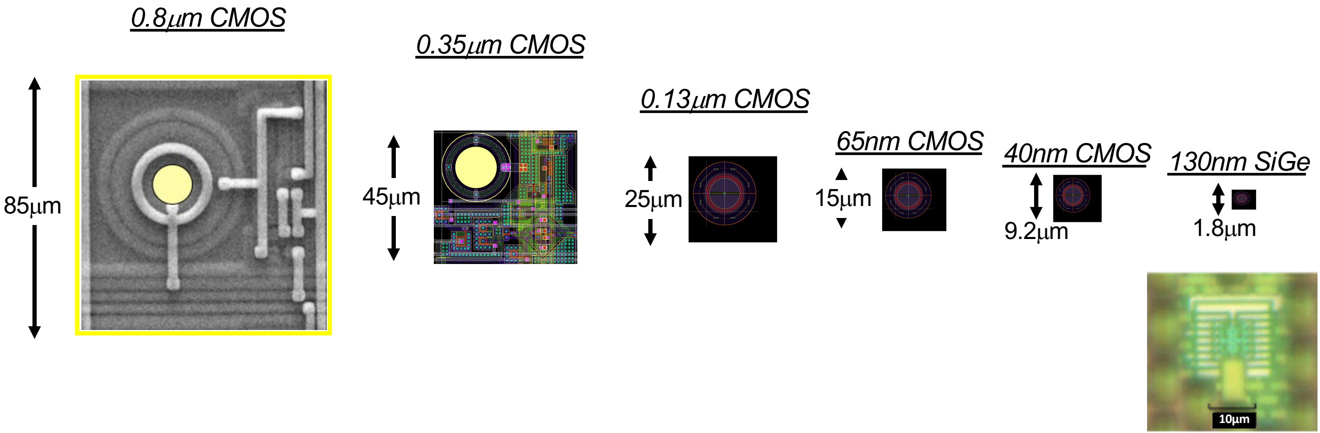
The phenomenal CMOS SPAD evolution

- Timing resolution (100ps → 7.5ps)
- Sensitivity
  - Photon Detection Probability (PDP) (10% → 90%)
  - Fill-factor (1% → 80%)
- Dead time (100ns →1.5ns)
- Dark counts (kcps → cps → mcps)
- Afterpulsing (10% → 0.1%)



cps = counts per second
kcps = 10^3 cps
mcps = 10^{-3} cps

The true marvel: scaling

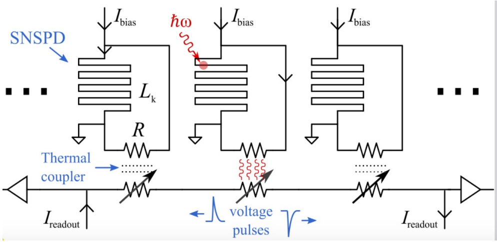


F. Liu and E. Charbon, Optics Express 2024

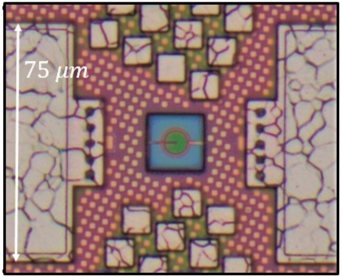
Why Cryogenic Electronics?

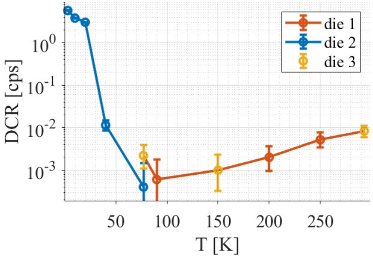
Emerging applications may require cryo

- SNSPDs
- SPADs
- Quantum computing
- High-performance computing



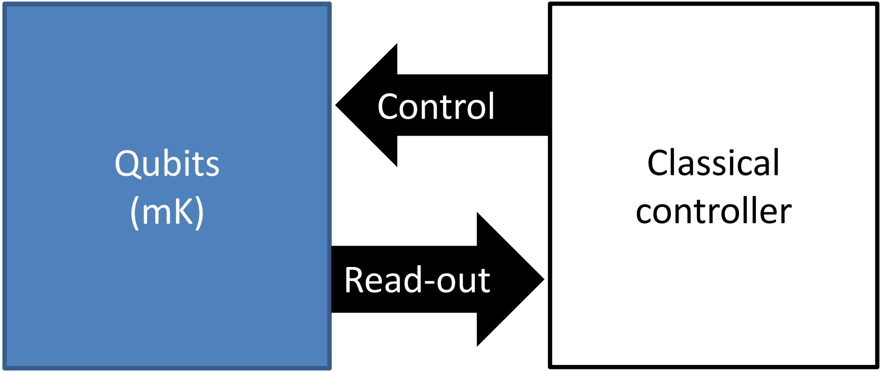
Wollman et al, Optics Express (2019) MacCaughan et al, APL (2022)





Morelle et al., QIM 2021

Role of classical control in QC

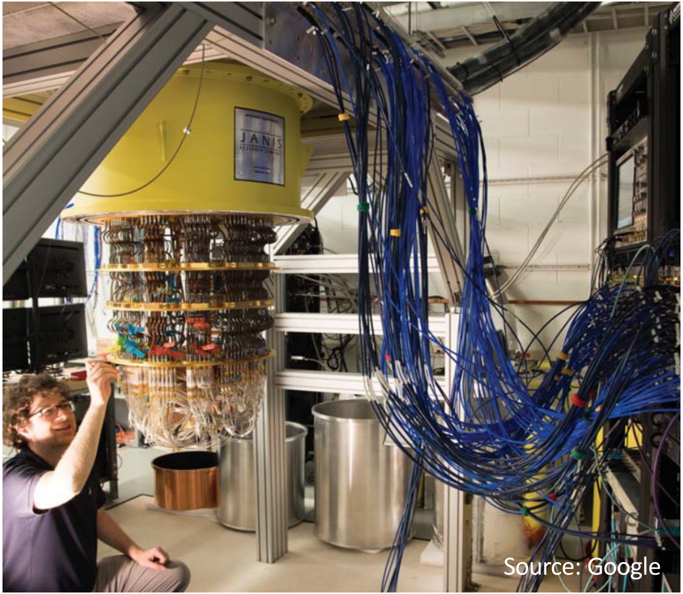


Charbon *et al.*, *IEDM* 2016

- Carrier frequency: 5 – 6 GHz
- Pulses: 10 – 100 ns
- Various readout schemes

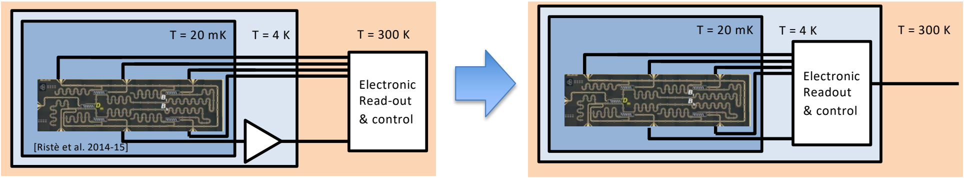
Examples of readout schemes: ESR: Electron spin resonance – EDSR: Electric dipole spin resonance

Current solution



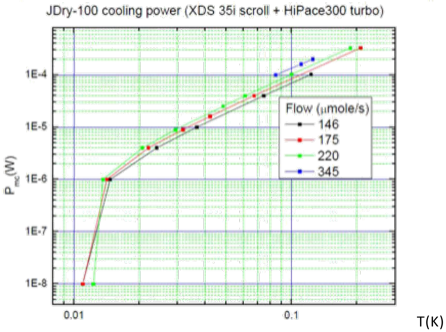
Proposed solution

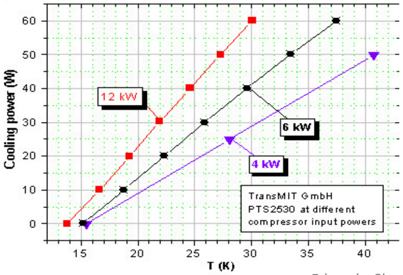
- **Proposed solution**
  - Electronics at 4 K
  - Only connections to 4 K to 20 mK are needed



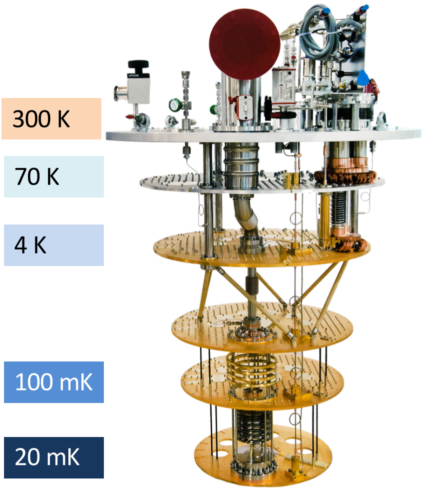
- **Ultimate solution**
  - Qubits at 4 K
  - Monolithic integration

Cooling power issue



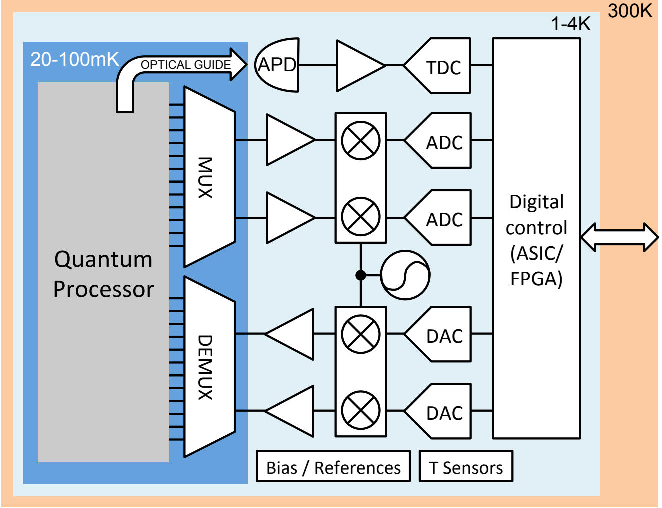


Dilution refrigerator



Courtesy: Oxford instruments

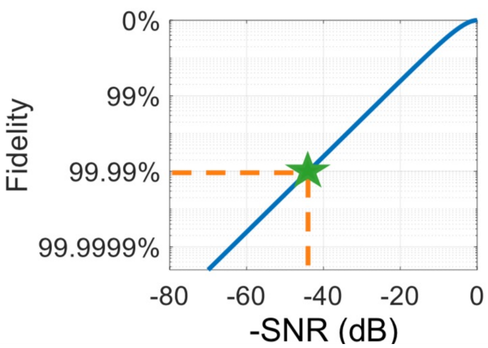
Electronic readout & control



E. Charbon *et al.*, *IEDM* 2016

How do we get electrical specs?

- State-of-the-art spin qubits: fidelity < 99.9%
- Target: 99.99% (four 9's)
  - This translates to a SNR > 44 dB for a bandwidth of 25 MHz



J. v.Dijk et al., *PRA* 2019

Scalability issue

- Noise budget..< 0.1nV/√Hz
- Power budget (for scalability)................... << 2mW/qubit
- Physical dimensions (for scalability)......... 30nm
- Bandwidth (for multiplexing).................... 1-12GHz
- Kick-back avoidance

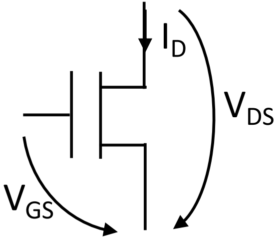
The design of a qubit controller

The right technology

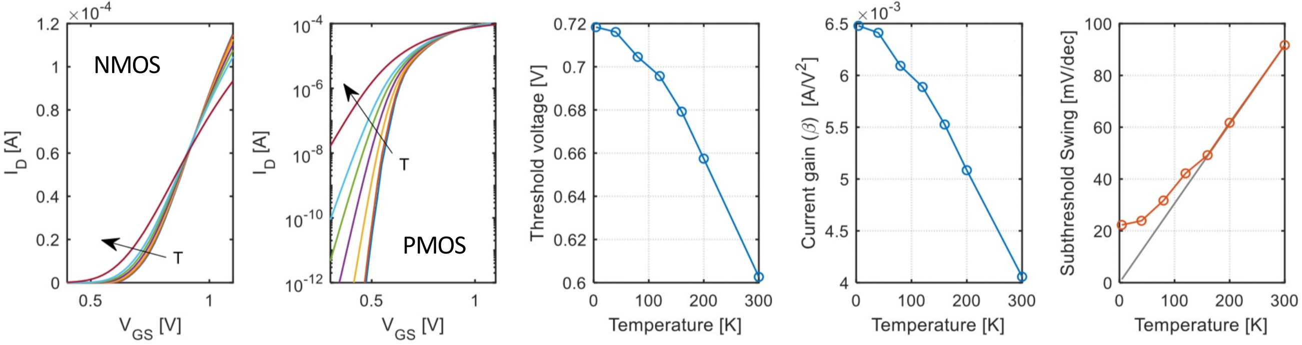
Device	Lowest useable temperature	Limit
Si BJT	100 K	Low gain
Ge BJT	20 K	Carrier freeze-out
SiGe HBT	4 K (or lower)	
Si JFET	40 K	Carrier freeze-out
III-V MESFET	4K (or lower)	Lower freeze-out?
CMOS (>160nm)	4 K	Non-idealities
CMOS (<40nm)	40 mK	Power dissipation

Most used

Cryogenic effects



- Mismatch increases
- Leakage drastically reduces
- Substrate become floating

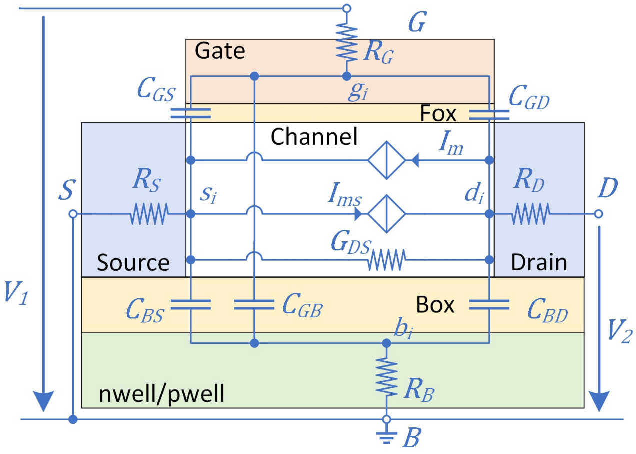


Fabio Sebastiano, Quantum Week, Oct. 12, 2020

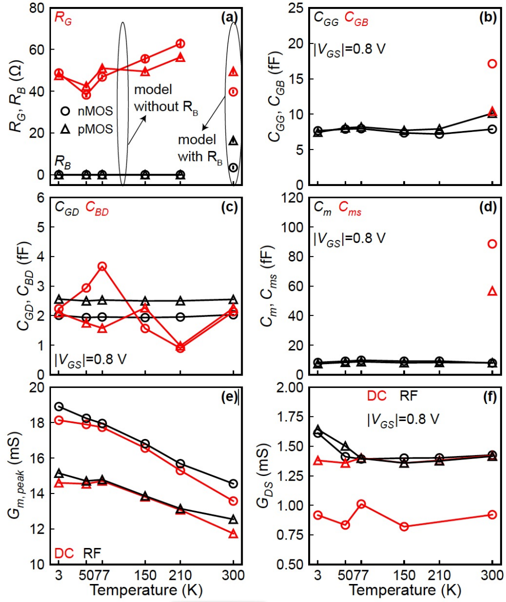
Extensive modeling campaigns

- CMOS 0.16μm STMicroelectronics
- CMOS 40nm TSMC
- CMOS 28nm STMicroelectronics bulk/FDSOI
- CMOS 22nm FDSOI Global Foundries
- CMOS 16nm FinFET TSMC

RF modeling of CMOS 22nm FDSOI

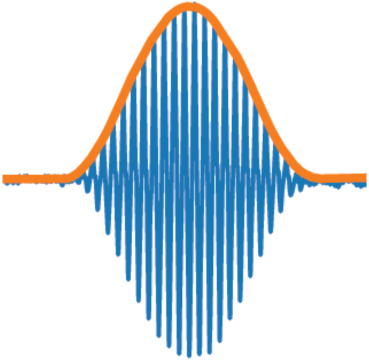


H.C. Han et al., *ESSDERC* 2022

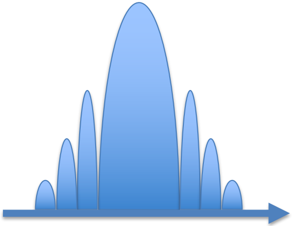


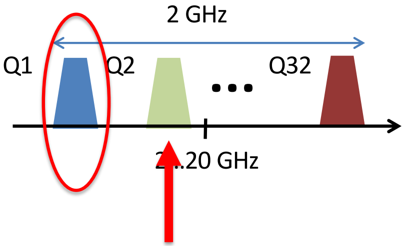
Qubit controller: the problem at hand

Time domain



Frequency domain





The design of Horse Ridge

	Value	Infidelity contribution to an operation	Infidelity contribution to idling
Frequency			
nominal	10 GHz	0.64×10^{-9} (a)	
spacing	1 GHz		1×10^{-6} (b)
inaccuracy	11 kHz	125×10^{-6}	308×10^{-6}
oscillator noise	11 kHz $_{rms}$	125×10^{-6}	308×10^{-6}
nuclear spin noise	1.9 kHz $_{rms}$ (c)	3.6×10^{-6}	8.9×10^{-6}
wideband noise	12 μV $_{rms}$	125×10^{-6}	
Phase			
inaccuracy	0.64°	125×10^{-6}	31×10^{-6} (d)
Amplitude			
nominal	2 mV		
inaccuracy	14 μV	125×10^{-6}	
noise	14 μV $_{rms}$	125×10^{-6}	
off-spur	19 μV (e)		217×10^{-6}
off-noise	10 μV $_{rms}$		125×10^{-6}
Duration			
nominal	500 ns		
inaccuracy	3.6 ns	125×10^{-6}	
noise	3.6 ns $_{rms}$	125×10^{-6}	
		$F_{X,Y} = 99.9\,\%$	$F_I = 99.9\,\%$

← **Target fidelity**

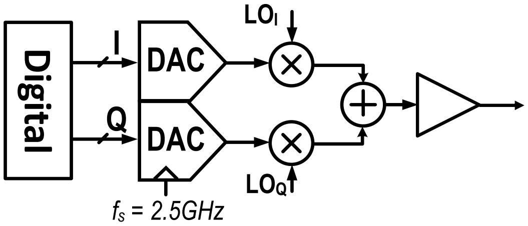
Noise source	ENBW	Noise level
Frequency noise	2.5 MHz	$\mathcal{L}(1\,\text{MHz}) = -106\,\text{dBc/Hz}$
Wideband additive noise	2.9 MHz	$7.1\,\text{nV}/\sqrt{\text{Hz}}$
Amplitude noise	1.0 MHz	$14\,\text{nV}/\sqrt{\text{Hz}}$, SNR = −40 dB
Amplitude off-noise	2.0 MHz	$7.1\,\text{nV}/\sqrt{\text{Hz}}$

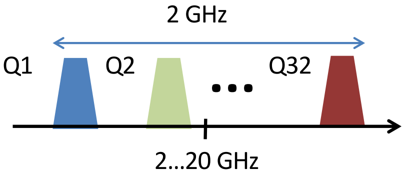
(a) Due to the RWA.
(b) Due to leakage in FDMA-setup using rectangular envelopes.
(c) From [61], $T_2^* = 120\,\mu s$.
(d) FDMA Z-corrections limit the idling operation.
(e) Equivalent to −41 dBc.

Jeroen van Dijk, Thesis, 2021

Initial architecture

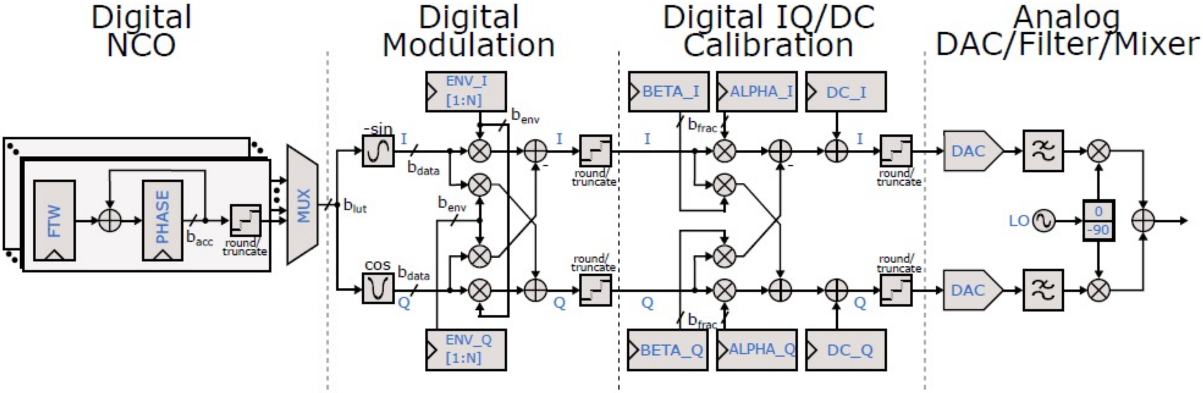
➢ **Lower Speed DAC + Mixer**





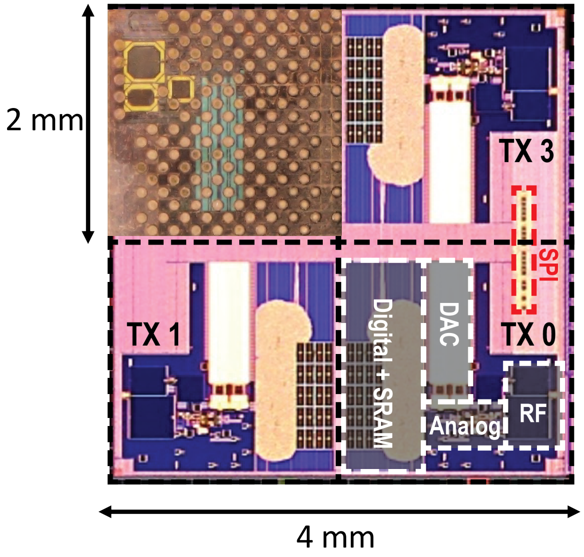
Analog: noise/linearity specifications known + feasible

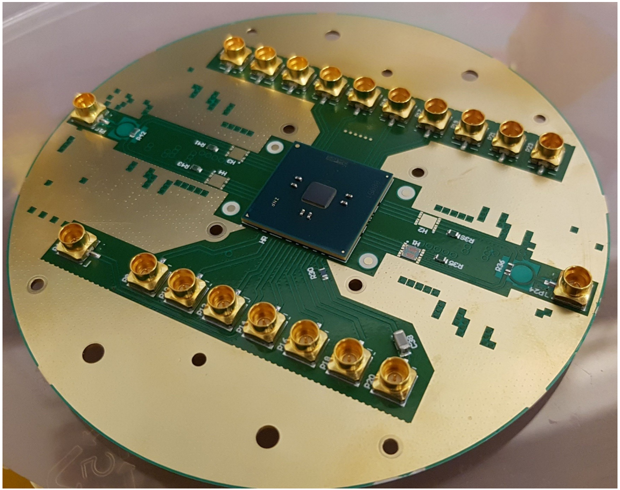
Final architecture



Patra, van Dijk, Xue *et al*., *ISSCC* 2020 & *JSSC* 2020

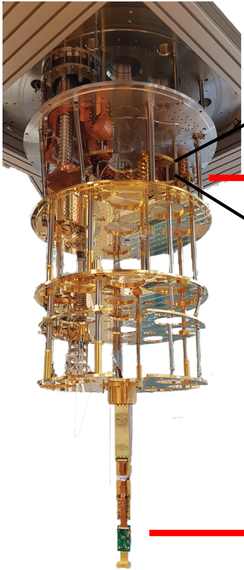
The Horse Ridge chip & package





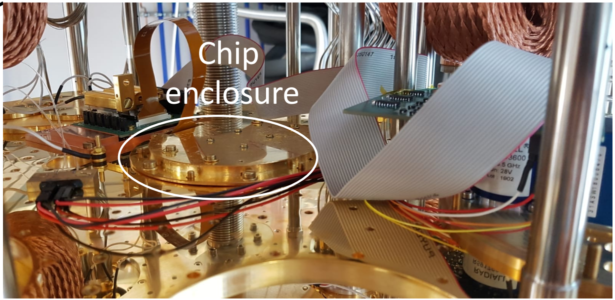
Intel 22nm FinFET Technology
4 TX => 128 qubits

Measurement setup

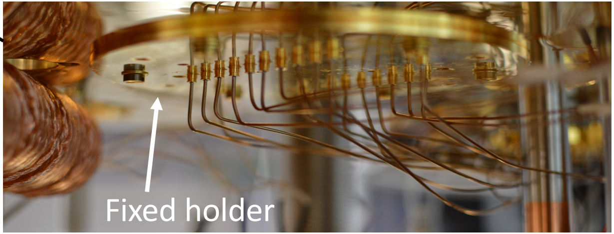


Chip at 3 K plate

Qubit at 10 mK

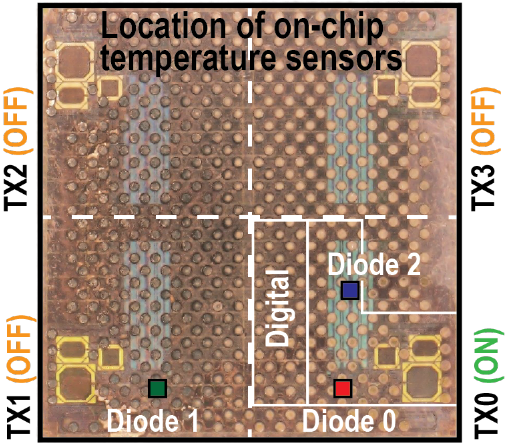


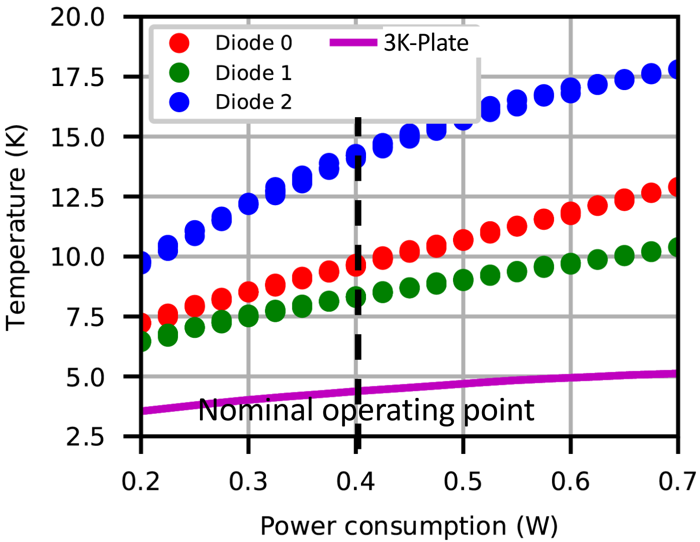
Top view



Bottom view

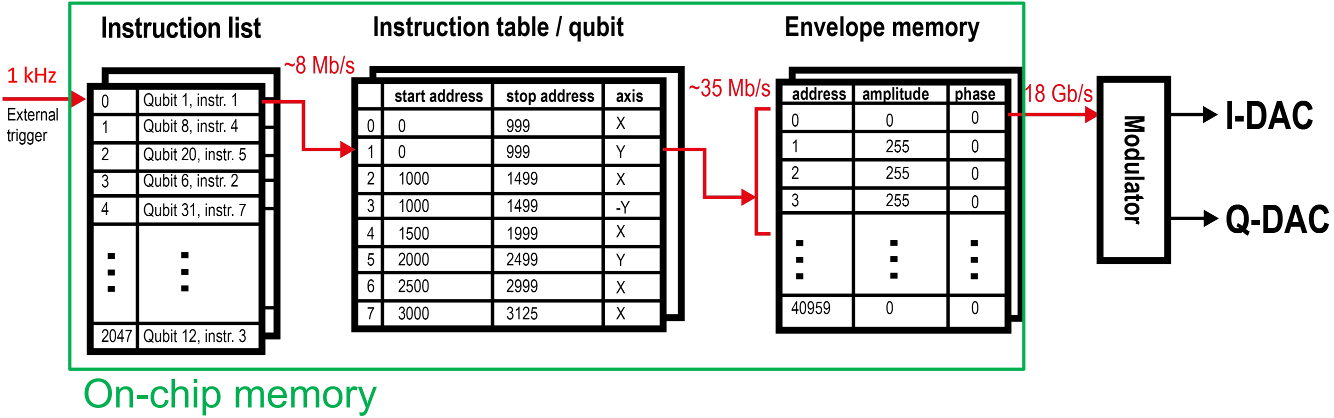
Self-heating





Instruction set memory

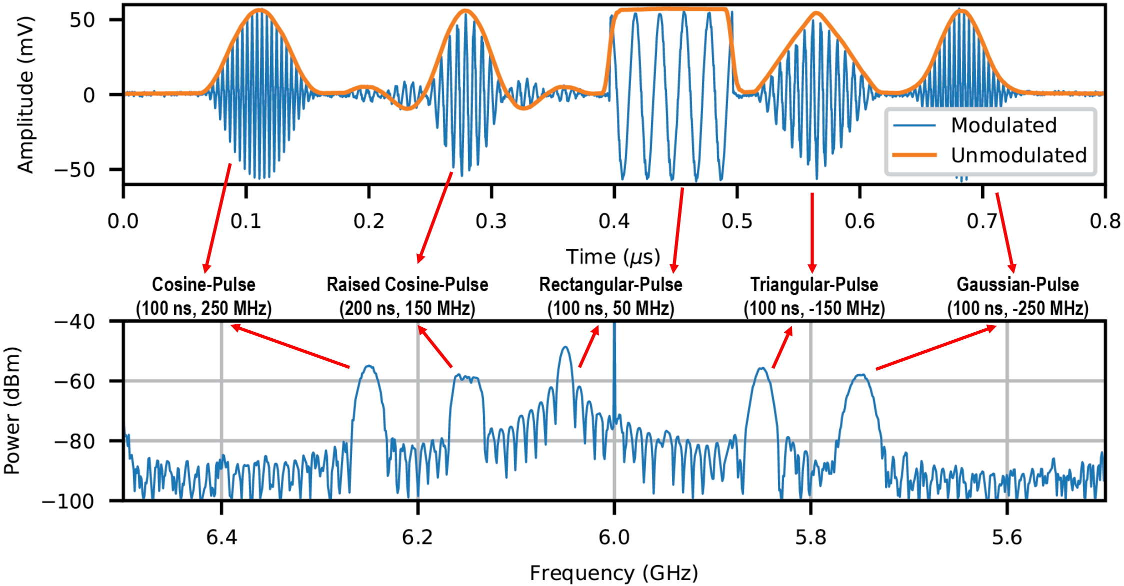
- No high-speed connection required during quantum algorithm execution



0	Qubit 1, instr. 1
1	Qubit 8, instr. 4
2	Qubit 20, instr. 5
3	Qubit 6, instr. 2
4	Qubit 31, instr. 7
⋮	⋮
2047	Qubit 12, instr. 3

	start address	stop address	axis
0	0	999	X
1	0	999	Y
2	1000	1499	X
3	1000	1499	-Y
4	1500	1999	X
5	2000	2499	Y
6	2500	2999	X
7	3000	3125	X

address	amplitude	phase
0	0	0
1	255	0
2	255	0
3	255	0
⋮	⋮	⋮
40959	0	0

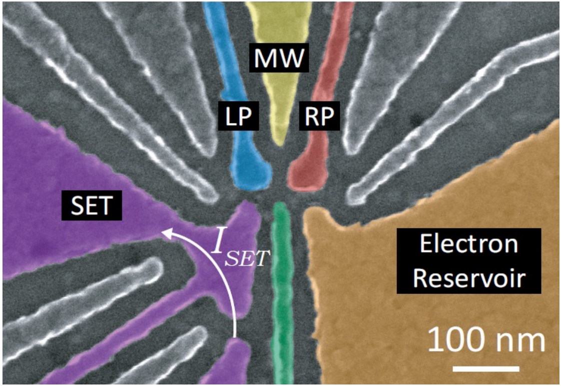


Amplitude (mV)
50
0
−50
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
Time (μs)
Modulated
Unmodulated
Cosine-Pulse (100 ns, 250 MHz)
Raised Cosine-Pulse (200 ns, 150 MHz)
Rectangular-Pulse (100 ns, 50 MHz)
Triangular-Pulse (100 ns, -150 MHz)
Gaussian-Pulse (100 ns, -250 MHz)
Power (dBm)
−40
−60
−80
−100
6.4
6.2
6.0
5.8
5.6
Frequency (GHz)

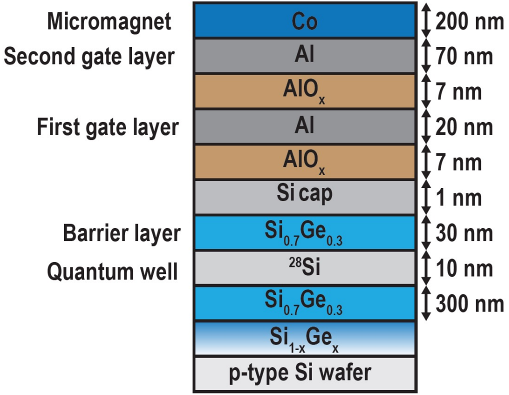
Qubit device in experiments

- Two-qubit processor

Top-view

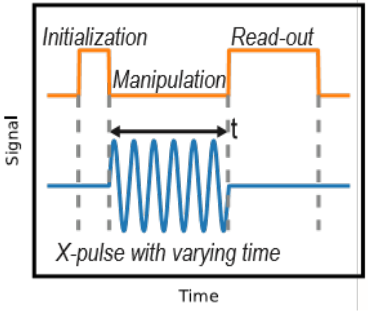


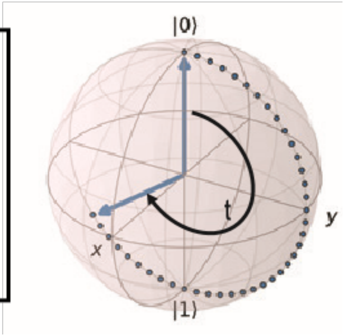
Cross-section view



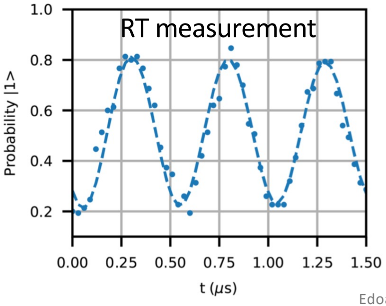
X.Xue, B. Patra, arXiv, 2020

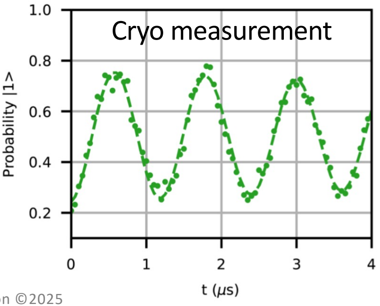
Rabi experiment



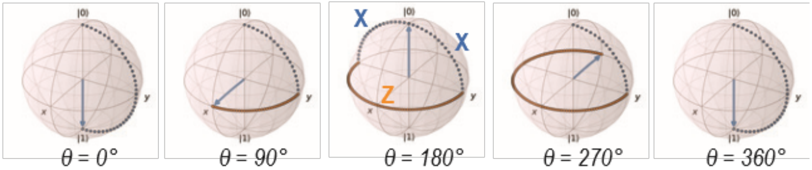


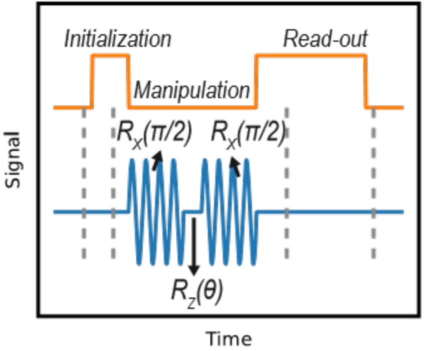
B. Patra, J.v.Dijk *et al.*, *ISSCC* 2020, *JSSC* 2020

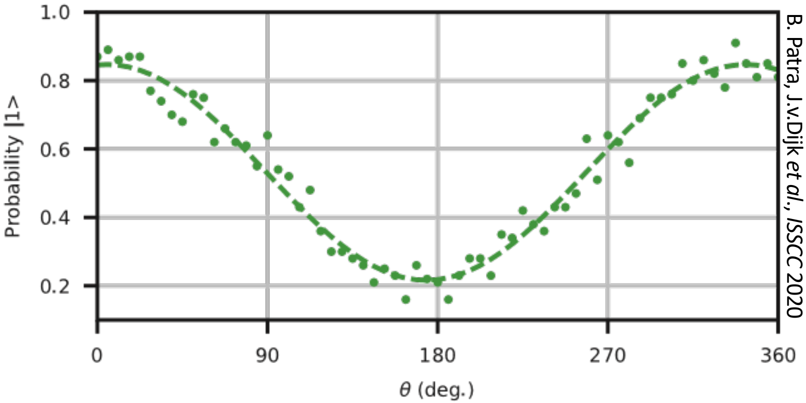




Multiple qubit manipulations: the Ramsey experiment



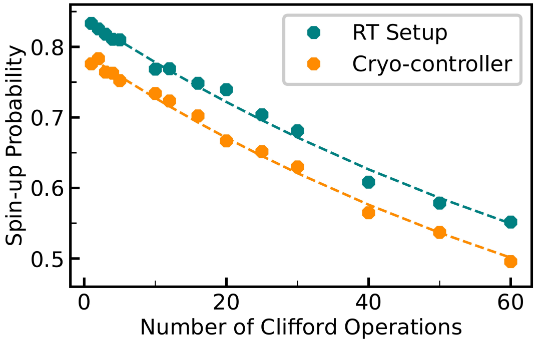




B. Patra, J.v.Dijk *et al.*, *ISSCC 2020*

Randomized benchmarking

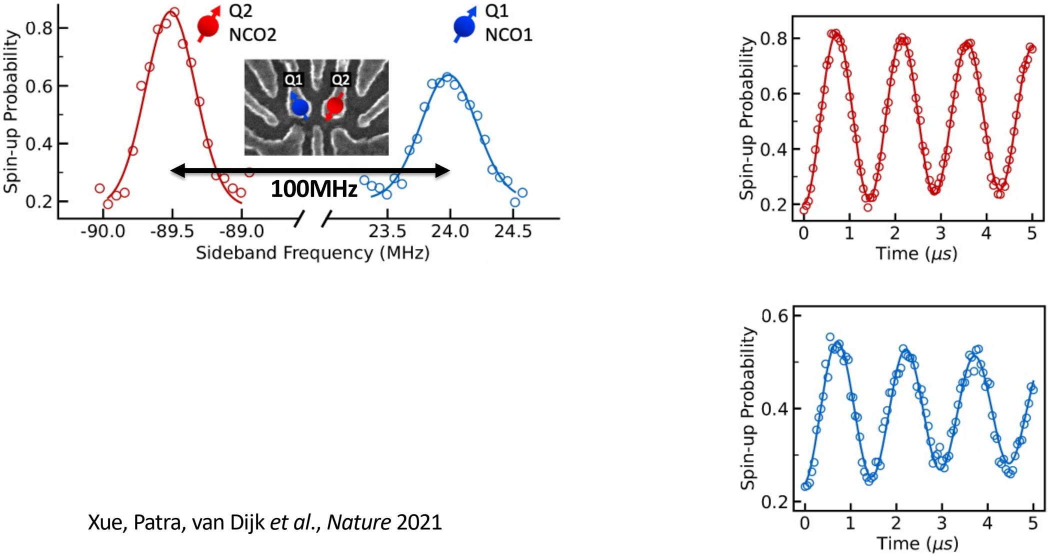
- Up to 60 Clifford gates: Each Clifford gate is averaged over 32 different randomized sequences
- Consistently repeatable: Fidelity limited by qubit sample



Fidelity = 99.71±0.03%

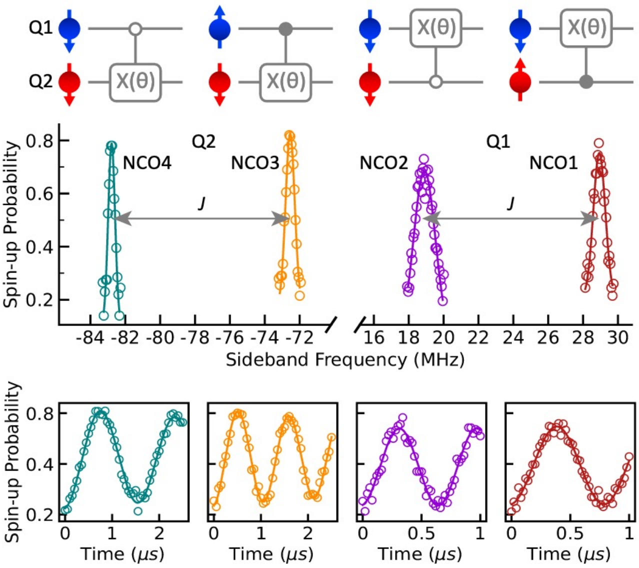
Fidelity = 99.69±0.02%

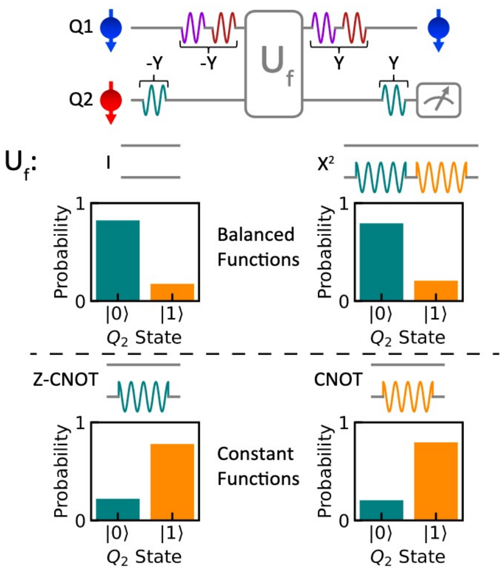
Simultaneous Rabi oscillations by way of FDMA



Xue, Patra, van Dijk *et al.*, *Nature* 2021

2-qubit gate

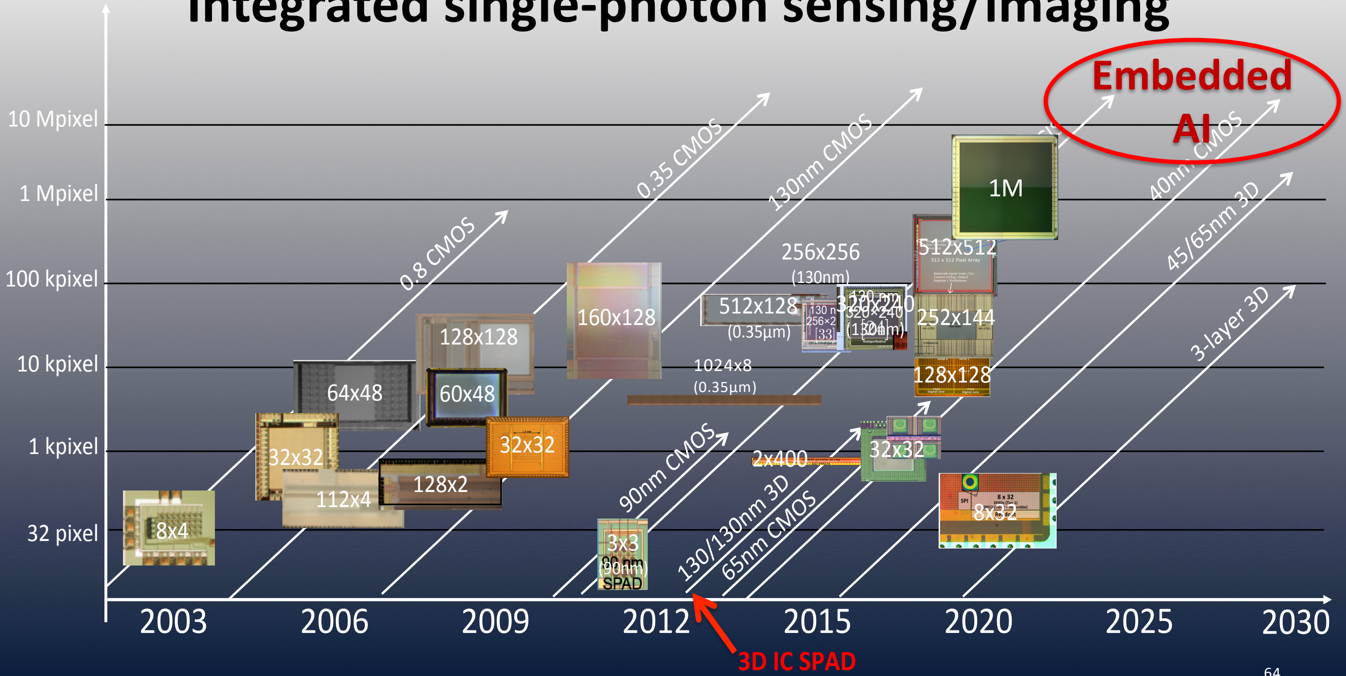




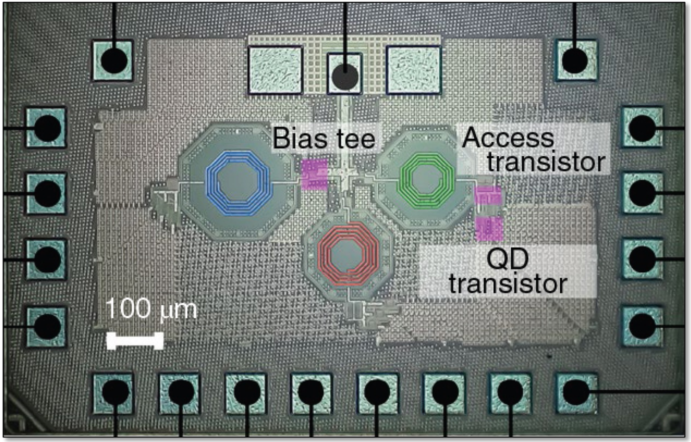
Xue, Patra, van Dijk *et al.*, *Nature* 2021

Perspectives

Integrated single-photon sensing/imaging

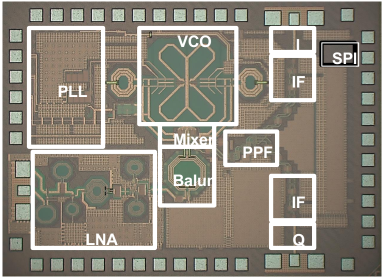


Integrated qubits

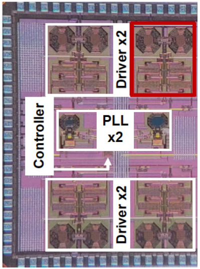


Y. Peng *et al*., JSSC 2022
A. Ruffino *et al*., *Nature Electronics* 2021

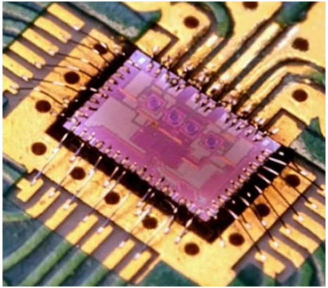
Integrated qubit controllers

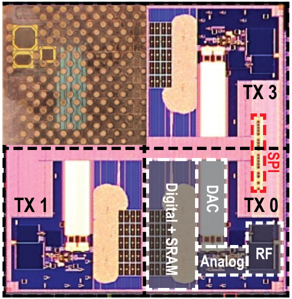


A. Ruffino et al., ISSCC 2021 – Y. Peng et al., *JSSC* 2022

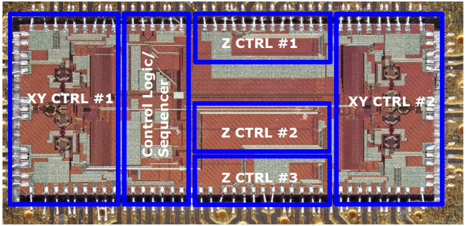


Kang *et al.*, *ISSCC* 2023

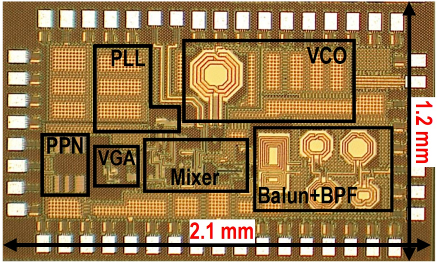

Bardin *et al.*, *ISSCC* 2019



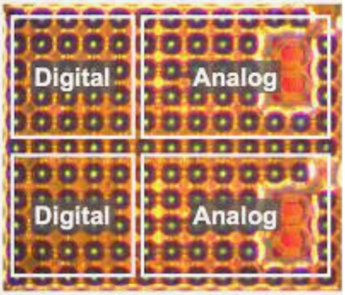
Patra, van Dijk, Xue *et al.*, JSSC 2020
Xue, Patra, van Dijk *et al.*, *Nature* 2021



Yoo *et al.*, *ISSCC* 2023



Peng, Benserhir *et al.*, *CICC* 2024



Underwood *et al.*, *ISSCC* 2023
Parker *et al.*, Nature Electronics 2022

Take-home messages

- Quantum computing and quantum sensing/imaging are here to stay
- Cryogenic electronics can be useful
- But, new tools are badly needed:
  - Cryo-cooling
  - Cryo-modeling
  - Cryo-design
  - Cryo-metrology

Study Quantum Mechanics or dust up your old books

Thank You

http://aqua.epfl.ch

2nd User Group Meeting, Les Diablerets, 2024

Next UGM: 2026

ISSCC 2023