Status and plans for eFEC in Valencia

J. Toledo (Curro)
Universitat Politècnica de València
jtoledo@eln.upv.es

Manpower

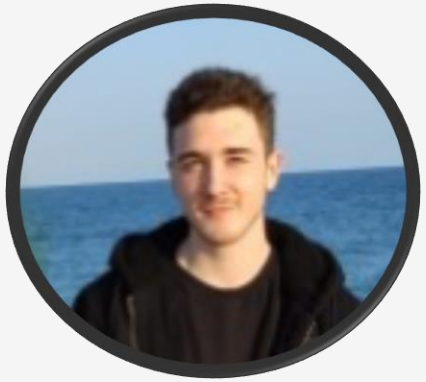
J. Toledo (aka Curro)

Coordinator

In coordination with H. Müller & IFIN-HH

Rubén Caballer, M.Sc. student

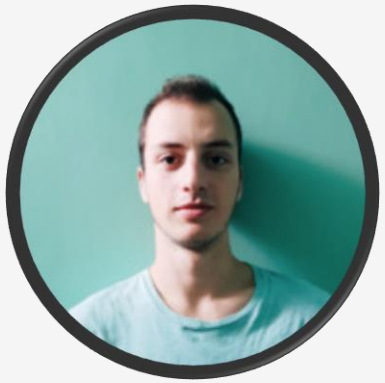
eFEC schematics and routing



In coordination with H. Müller

Juan Atanes, engineer (1yr contact)

Zynq Ultrascale+ FW&SW

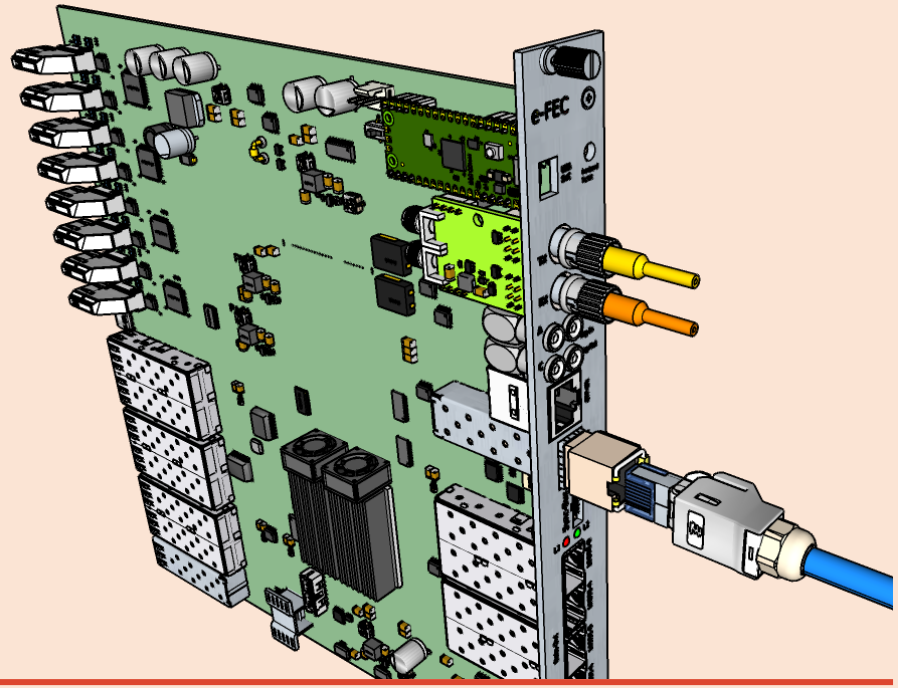


In coordination with H. Müller & IFIN-HH

eFEC prototyping

Juan Atanes, engineer (1yr contact)

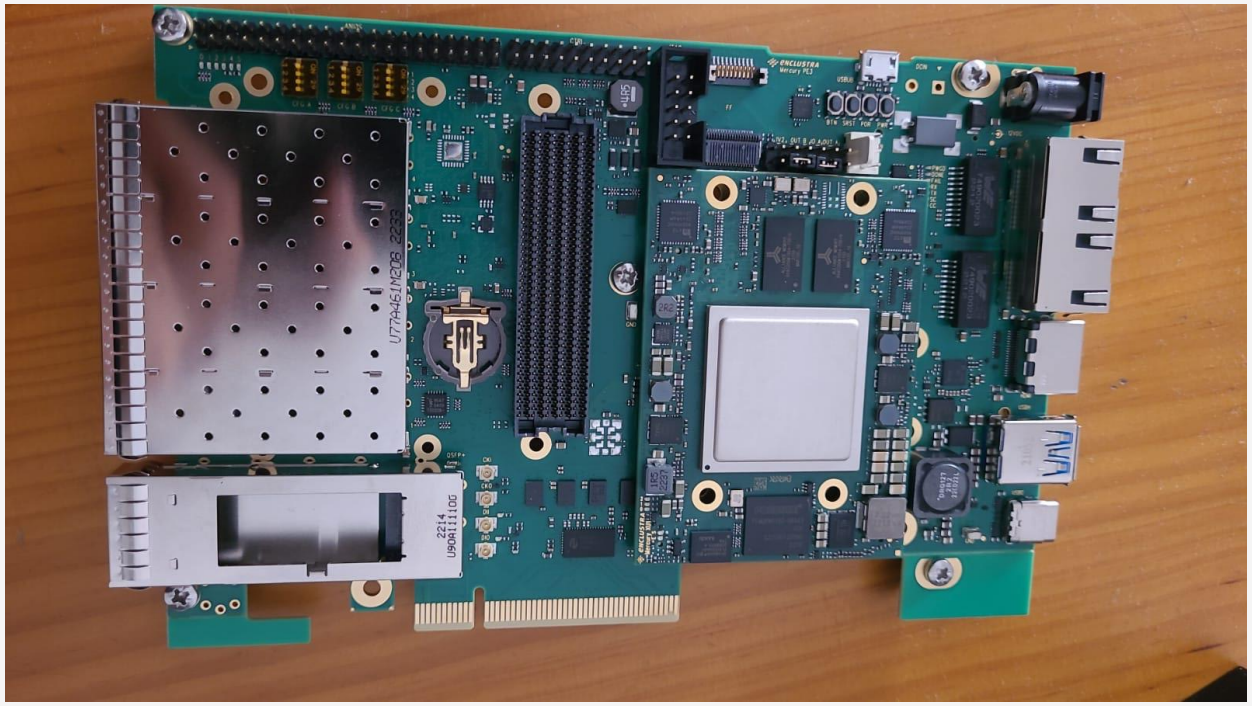
Zynq Ultrascale+ FW&SW



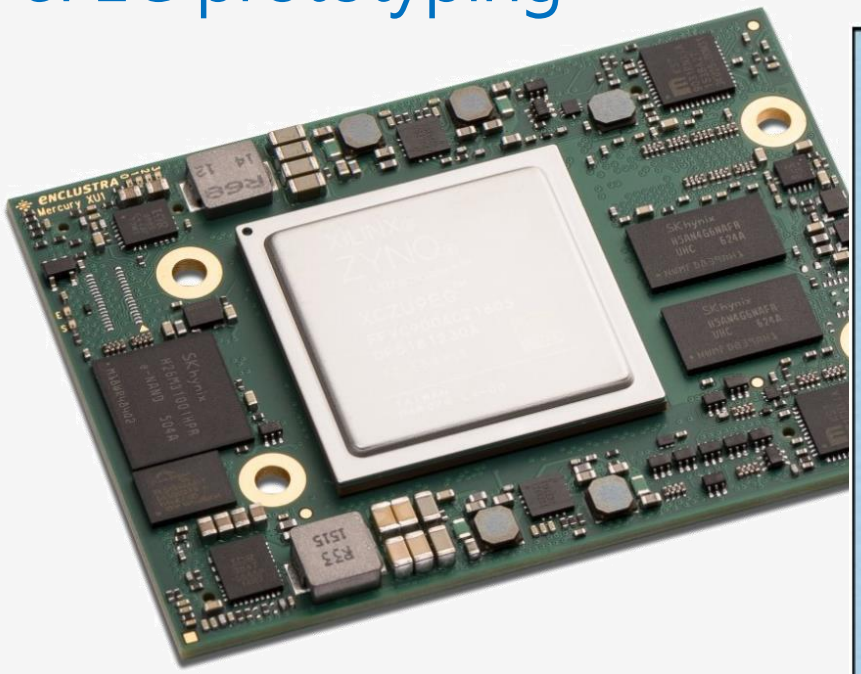
eFEC prototyping

- Already started prototyping eFEC: purchased 2x Enclustra PE3 board + SoM with -9EG SoC
  - SOM: Enclustra ME-XU1-9EG-1E-D11E-G1
  - Base board: Enclustra Mercury+ PE3 board
  - 1 kit in Valencia + 1 kit available for CERN

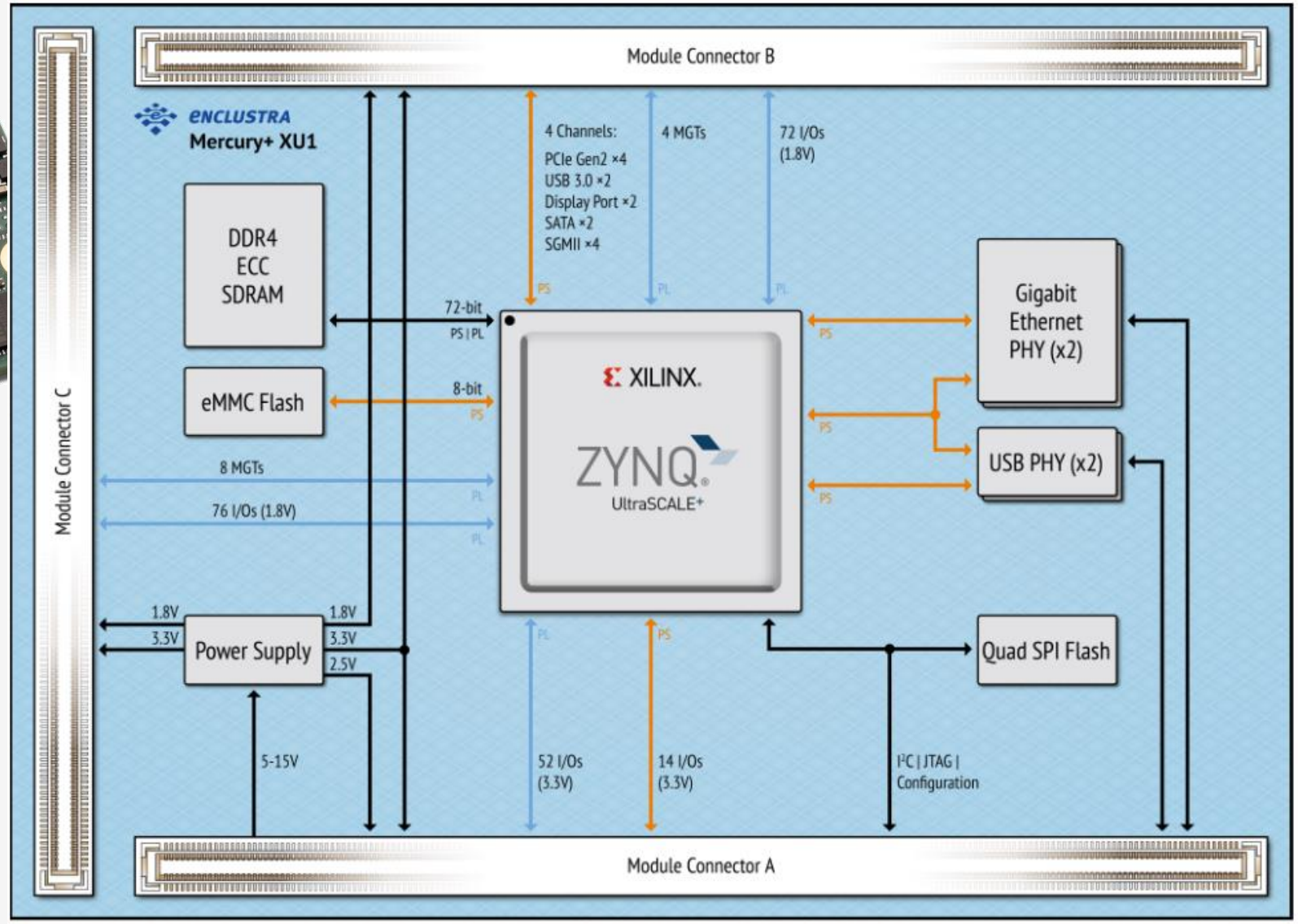
- Allows up to 25 Gbps via QSFP+
- Not valid for 100 Gbps
- Still, a good development platform for Zynq Ultrascale+



eFEC prototyping



Enclustra ME-XU1-9EG-1E-D11E-G1-R4.2



12x MGTs PL side (no GTYs!)

2x GbE PHY PS side

4x additional PS MGTs (SGMII)

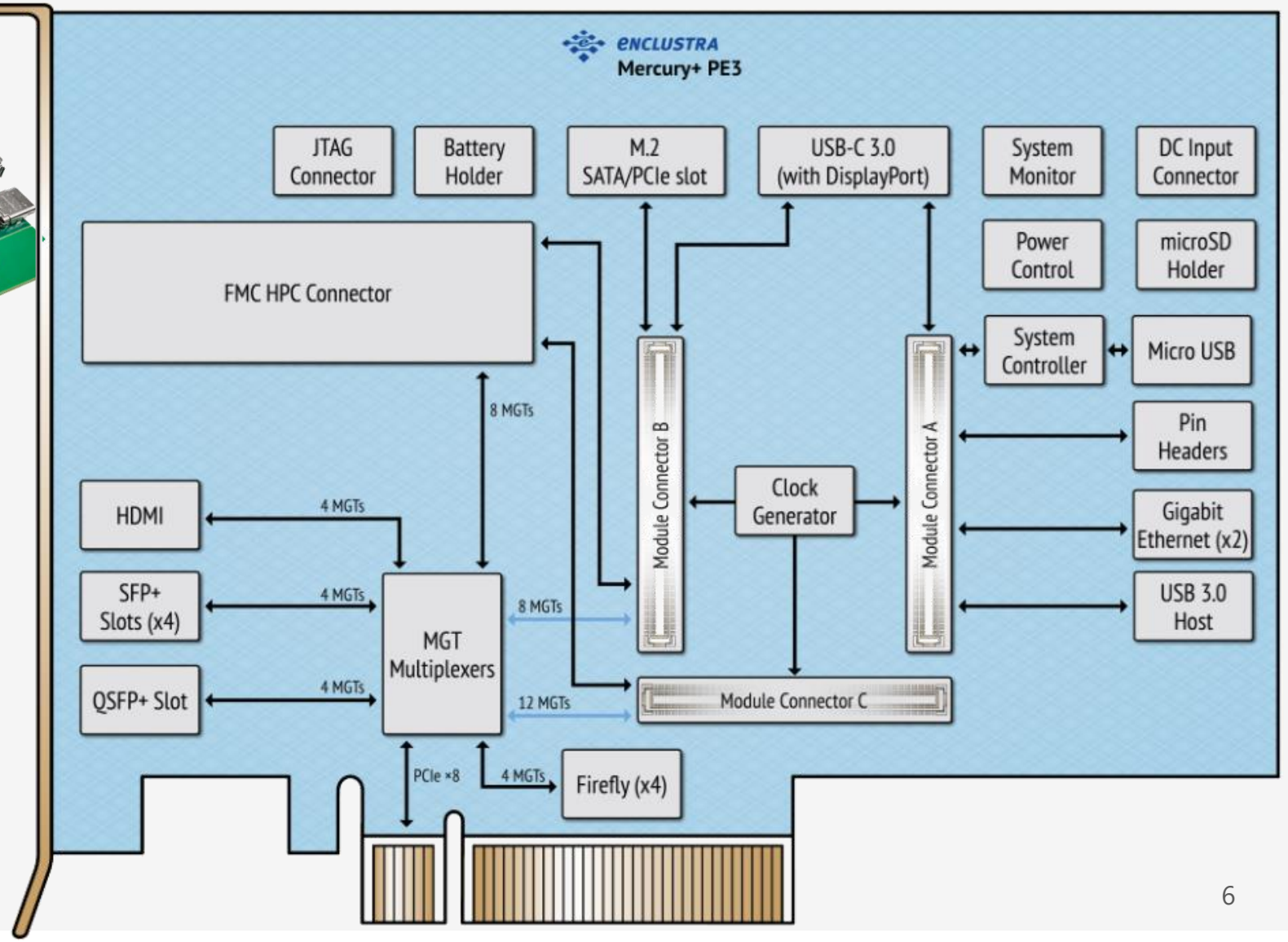
2x USB 3.0

2GB DDR4 (up to 8 GB)

eMMC + QSPI boot memory

eFEC prototyping

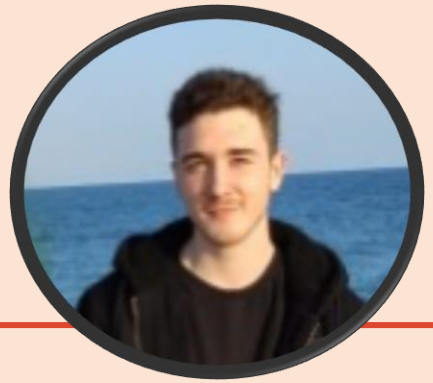
Enclustra Mercury+ PE3



eFEC prototyping

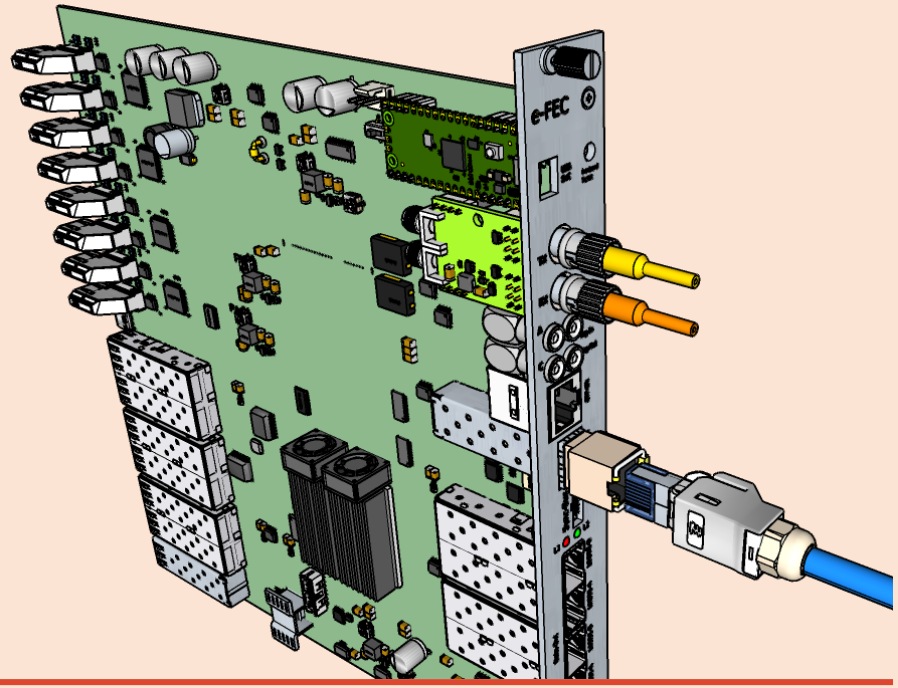
- Just received a donation from AMD at UPV
  - IP core license for 25/100 GbE
  - IP core for RDMA
- Status with FW/SW
  - SoM+PE3 operational (customized Linux version)
  - GbE comm on both PS and PL via optical SFP to PC
  - Currently implementing the 25 GbE IP core from AMD
- Milestones for coming weeks
  - 25 GbE core tests (Zynq Ultrascale+ to PC)
  - RDMA protocol comm with a PC at the highest bitrate allowed by Enclustra SoM+baseboard

eFEC design

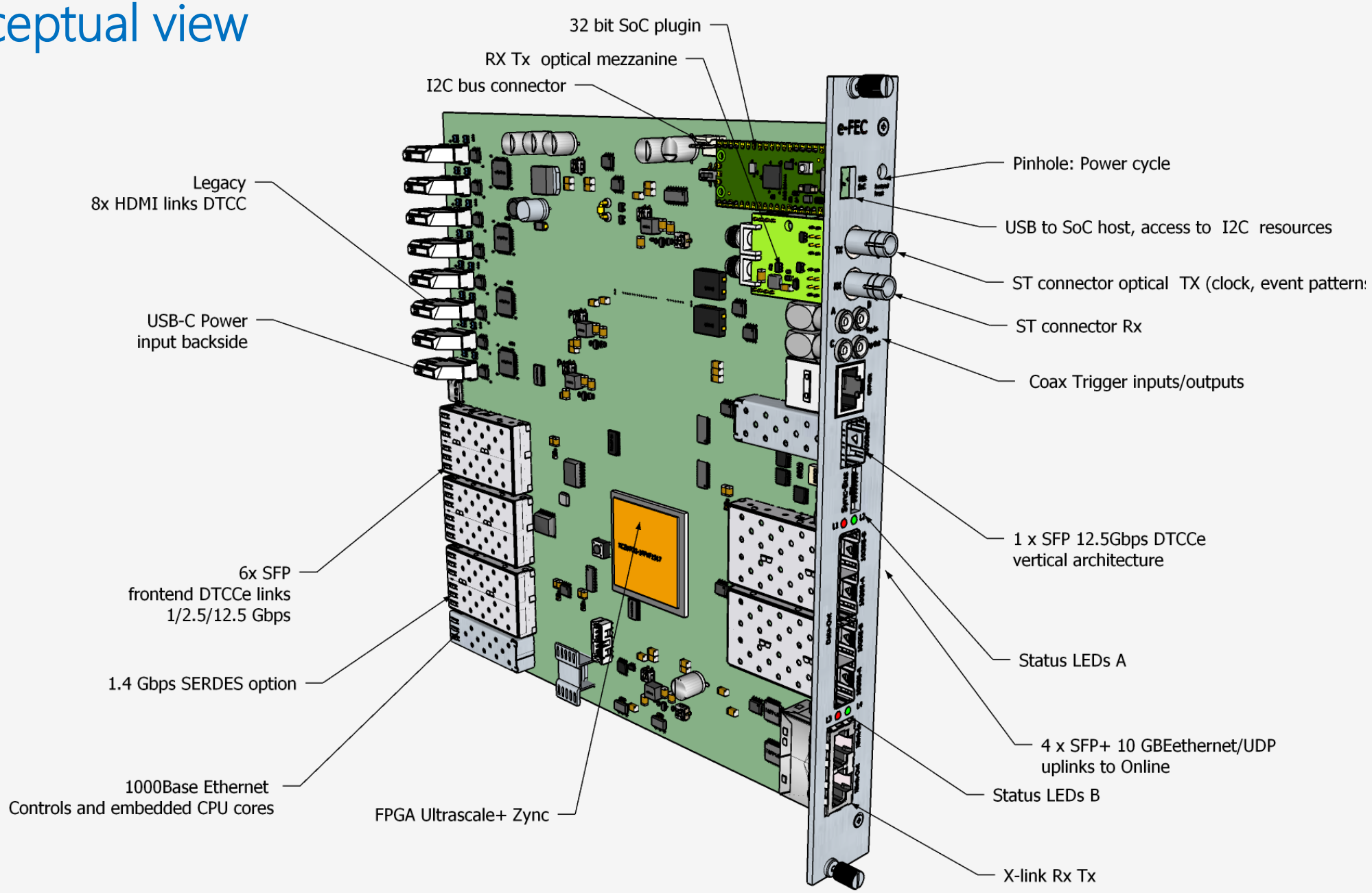


Rubén Caballer, MsC student

eFEC schematics and routing

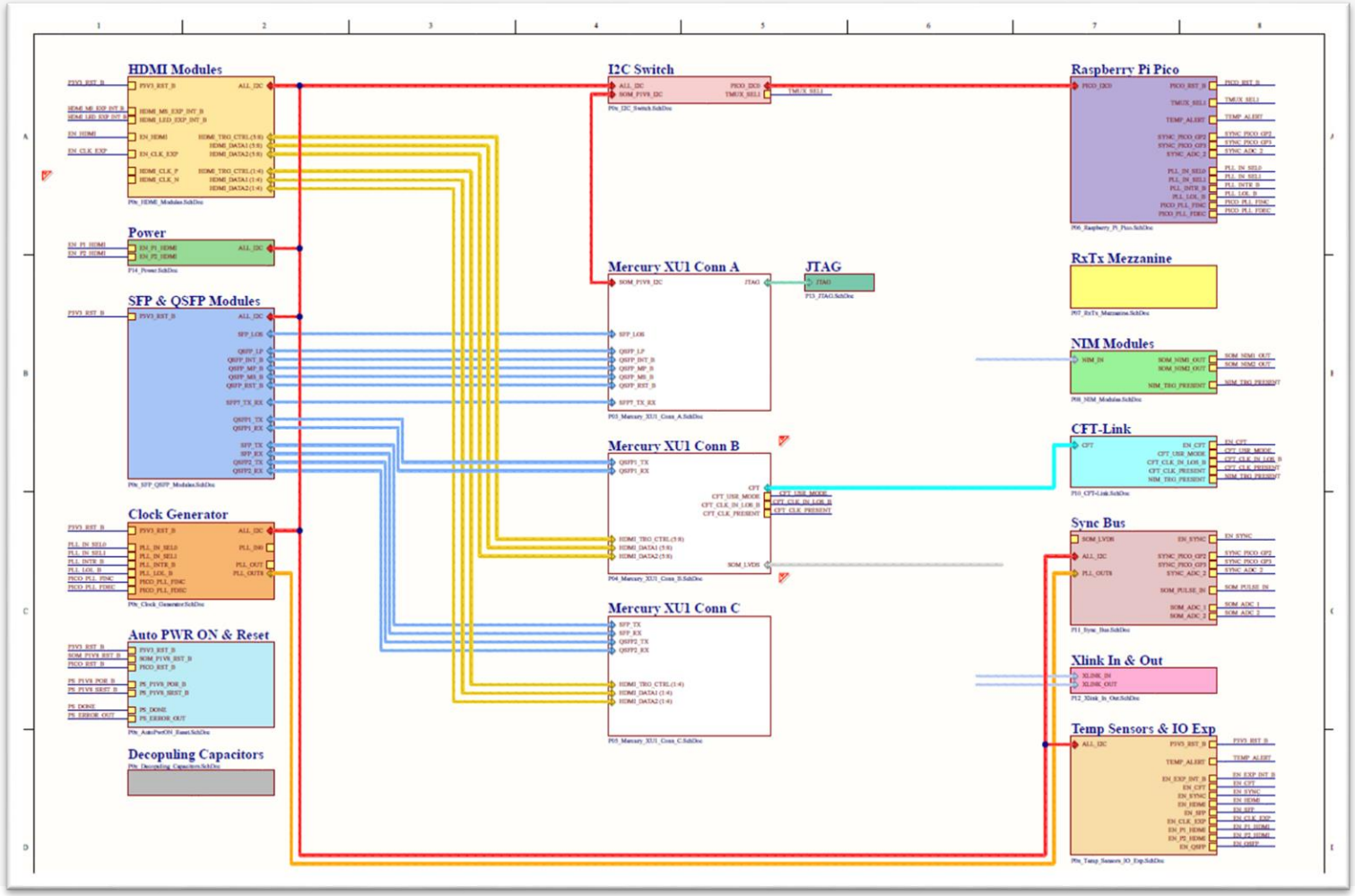


eFEC conceptual view



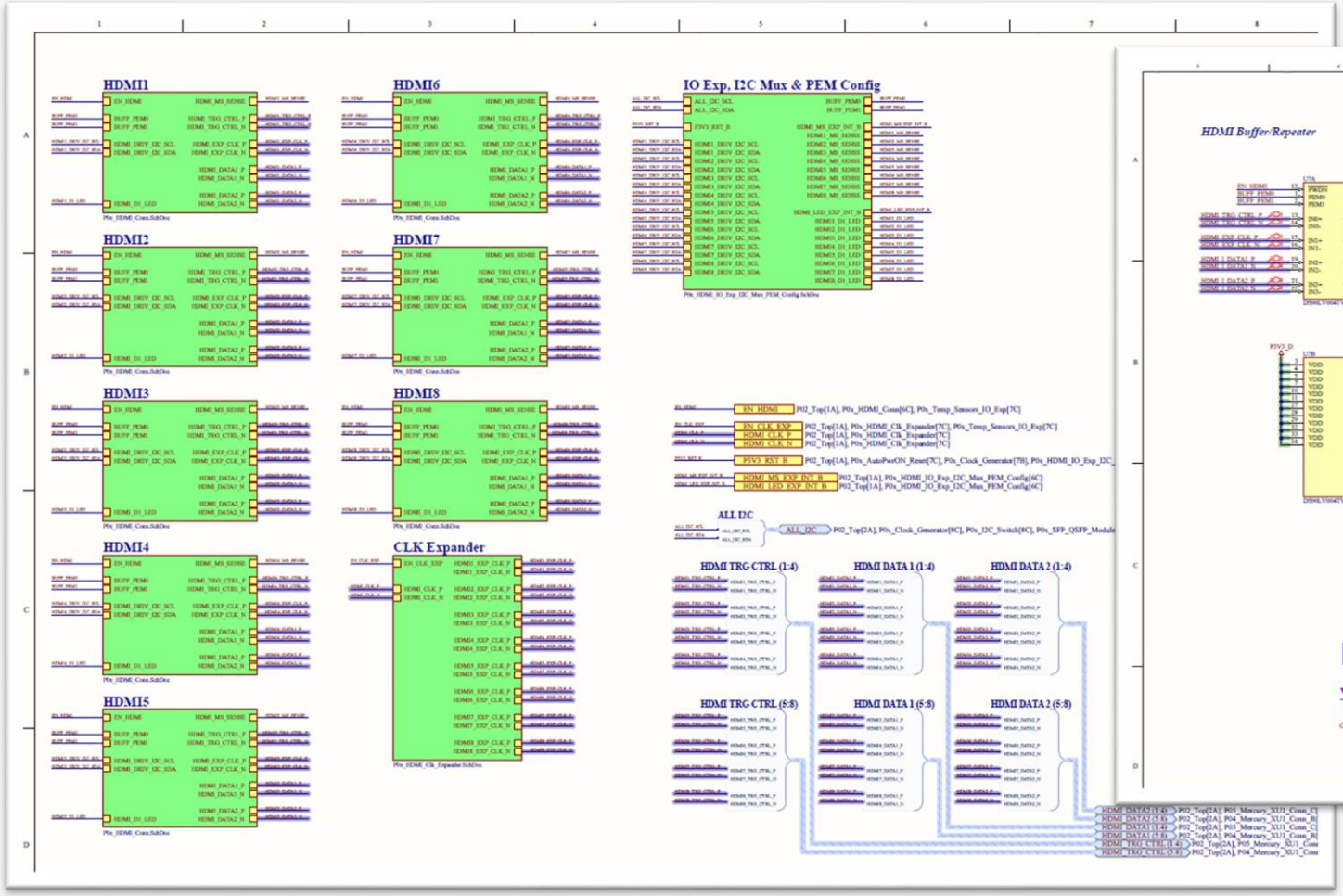
eFEC design

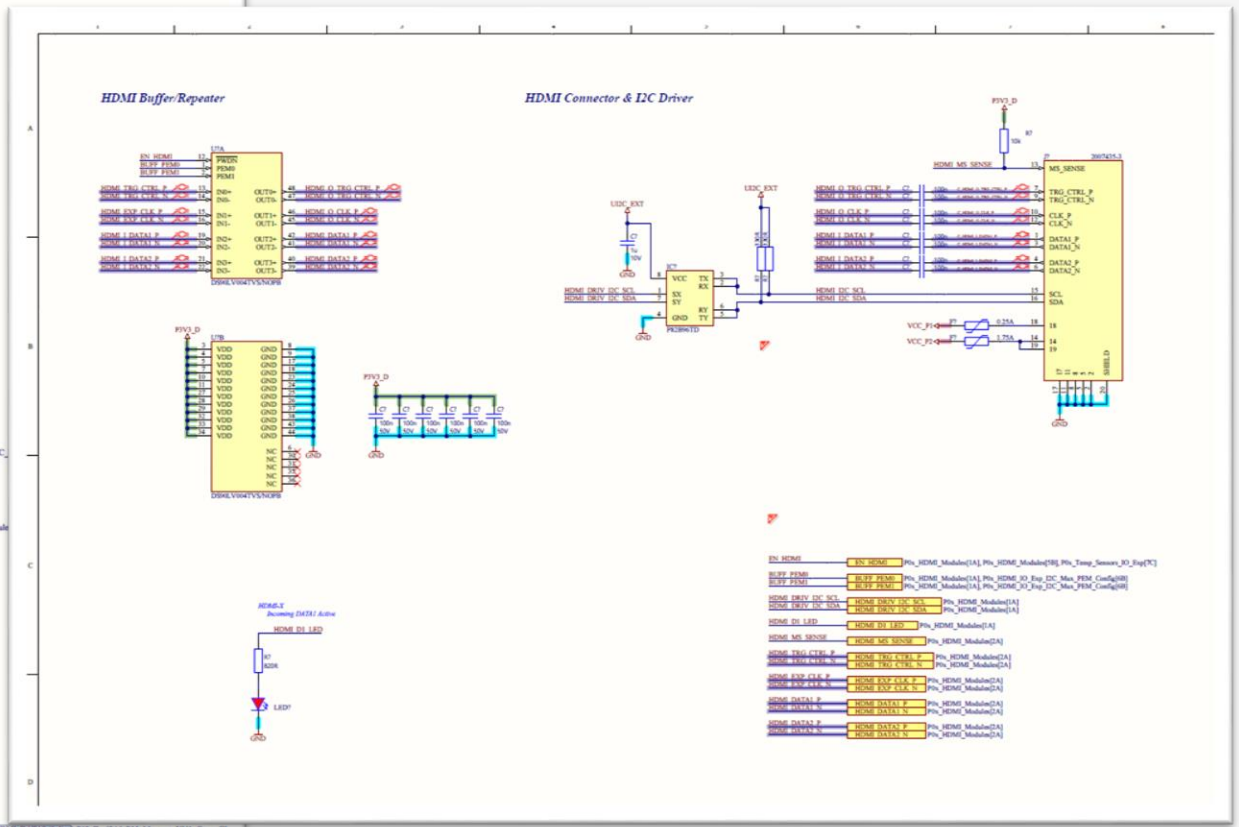
- Schematics
  - Top-down approach, translating specifications from Hans into schematic pages and completing the design



eFEC design

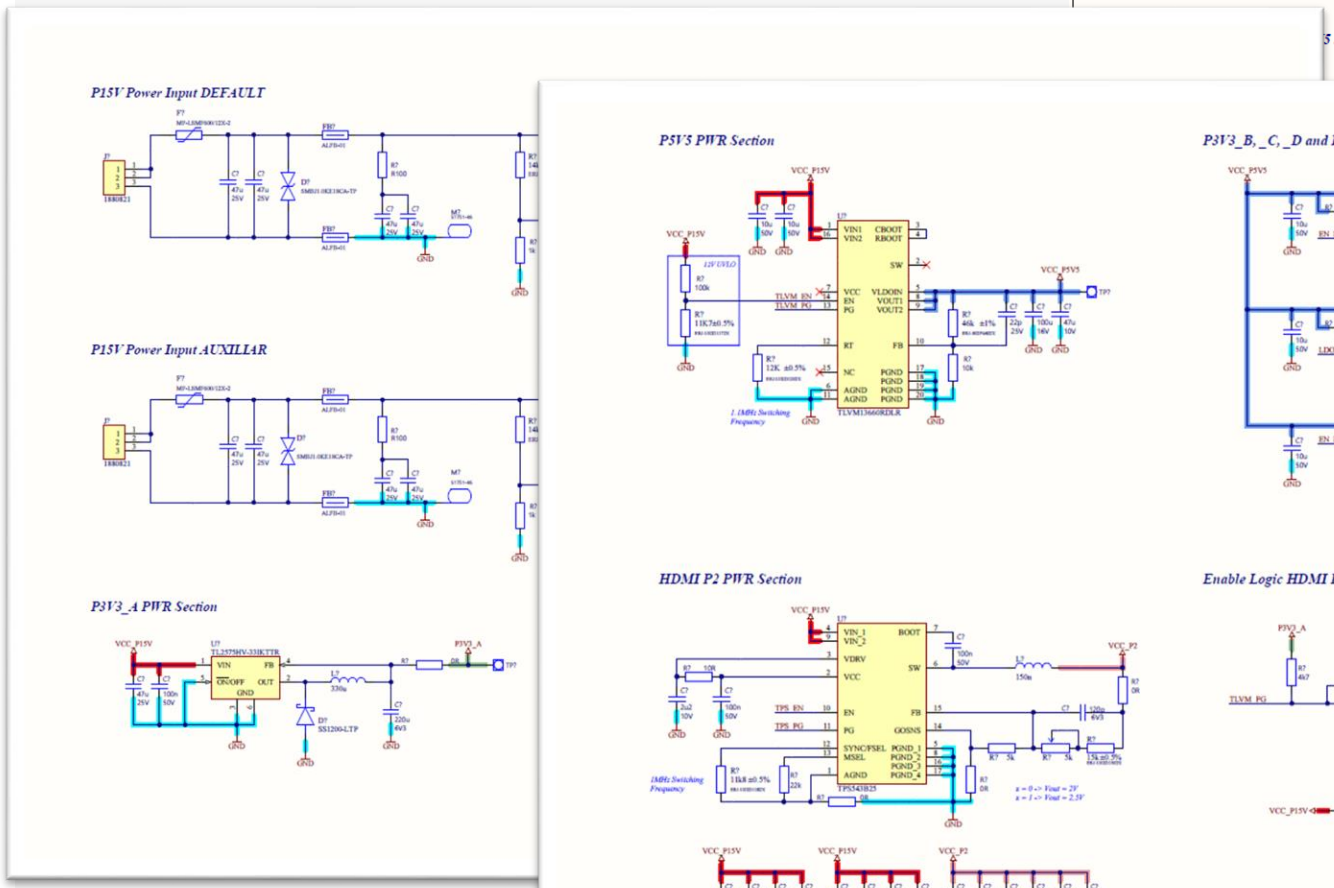
- Schematics
  - I/O blocks are advanced (not ready for external review yet)





eFEC design

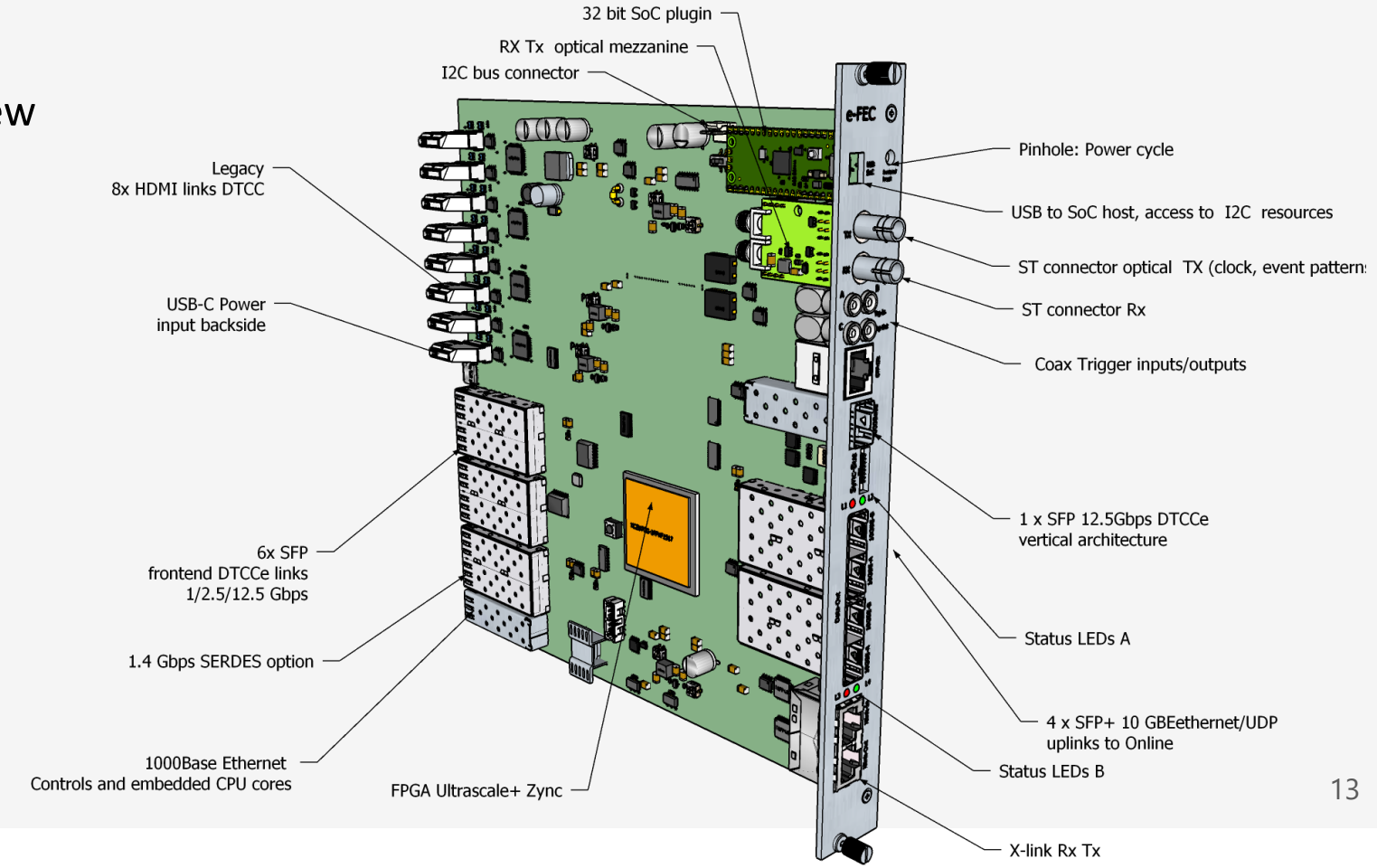
- Schematics
  - Power system is progressing



eFEC design

- Milestones for coming weeks
  - Reuse Zynq Ultrascale+ design files from Open hardware [DI/OT Zynq Ulrtscale+ board]

    This allows to avoid the SoM option and dramatically reduce the eFEC cost
  - I/O blocks ready for review
  - Power subsystem ready for review



Summary

- Manpower: 2 full-time engineers + coordinator
- Goals:
  - Schematics design
  - Advance bord layout as much as possible (tbd: Will we need additional help?)
  - Implement basic functional FW&SW on Zynq Ultrascale+

Thanks for your attention!