

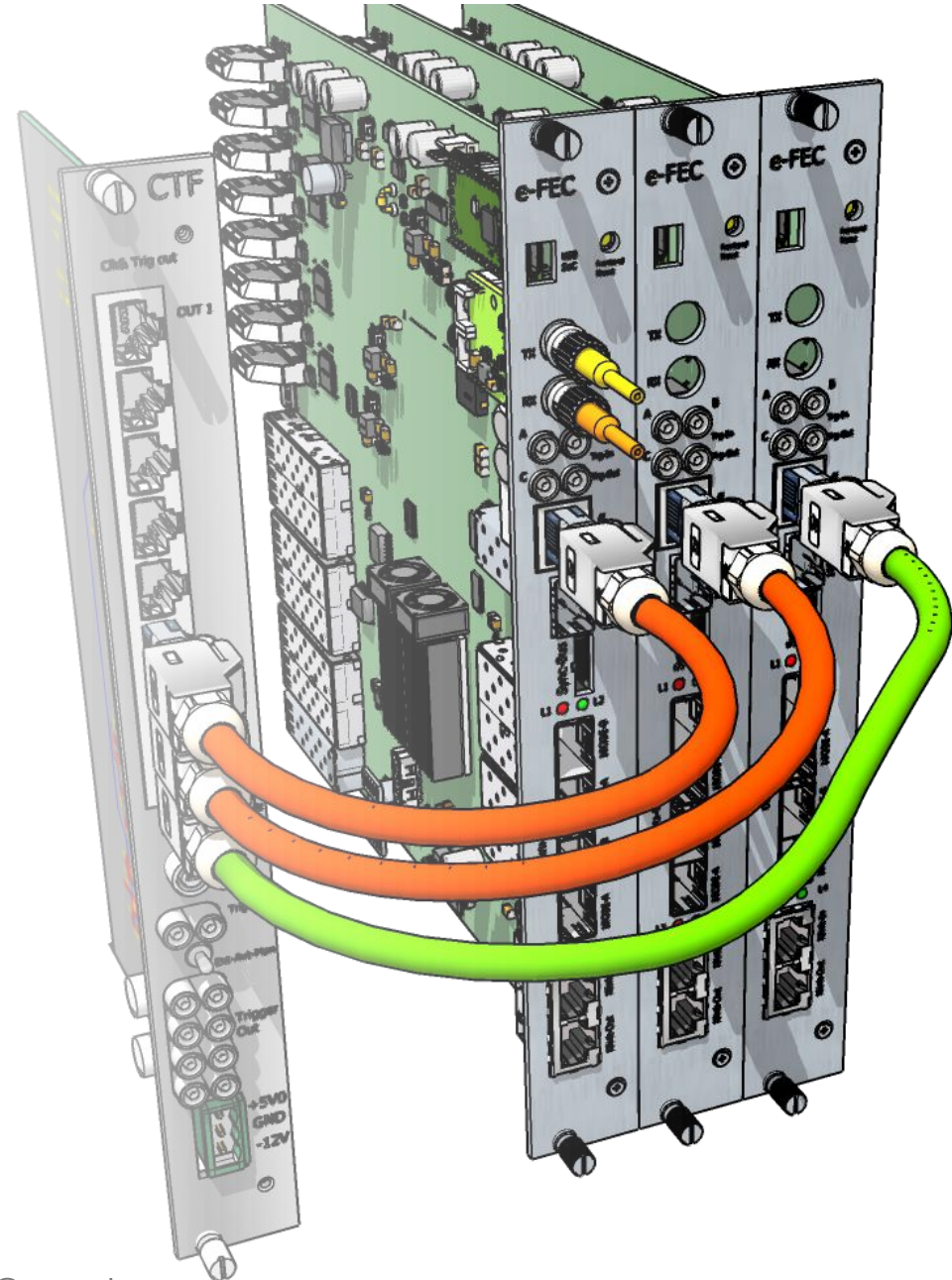
# SRSe: clock, trigger and power distribution

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3<sup>rd</sup> DRD1 Coll meeting WG5 December 24

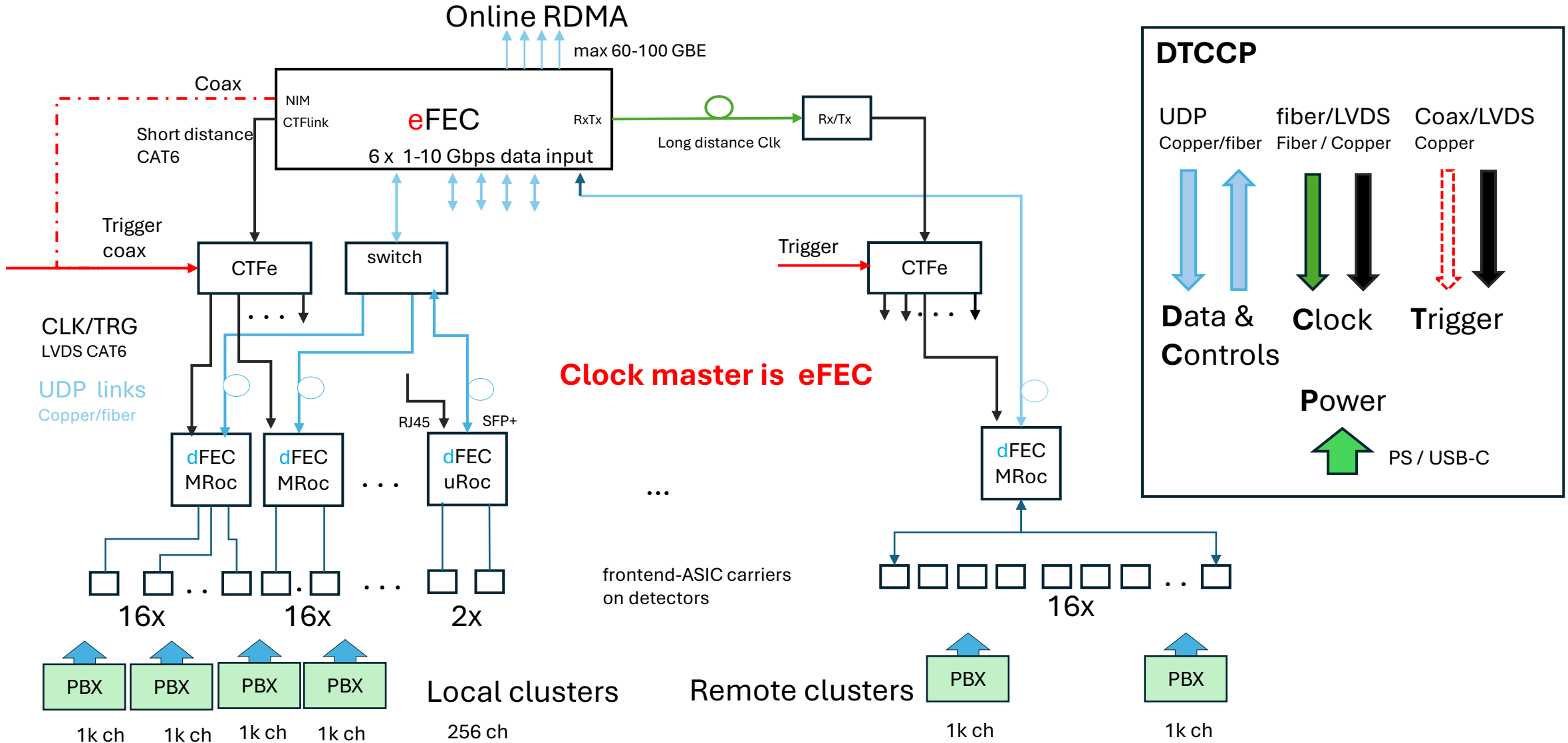
? What is SRS ?

## eFEC backend common clock from experiment



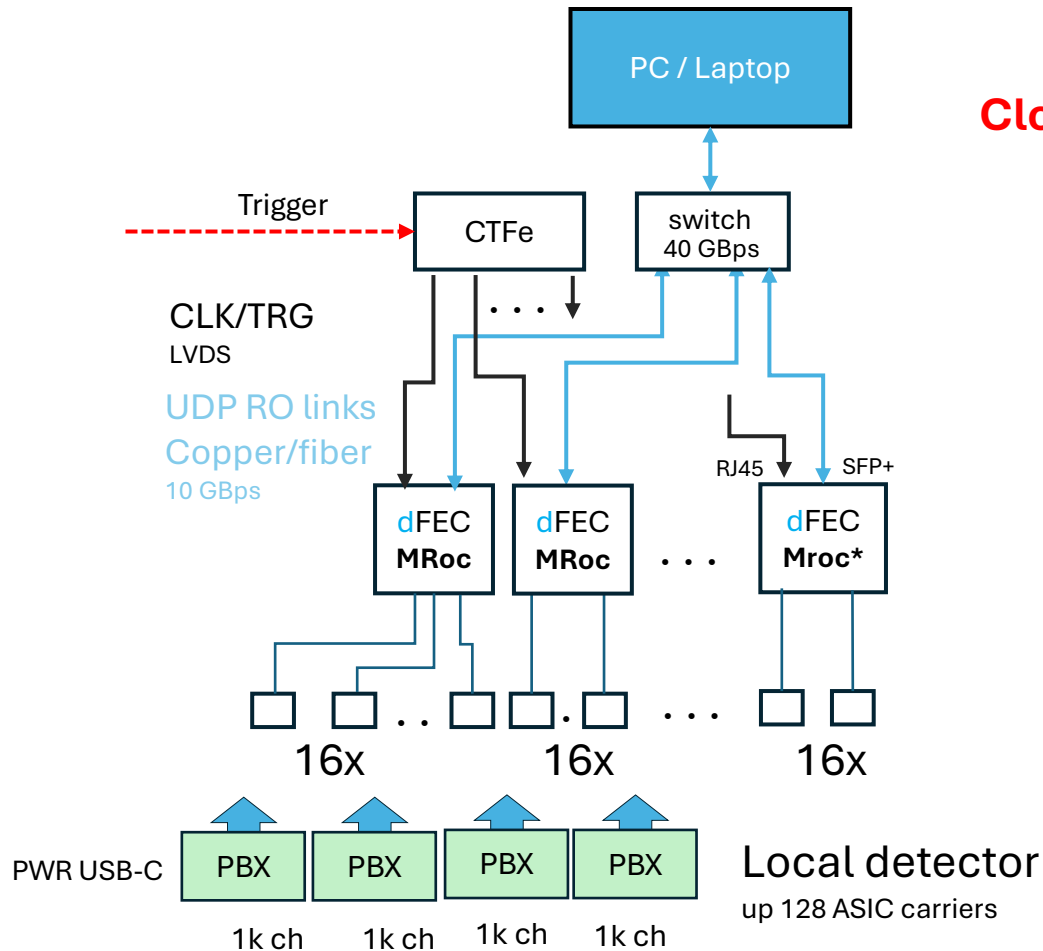
- For participation in the bi-weekly meetings on **SRS-e development** contact Sorin Martoiu for authorization access to Indico

# Scalable Readout Architecture



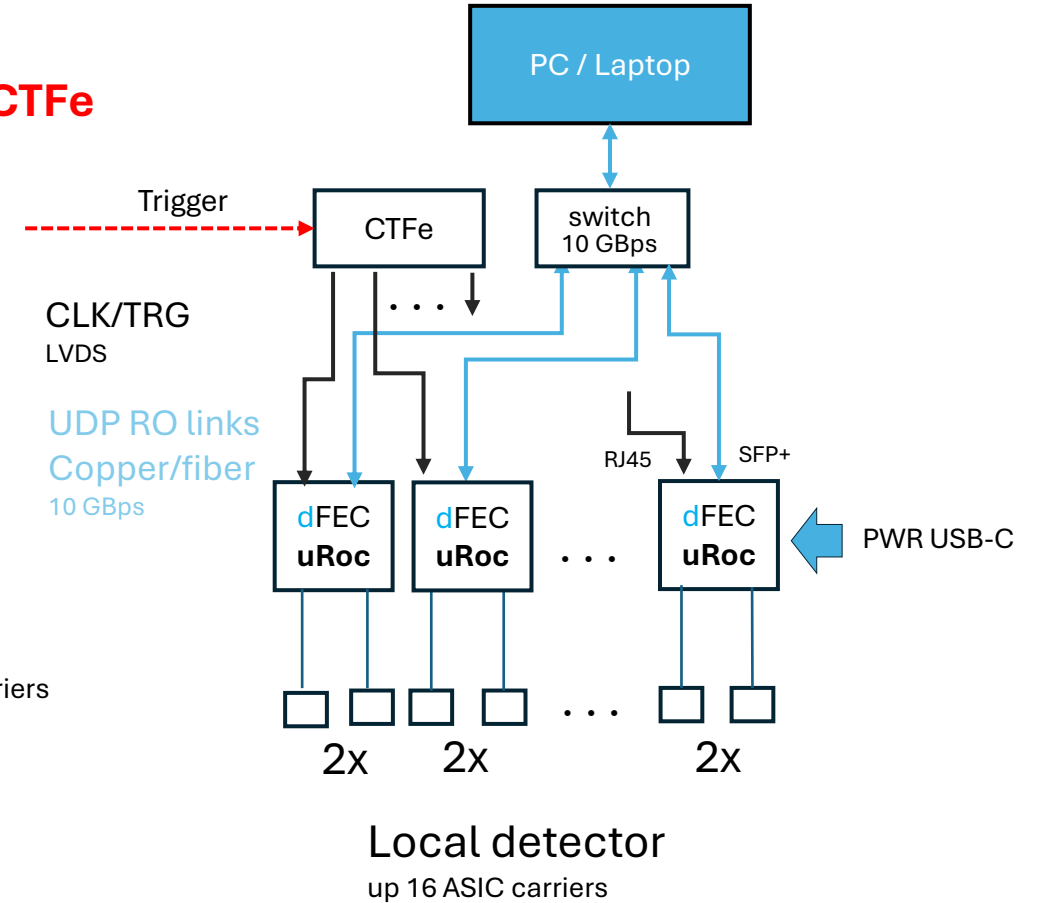
# Downscaled Architectures

## small systems without backend



**Clock master is CTFe**

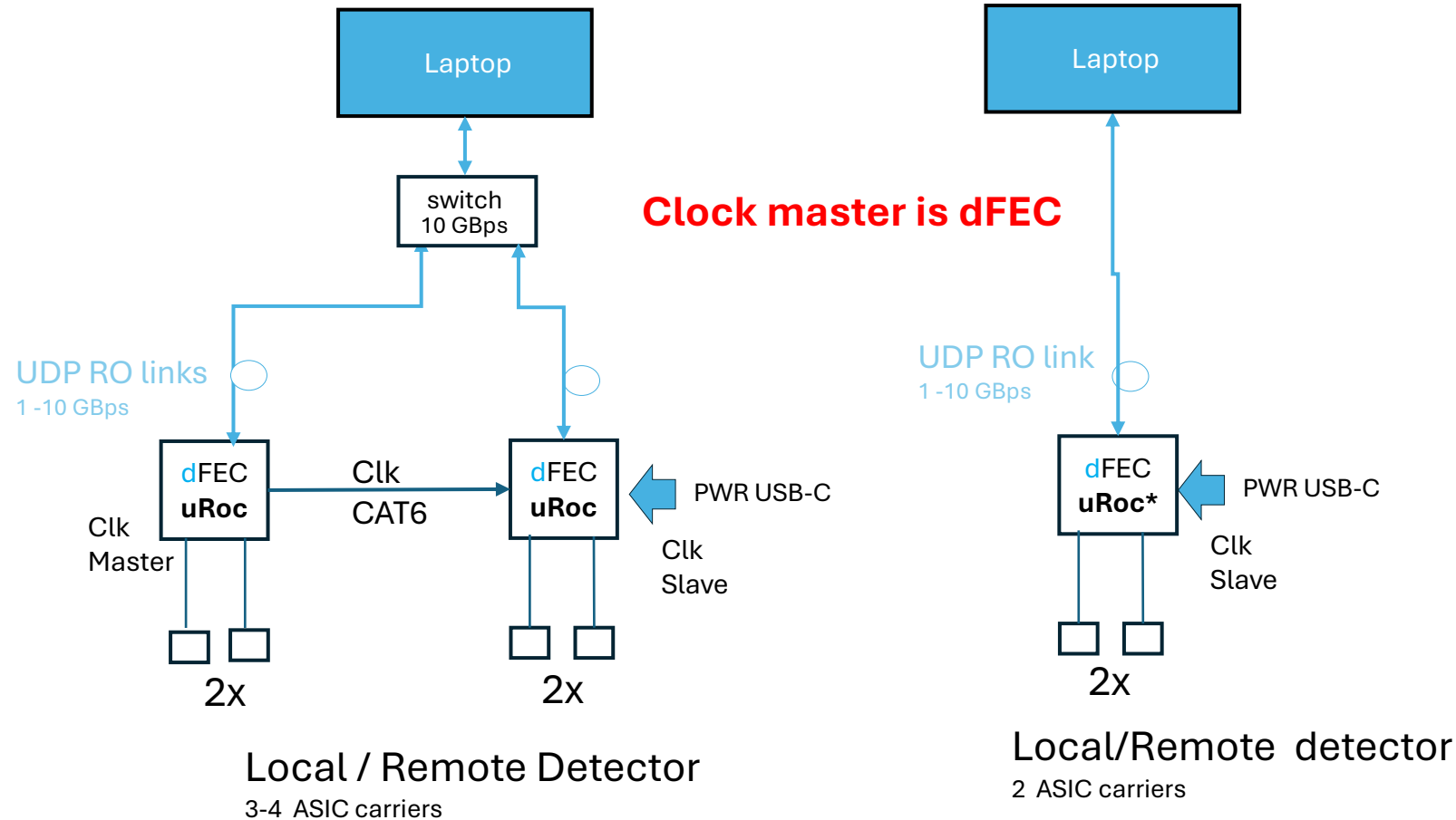
frontend-ASIC carriers on detectors



\* MRoc and uRoc: see presentation A.Rusu

# Downscaled Architectures

## very small triggerless systems



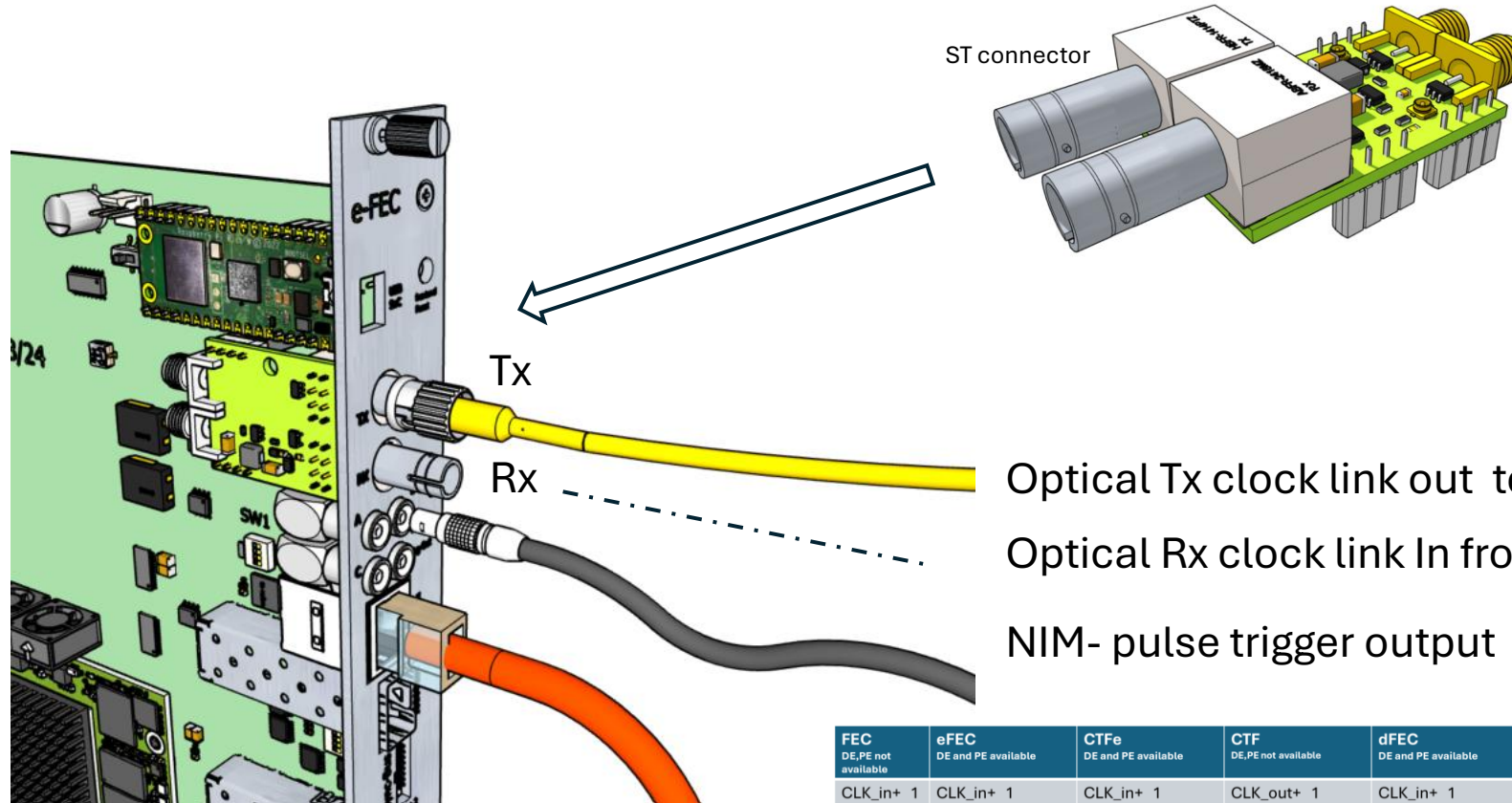
Note:

Same DAQ software for all downscaled architectures

DAQ for large eFEC backend tbd

\* uROC: see presentation A.Rusu

# eFEC as clock and trigger master



**Rx-Tx optical<->copper Mezzanine with loopback option**

*G50/125 multimode Fiber , 0.8db/m max 900m*

*G62.5/125 multimode Fiber , max 2000m*

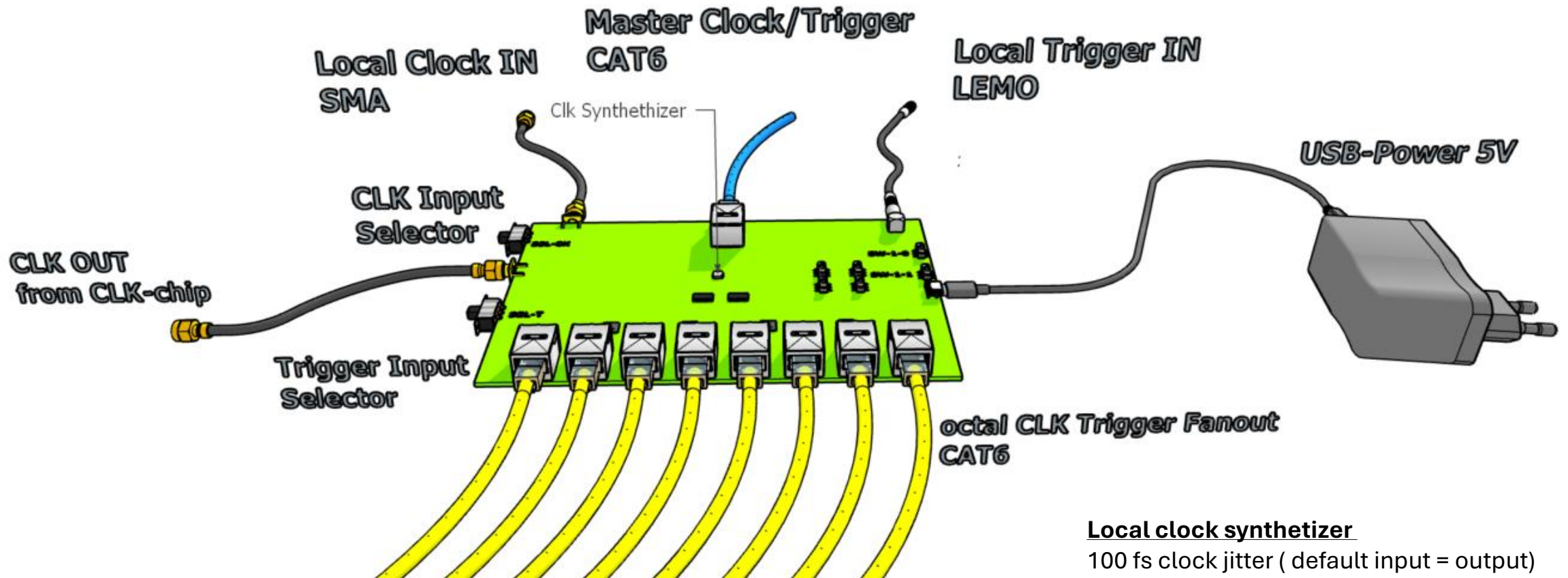
Optical Tx clock link out to remote CTFe  
 Optical Rx clock link In from remote CTFe (ring)  
 NIM- pulse trigger output CTFe (optional)

**Clock & trigger link to local CTFe CAT6 LVDS**

FEC DE,PE not available	eFEC DE and PE available	CTFe DE and PE available	CTF DE,PE not available	dFEC DE and PE available
CLK_in+ 1 CLK_in- 2	CLK_in+ 1 CLK_in- 2	CLK_in+ 1 CLK_in- 2	CLK_out+ 1 CLK_out- 2	CLK_in+ 1 CLK_in- 2
TRG_in+ 3 TRG_IN- 6	TRG_in+ 7 TRG_in- 8	TRG_in+ 7 TRG_in- 8	TRG_out+ 3 TRG_out- 6	TRG_in+ 7 TRG_in- 8
N.A.	TRG_out+ 4 TRG_out- 5	TRG_out+ 4 TRG_out- 5	N.A.	TRG_out+ 4 TRG_out- 5
N.A.	CLK_out+ 3 CLK_out- 6	CLK_out+ 3 CLK_out- 6	N.A.	CLK_out+ 3 CLK_out- 6



# CTFe box\* : a versatile clock synthesizer and trigger fanout

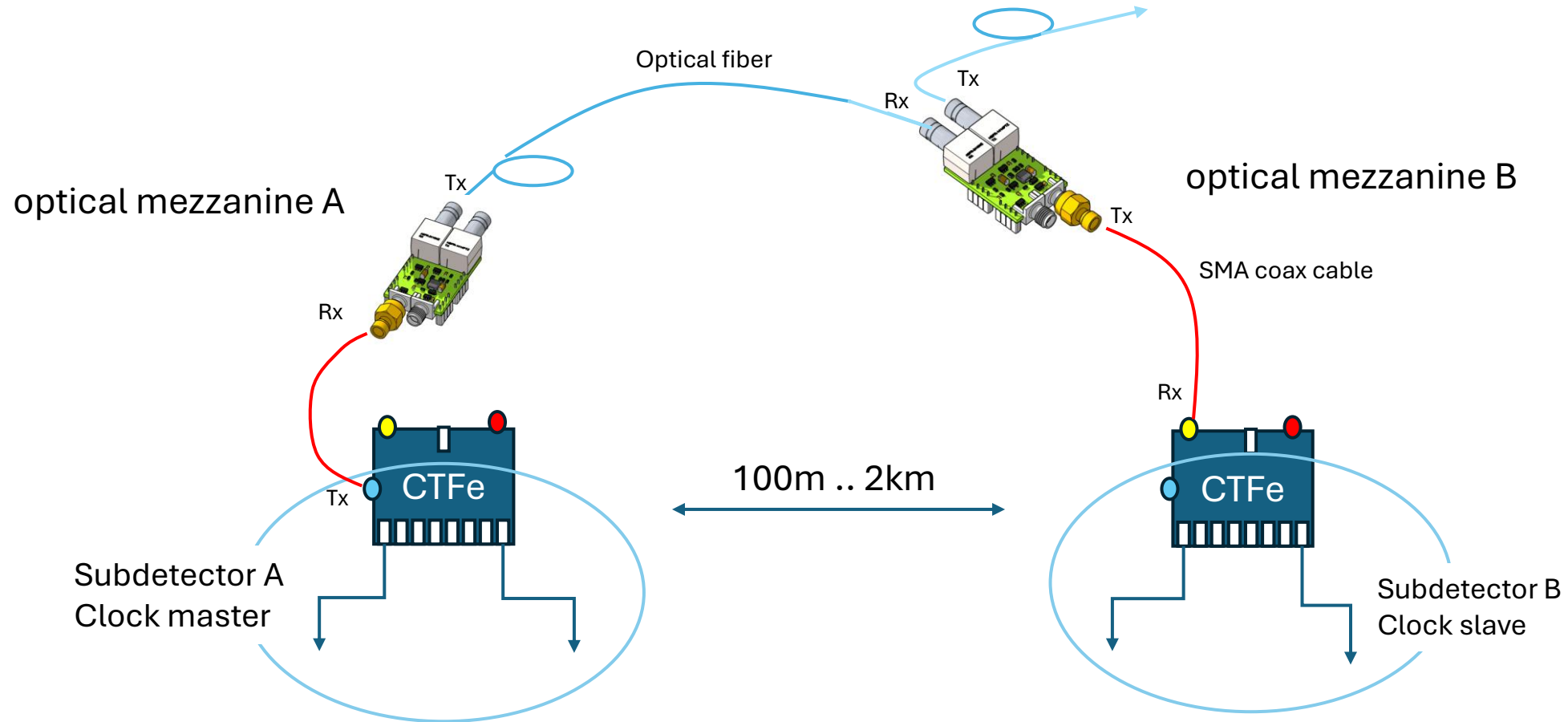


### Local clock synthetizer

100 fs clock jitter ( default input = output)  
programmable 100Hz-0.25 GHz

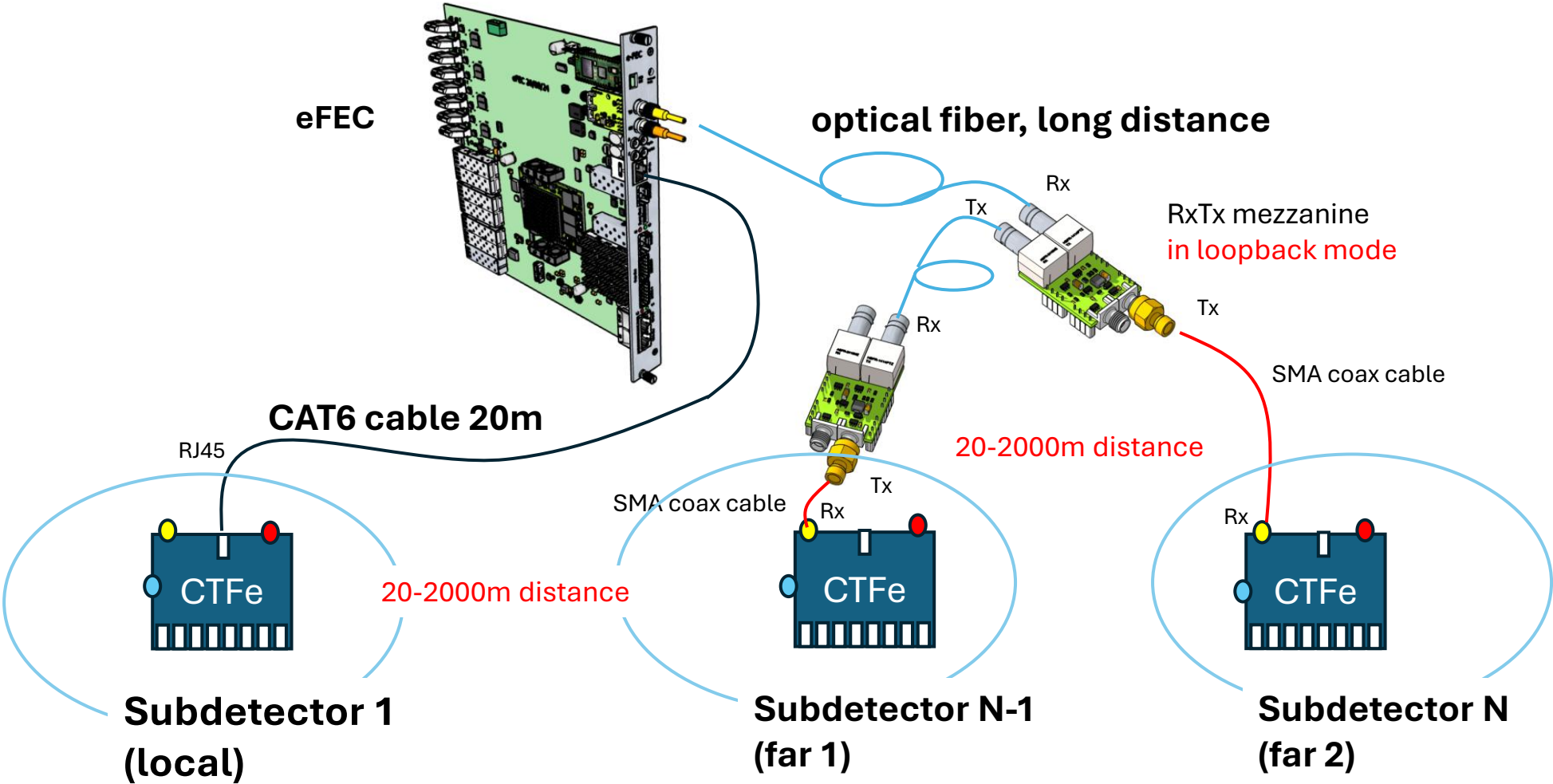
\* CTFe: see prenentation A.Rusu

# Long distance daisy chained clock

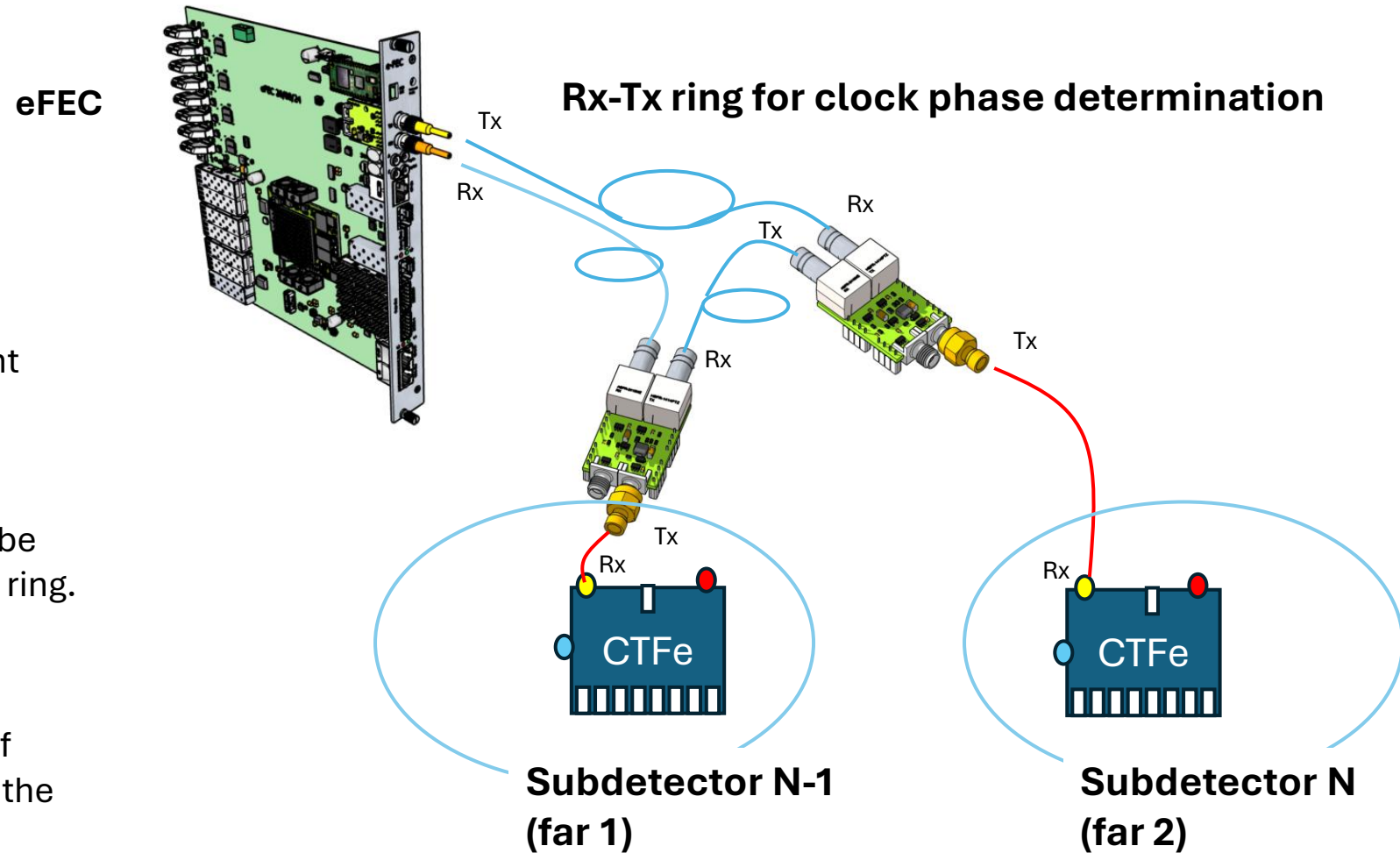




# Mixed short/long clock clusters



# Clock rings for clock phase measurement



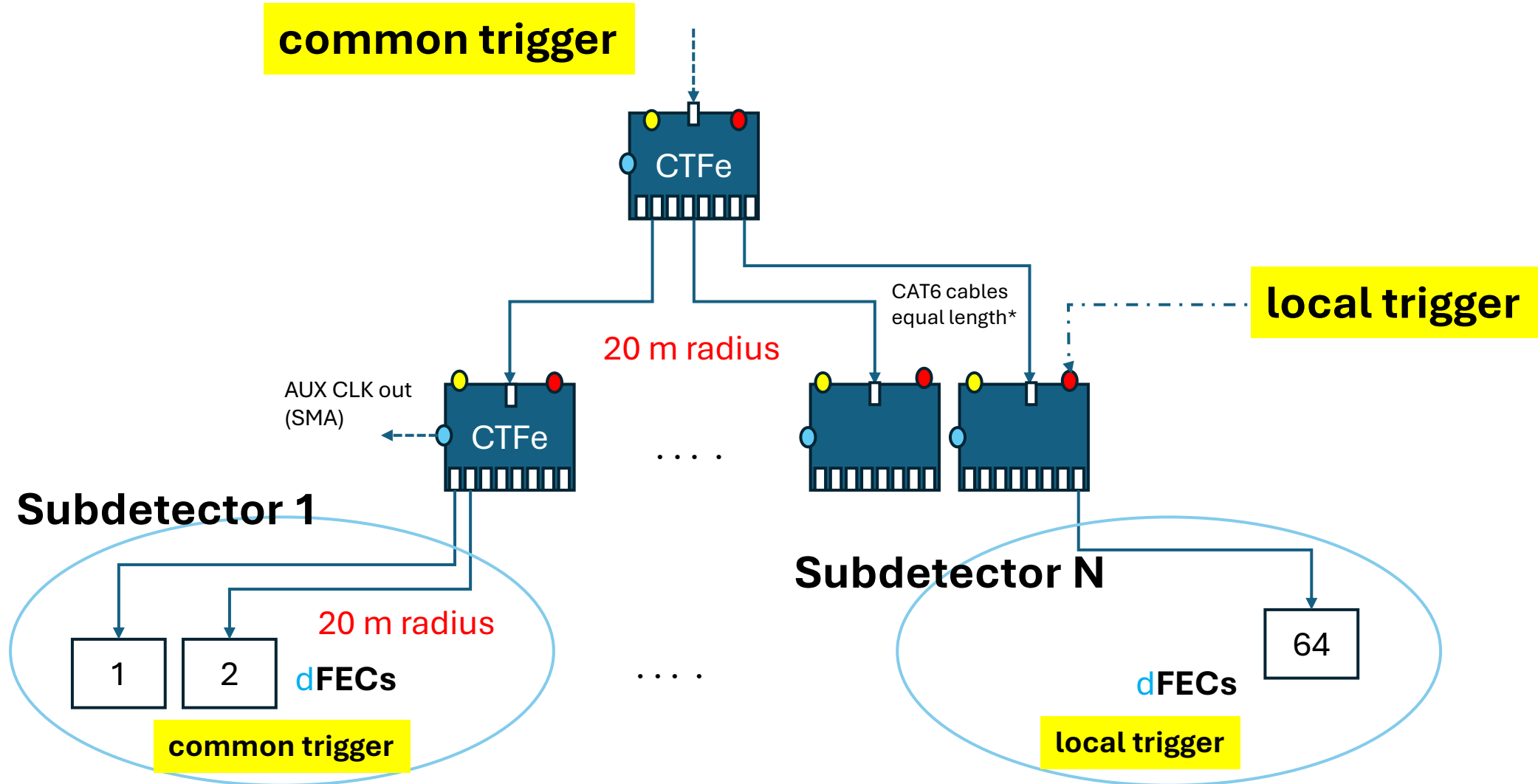
Clock phases  $\Phi$  are constant timestamp corrections.

The Clk phase of  $\alpha$  remotely connected subdetector can be measured via a Tx-Rx clock ring.

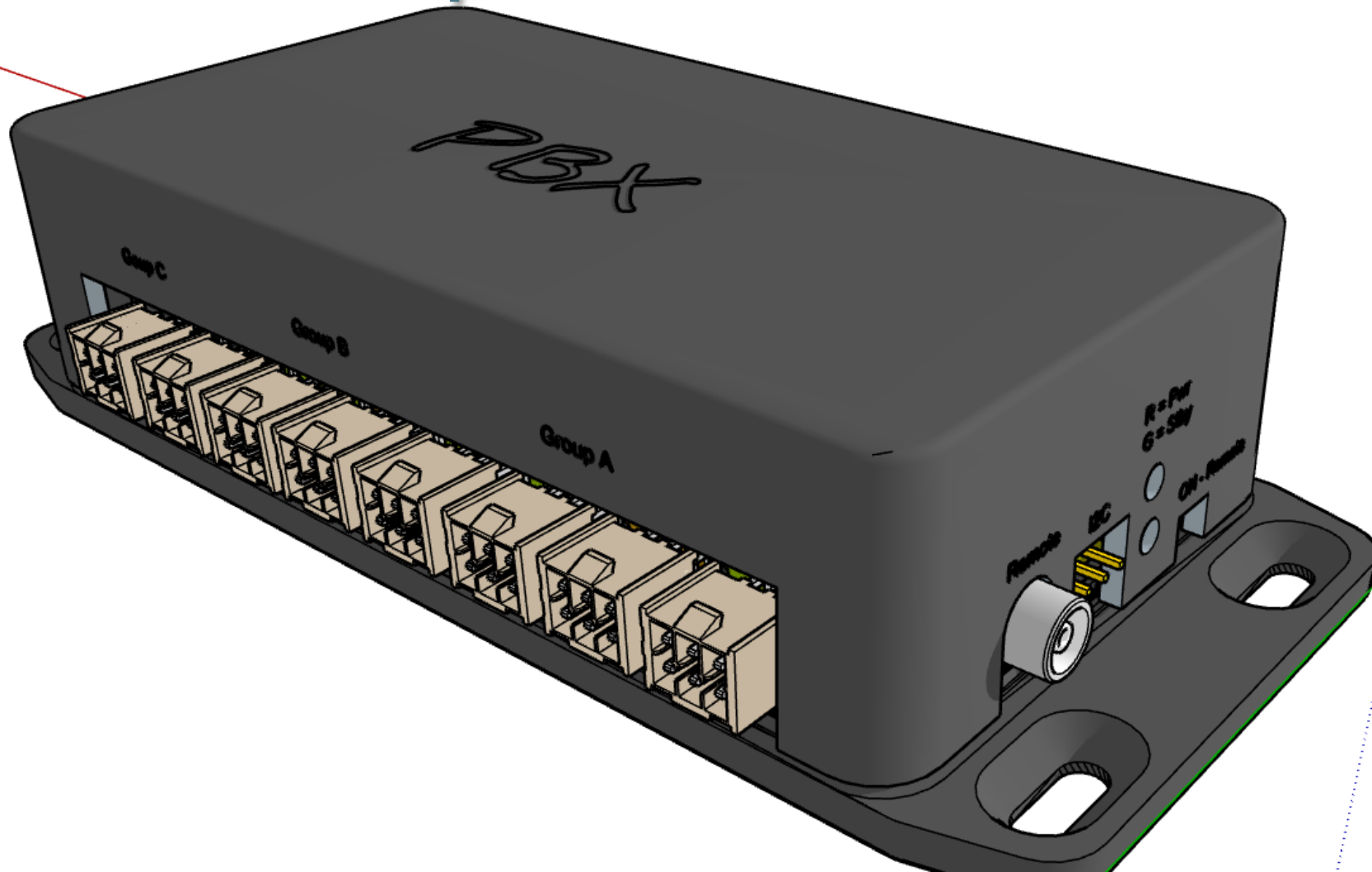
$$\Phi = \frac{\text{Tx}-\text{Rx}}{2}$$

Incremental measurement of roundtrip delays determine the additional phase of added detectors

# Subdetector triggers



# The PBX powerbox



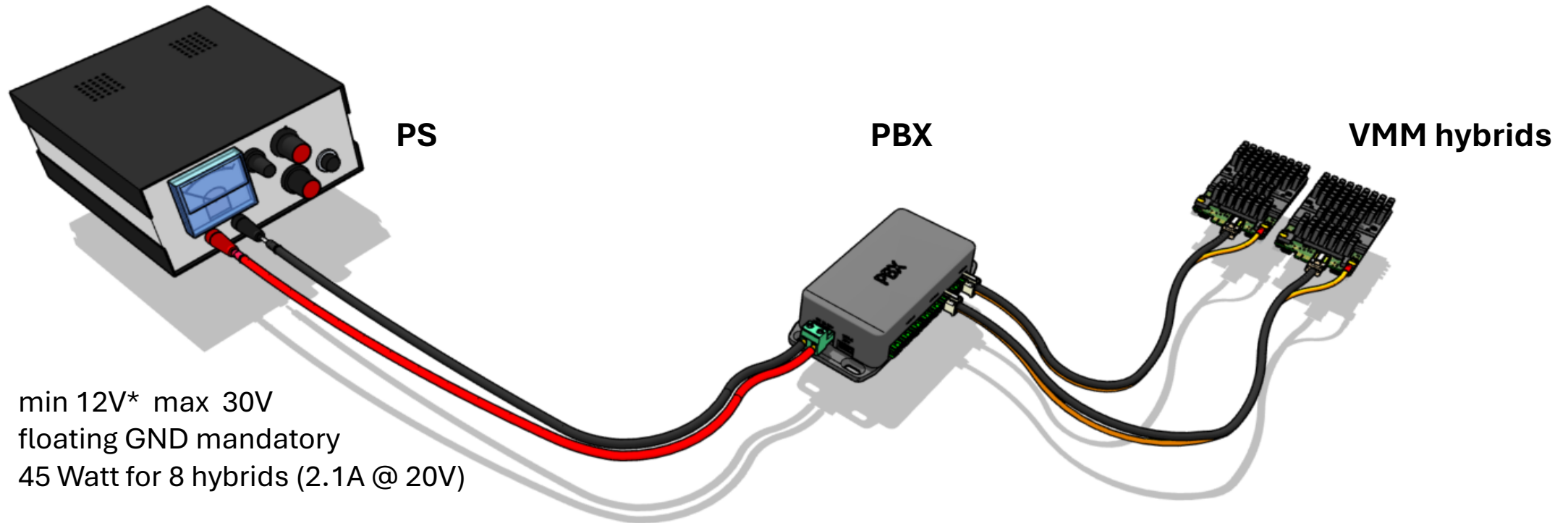
**Analogue and Digital power for FE ASIC carriers.**

**Primary power  
USB-C PD or PS 45W**

**Digital P1\* 3V3 @ 5A  
Analogue P2 3 x 1.8V @ 5A**

- Both voltages can be adjusted in a range +/-30% via internal trimmers. An external I2C master can read the Voltages and PCB temperature

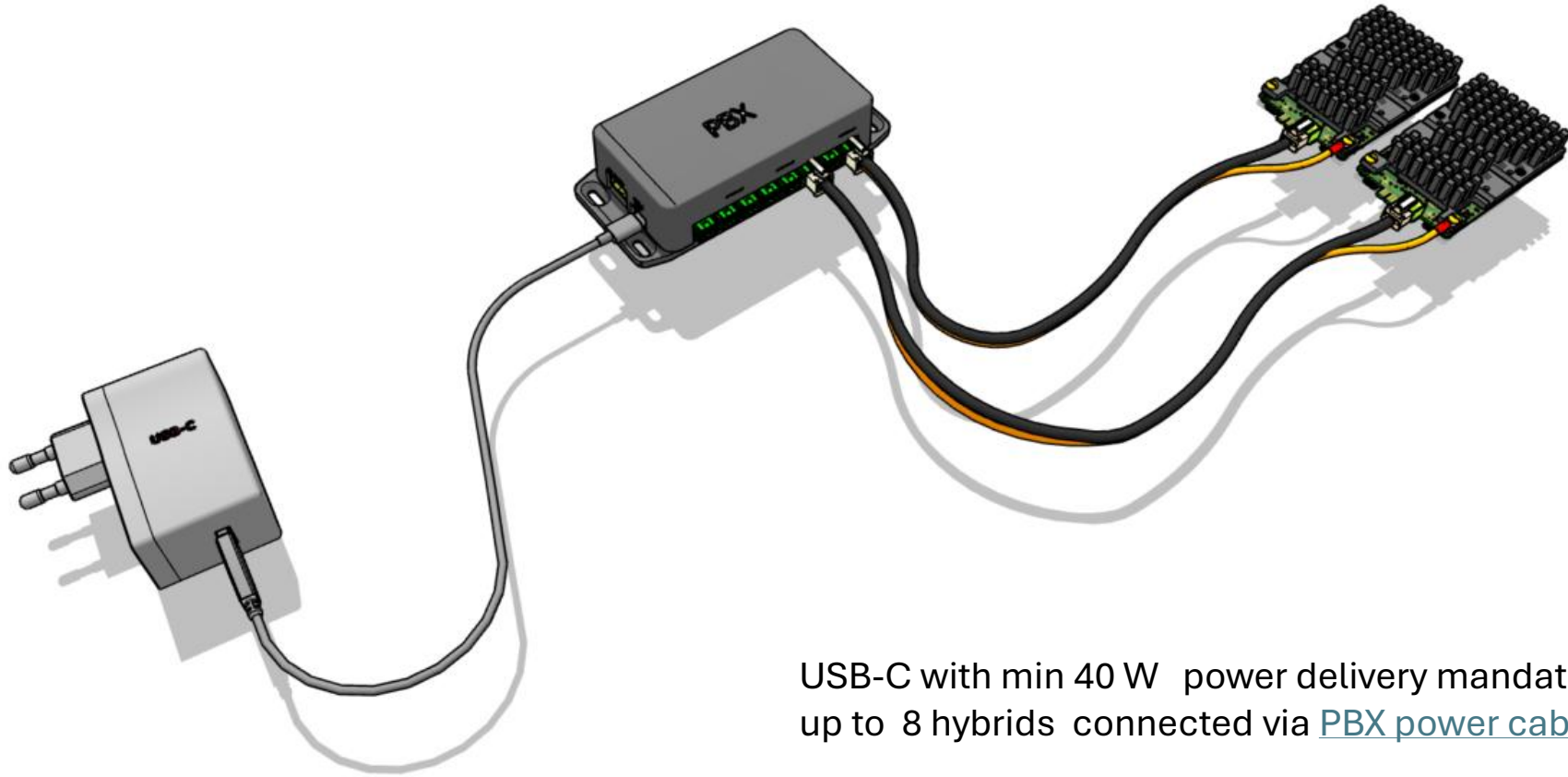
# Powersupply operation



- High current below 12 V inhibited by circuitry
- 2-pin Phoenix cable connector 1766990
- reverse polarity protection
- higher voltage minimizes power loss over cable

up to 8 hybrids connected via PBX power cables 1 .. 3m  
For cooling (max 6W loss) attach PBX to a dissipative rack or detector frame

# USB-C operation

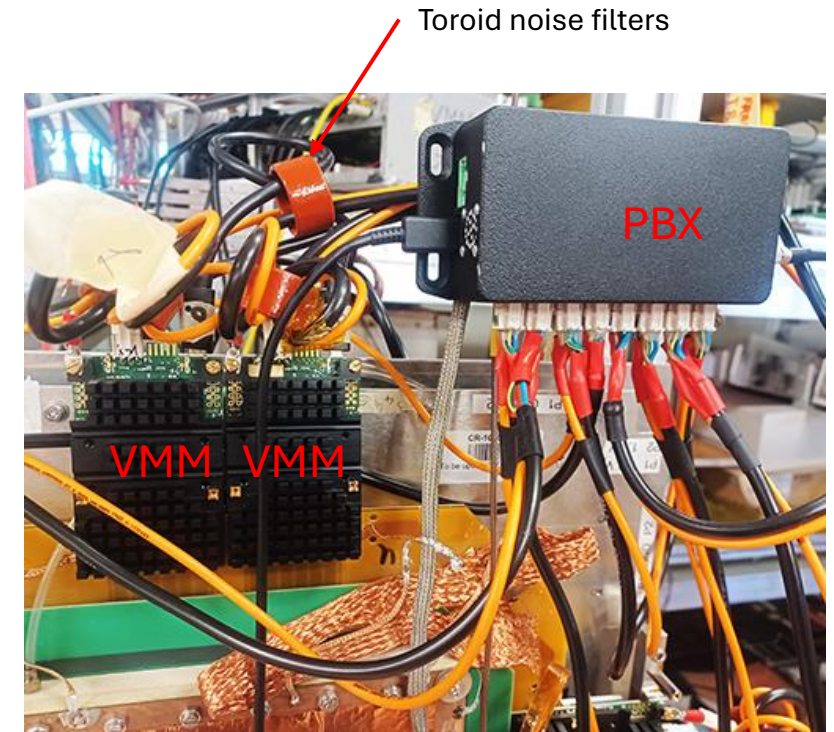
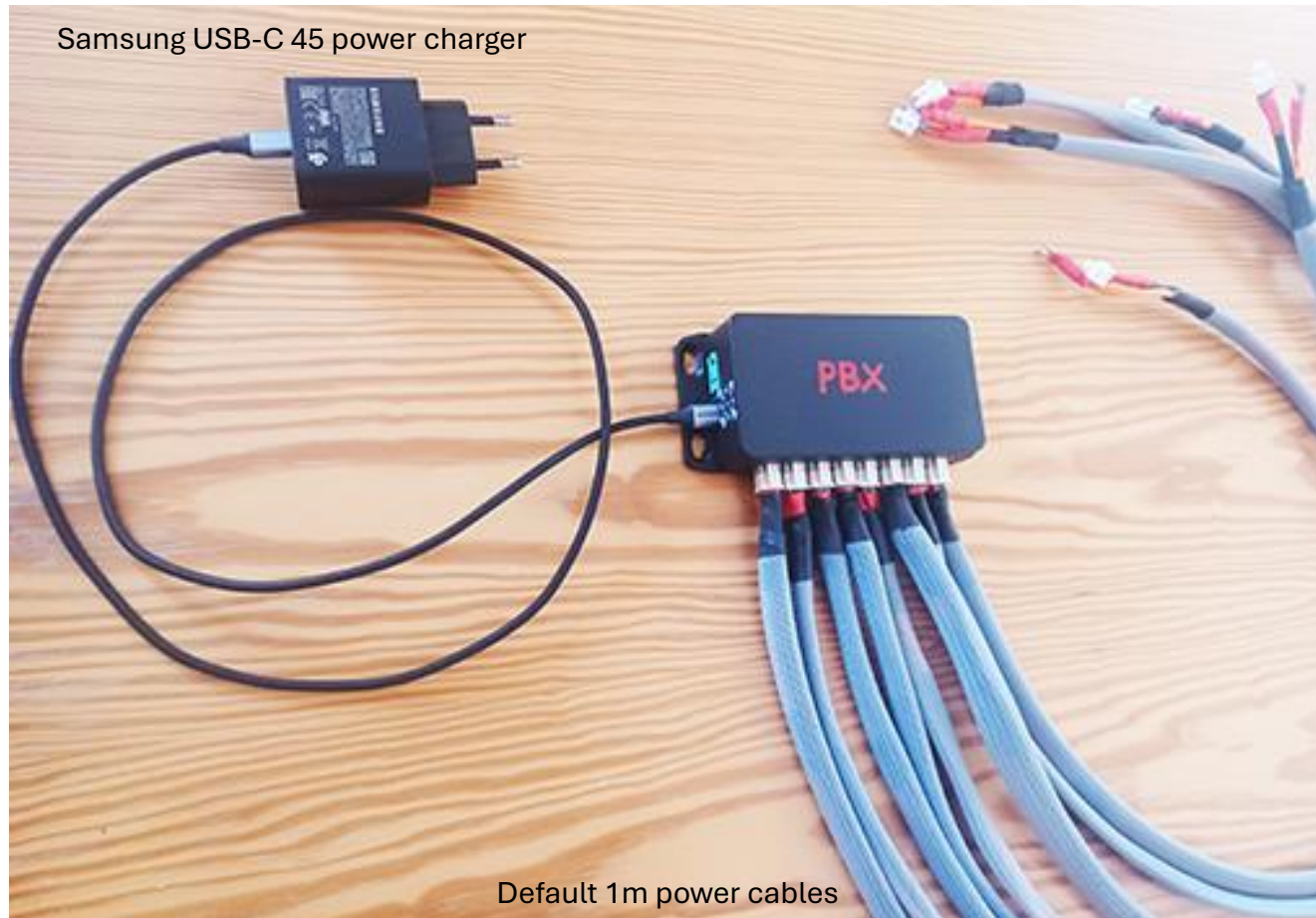


USB-C with min 40 W power delivery mandatory  
up to 8 hybrids connected via [PBX power cables](#) 1 .. 3m

- USB-C PD chargers min. 45W ( 20V capability) Samsung, Ikea...
- For uninterruptible backup connect Li 18V or 12V car battery simultaneously



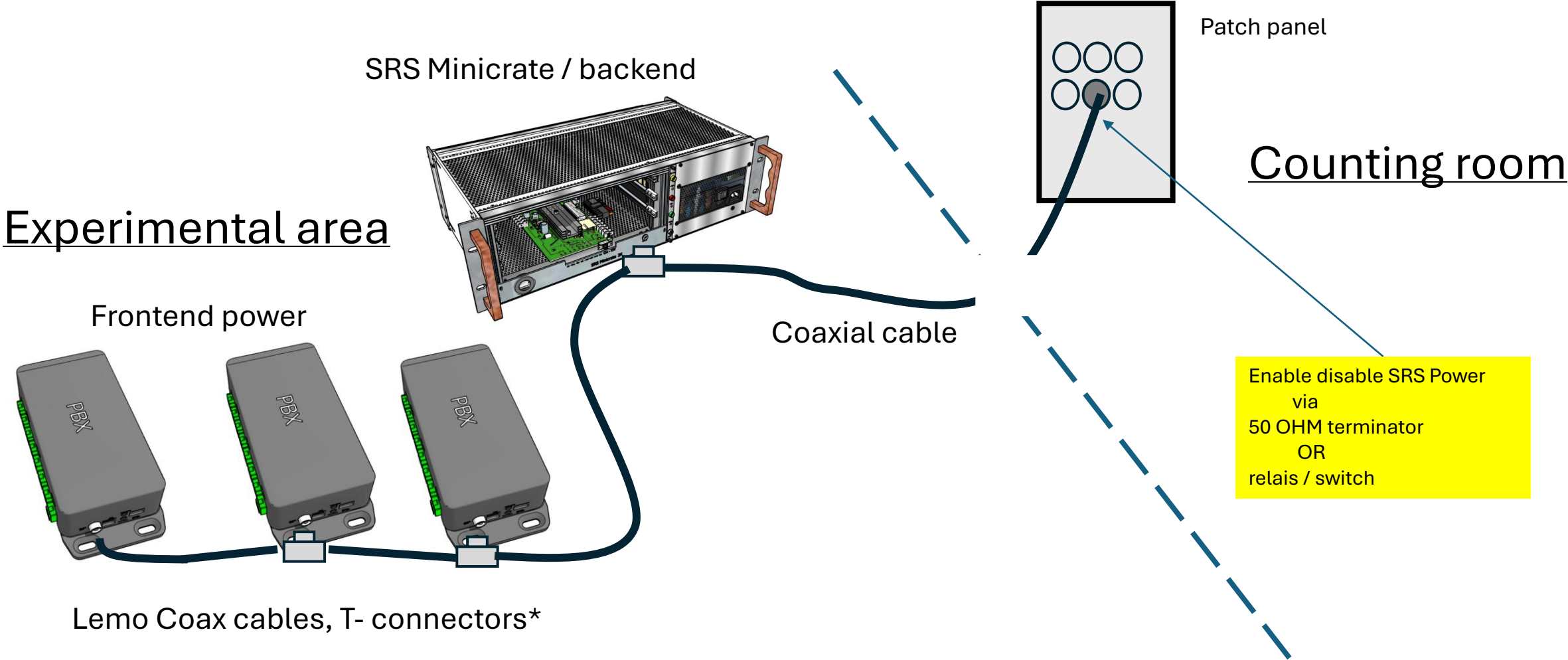
# Photo PBX for GEM tracker



**Digital and Analogue power P1+P2 for 8 x VMM hybrids ( 1k ch) from a 45 W USB-PD charger.**



# PBX remote SRS Power control



- GND loop and overvoltage protection via Insulated Coax input on Rev 1.2

Thank you!