# Readout electronics of the TGC detectors in ATLAS

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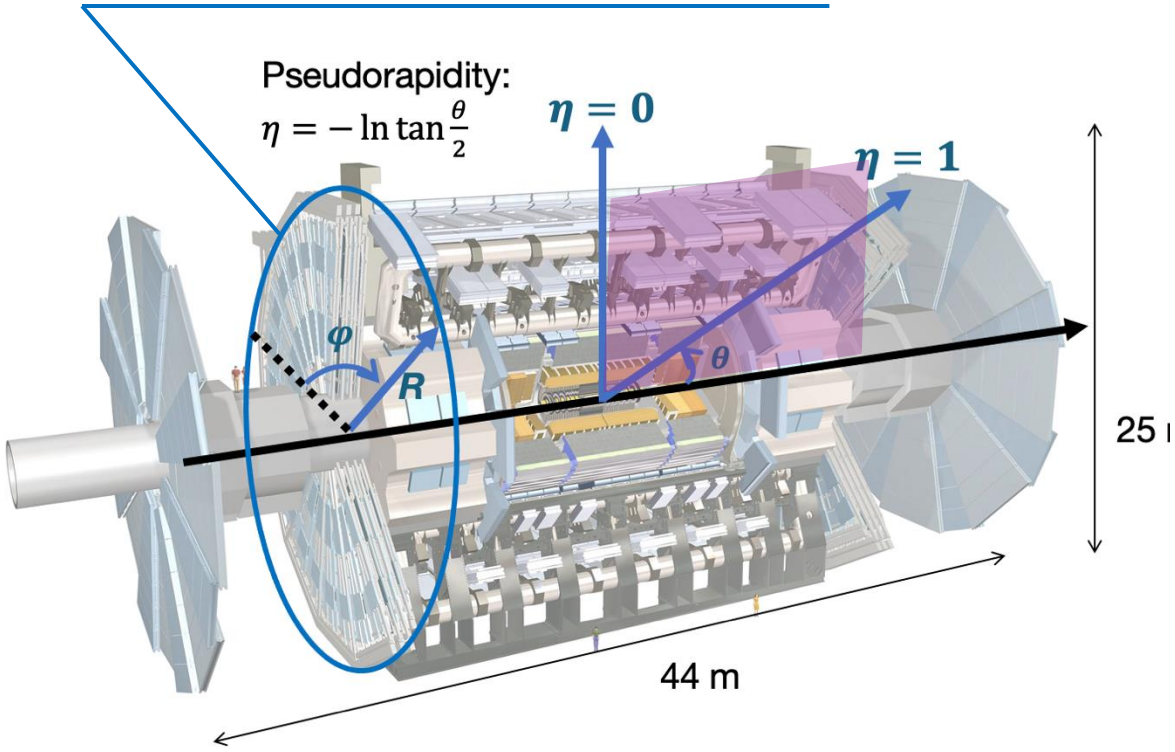
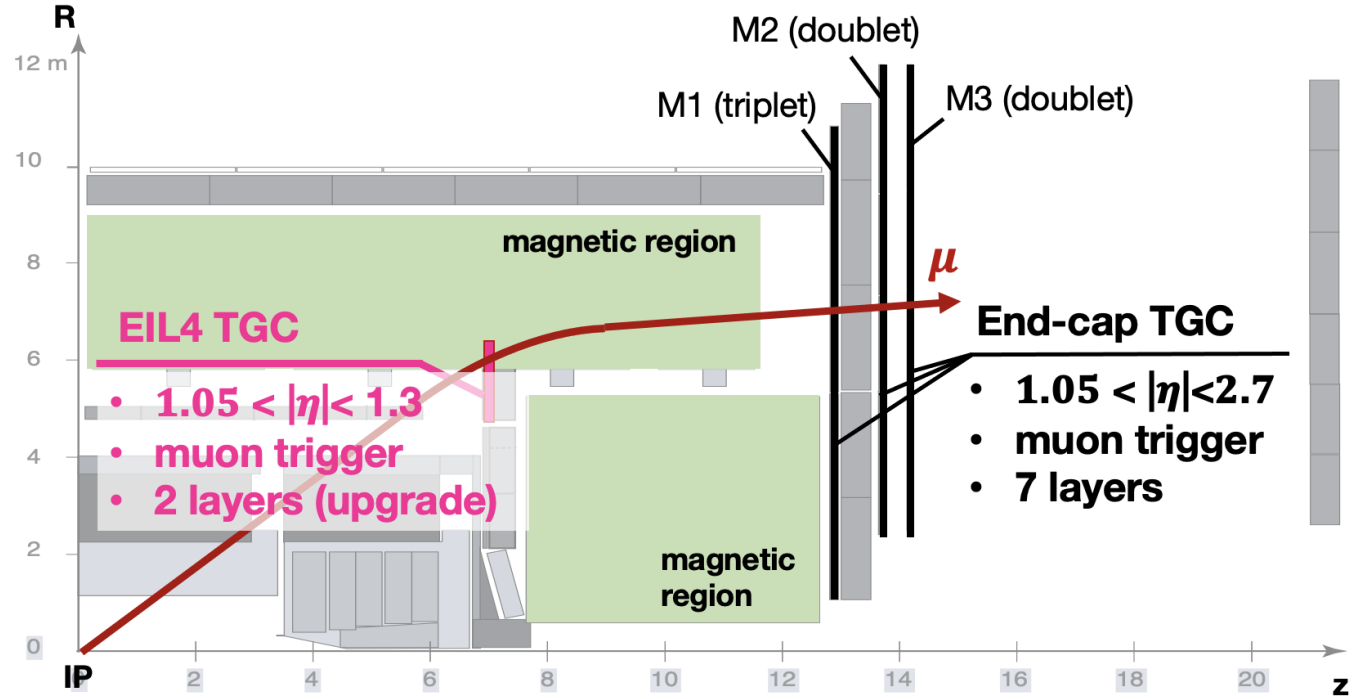
3rd DRD1 Collaboration Meeting

# ATLAS detector

## Thin Gap Chamber (TGC)

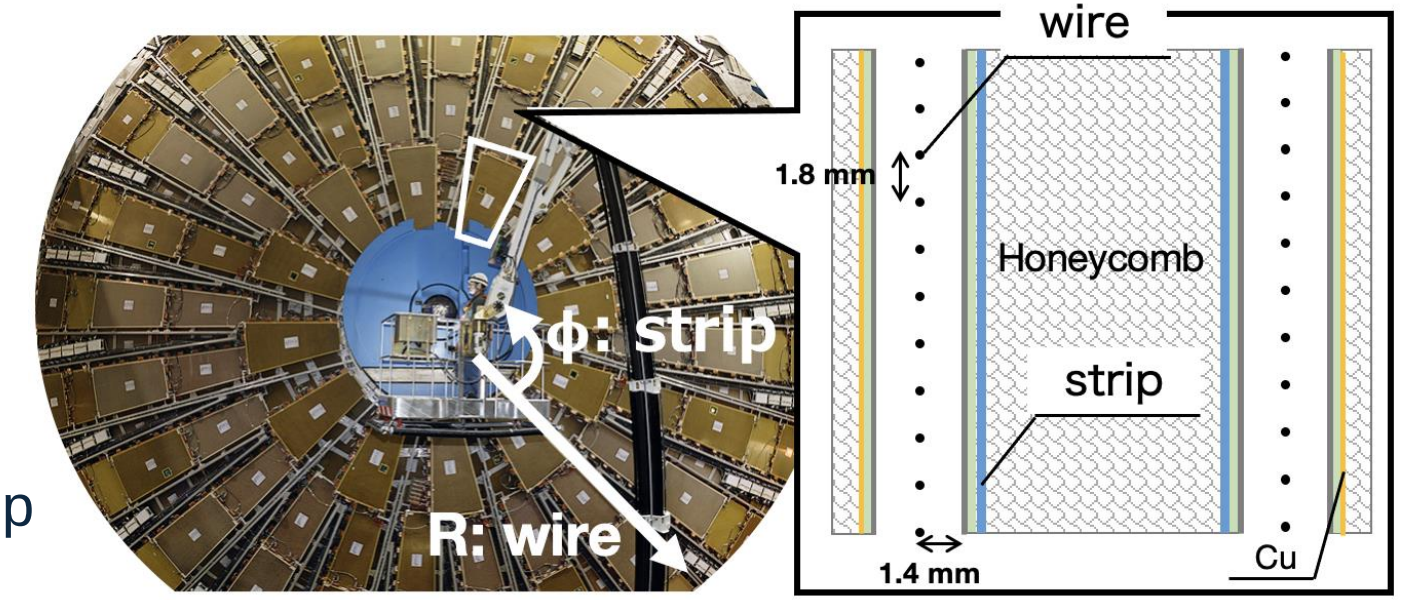


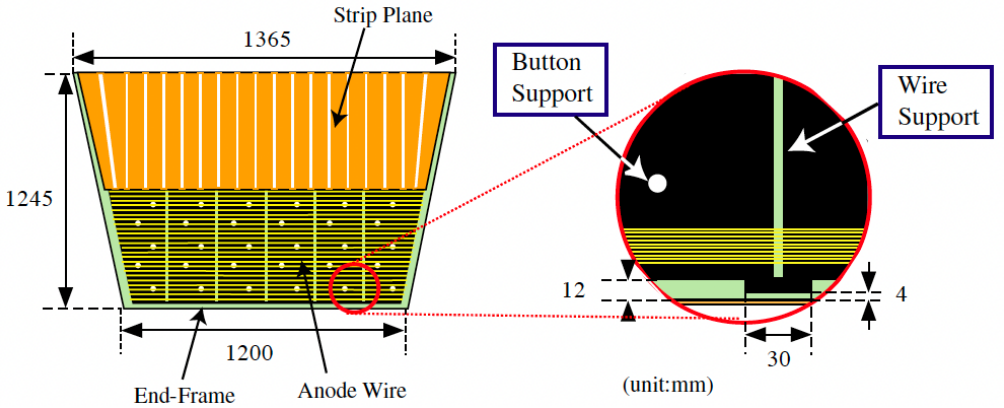




Quarter-cut view of the ATLAS detector

# Thin Gap Chamber (TGC)

- Multi-wire proportional chamber
  - CO2 : n-pentane (55:45)
  - supply 2.8 kV for anode wire
- Feature
  - 2D position (R, $\phi$) measurement using anode wire and cathode strip
  - thin gas gap (~2.8 mm)
  - fast time response ($\lesssim$ 25 ns)
- Role
  - Endcap muon trigger
  - Associating muons with proton-proton collisions
- Work stable from Run 1 to Run 3



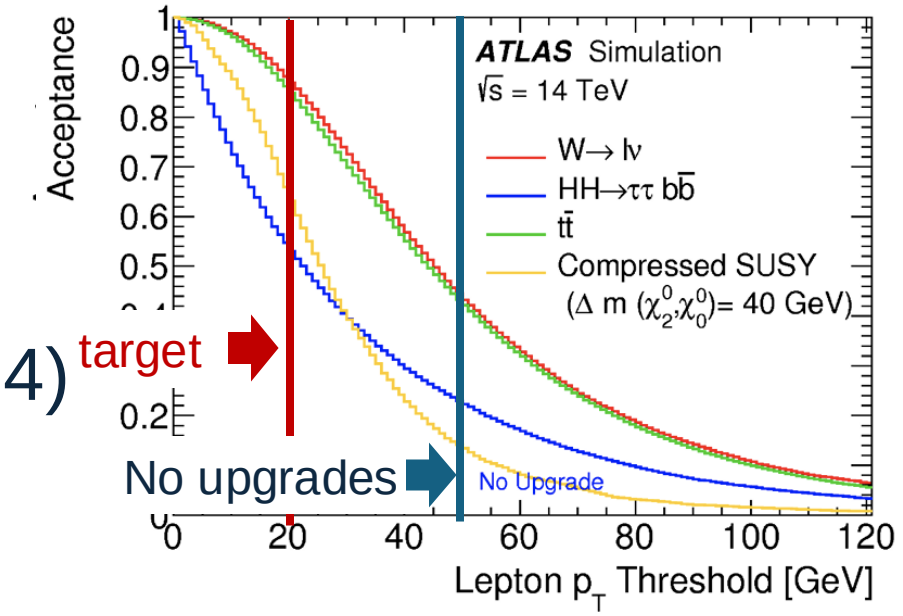



# TGC Phase II upgrade overview

- The Phase II upgrade for the HL-LHC, starting in 2030, is planned
  - instantaneous luminosity: $7.5\times10^{34}\,cm^{-2}s^{-1}$
  - integrated luminosity: 4000 $fb^{-1}$
  - To achieve high acceptance in high-luminosity environments, upgrades to the trigger, readout circuits, and detectors are required

This talk

1. Upgrade all TGC readout electronics
2. Upgrade inner-station TGC detector (EIL4)



# TGC readout electronics at HL-LHC

The Phase 2 trigger readout uses 4 readout circuits.

## Amplifer Shaper Discriminator Board

- amplifies and discriminates TGC hit signals
- converting to LVDS digital signals

## Patch-Panel ASIC and Sender Board

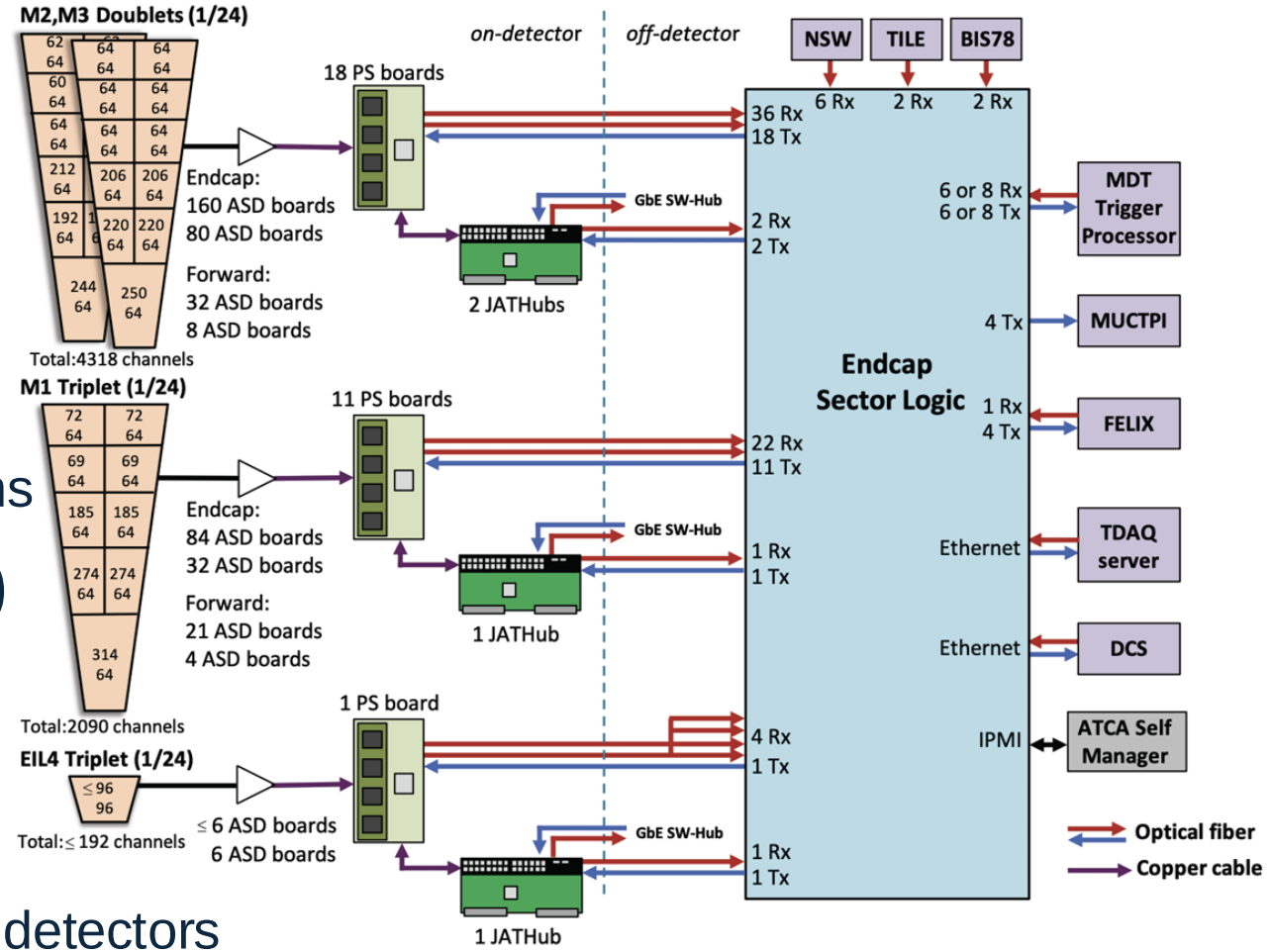
- adjusts timing and sends all hit data every 25 ns

## JTAG Assistance Hub (JATHub board)

- Monitor the FPGA on the PS board and recover from errors

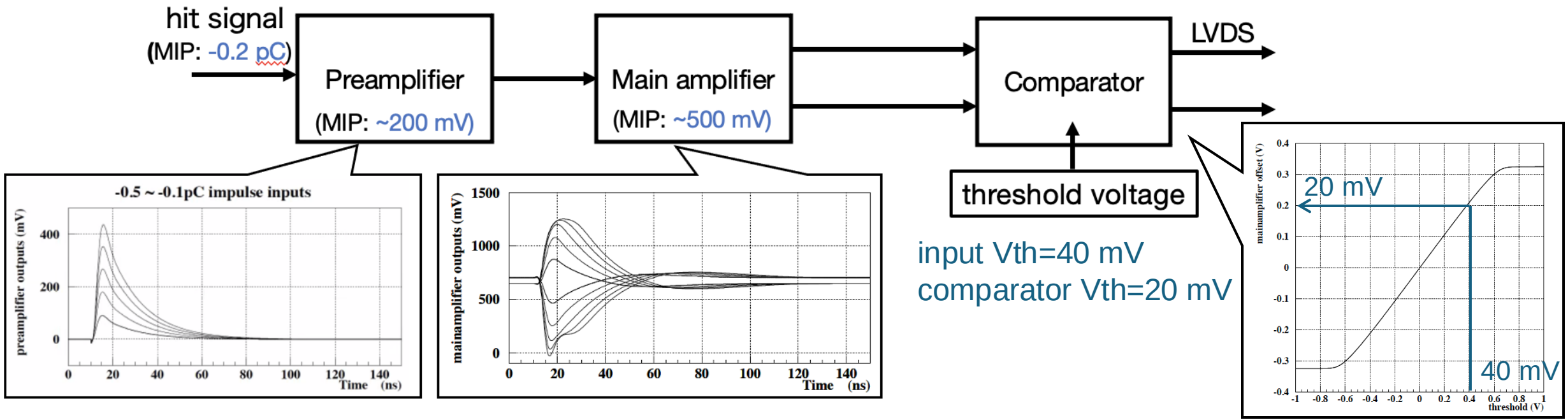
## Sector Logic Board

- Aggregates hit information from multiple muon detectors
- reconstructs tracks, calculates transverse momentum, and reduces muon candidates to six



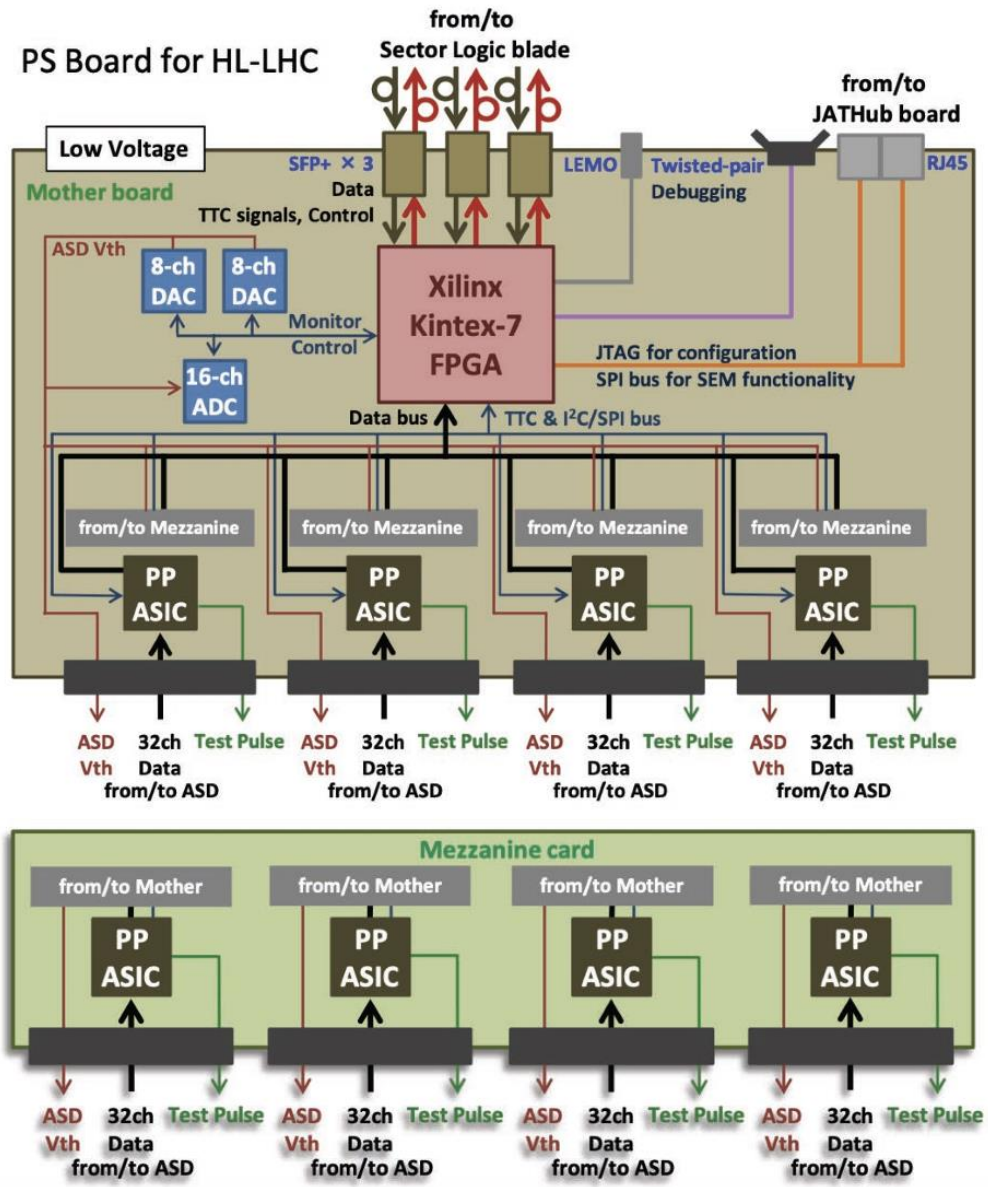
# Amplifer Shaper Discriminator Board (ASD board)

- The hit signal is amplified by a factor of 7 in the main amplifier.
- The threshold voltage is supplied from the DAC and compared with the signal.
- The external threshold input is set to half the value and used as the comparator threshold
- 16 channels per board



# Patch-Panel ASIC and Sender Board (PS board)

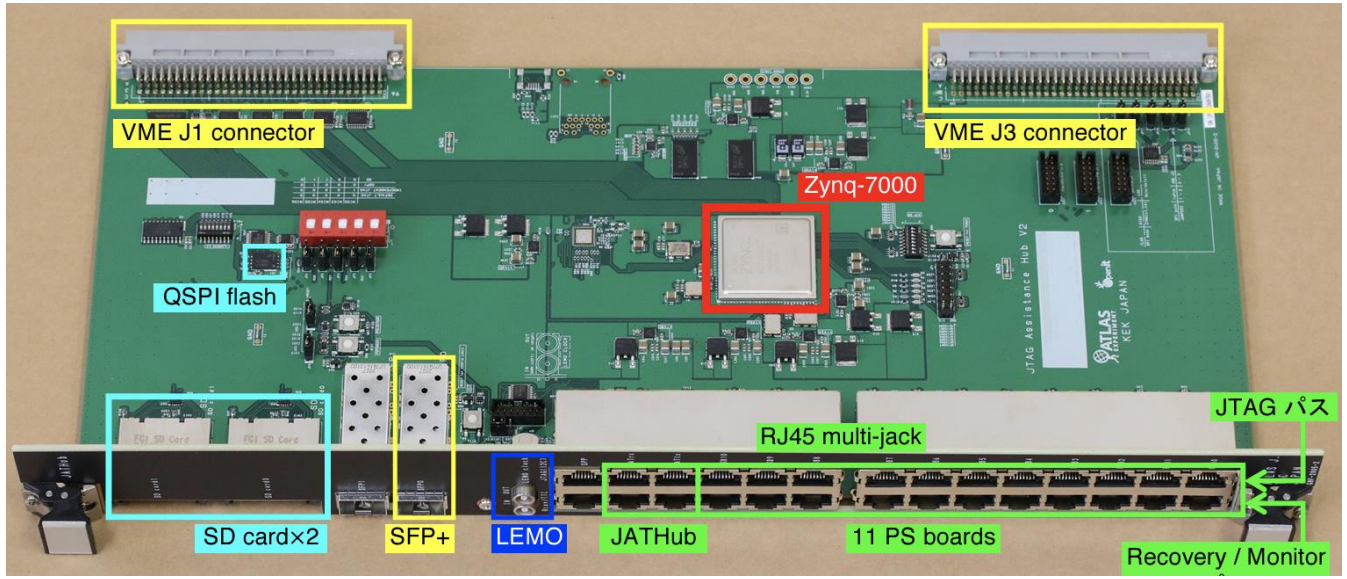
- Equipped with 8 PP ASICs and 1 FPGA
  - 32 channels for each PP ASIC
  - 256 channels for each PS board
- PP ASIC
  - apply a fine delay to each signal to compensate for the differences in cable lengths and adjust the timing of the signal (Bunch Crossing Identification)
  - synchronize signals with the LHC clock (40 MHz)
- Sends all TGC hit data to subsequent circuits ever 25 ns via two 8 Gbps GTX transceivers




A mezzanine card mounted on a motherboard

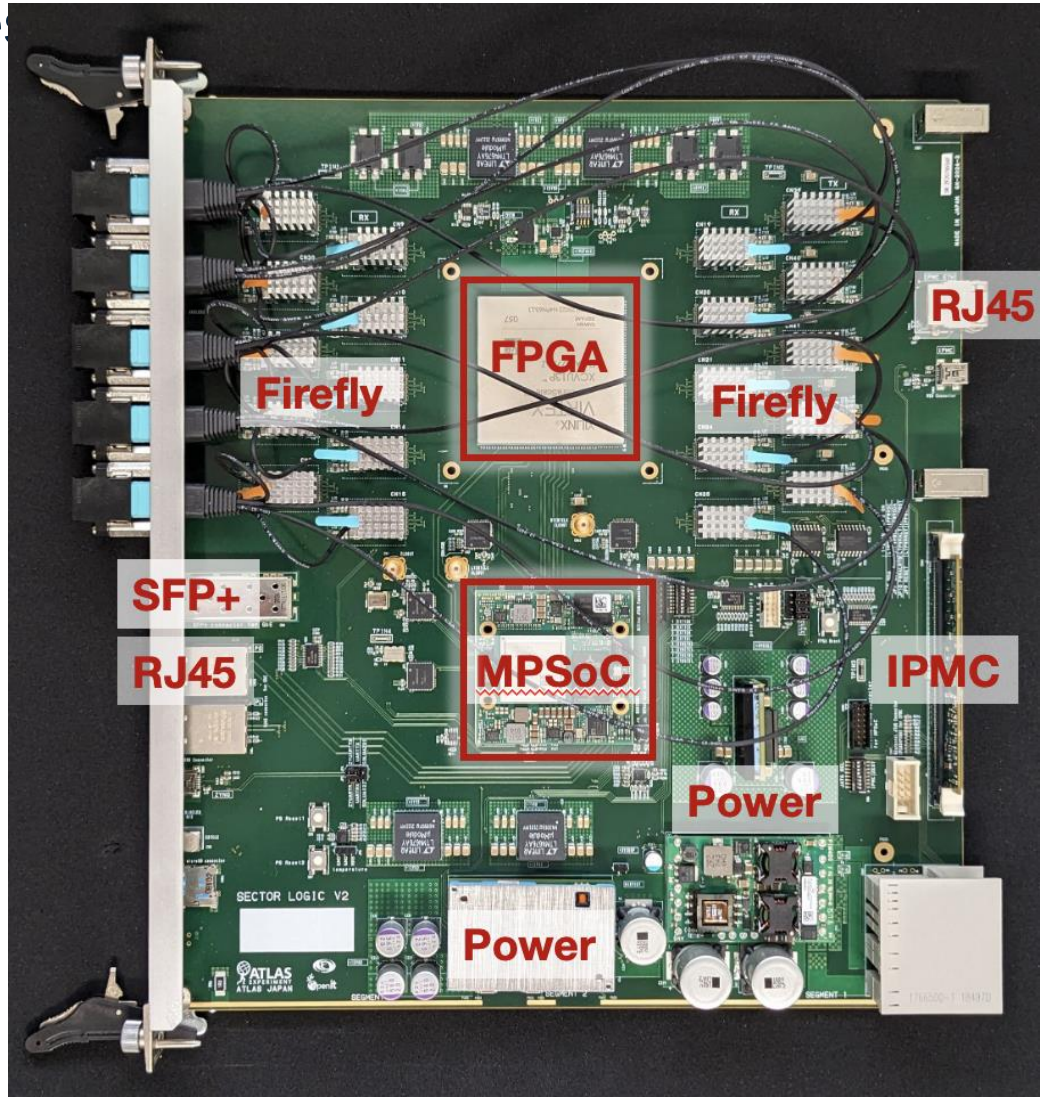
# JTAG Assistance Hub (JATHub board)

- Independently from the data path, the PS board handles the control
  - One JATHub is connected to up to 11 PS boards via Cat 6 cables with RJ45 multi-jacks
- PS board is installed in a location that is difficult to access
  - FPGA firmware configuration, handling SEU errors due to radiation damage, and monitoring the clock phase on the PS board are performed through JATHub
- Equipped with the Xilinx Zynq-7000 (integrated CPU and FPGA)

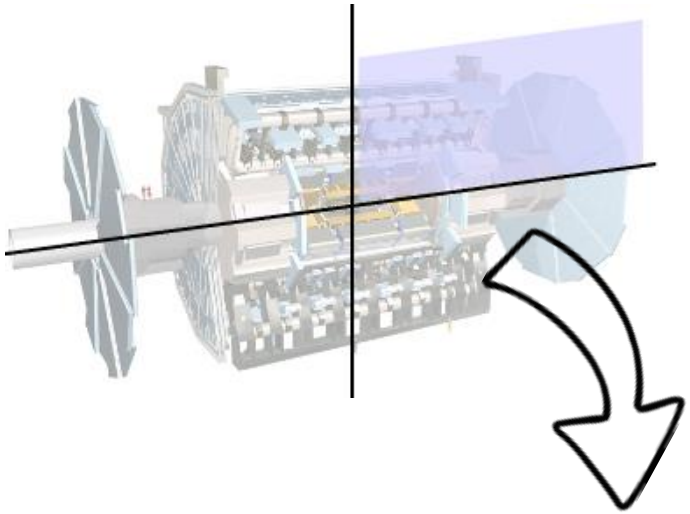


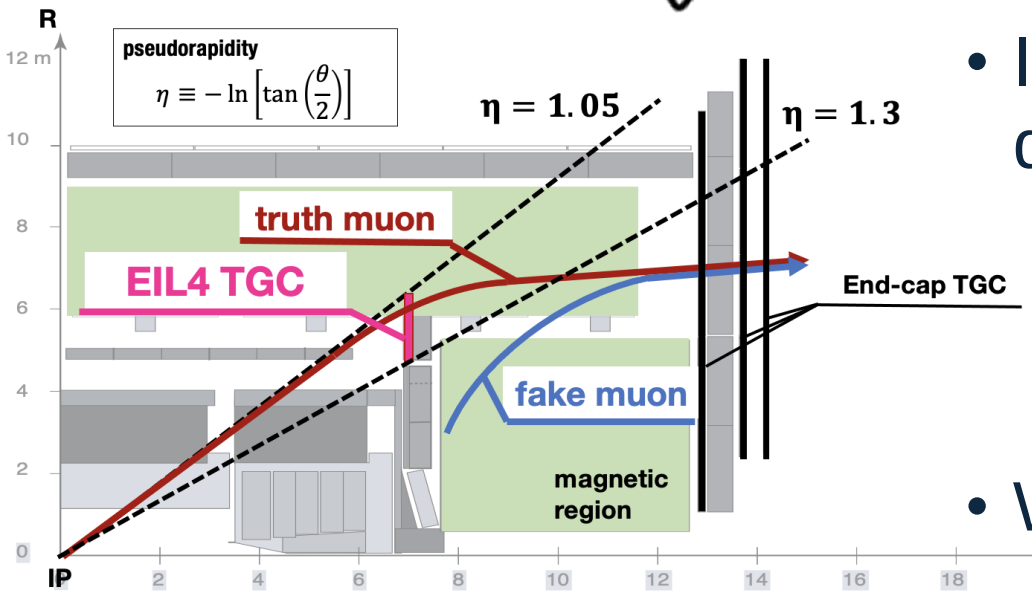
# Sector Logic Board (SL board)

- Includes high-capacity optical communication modules, an FPGA, and mezzanine cards
  - Equipped with 10 Firefly modules for both transmission and reception
  - Capable of 120 optical communication links
- FPGA
  - Calculate $p_T$ using TGC hit data and information from other muon detectors
  - Stores and transfers data for which a trigger has been issued to the subsequent stages
- MPSoC
  - Operate the registers inside the SL FPGA to configure parameters related to triggering and readout
- IPMC
  - Monitor SL voltage and temperature and remotely control power through the IPMC from the ATCA crate



# Background suppression by EIL4 TGC






- Truth muons enter the EIL4 from the interaction point and pass through the end-cap TGC
- To suppress fake muon by taking coincidence with End-cap TGCs

- It plans to upgrade and early install the ATLAS detector this week
  - 4 chambers (Normal ×2, Special ×2)
  - Normal: 32 channels
  - Special: small chamber, 21 channels
- We evaluated three chambers

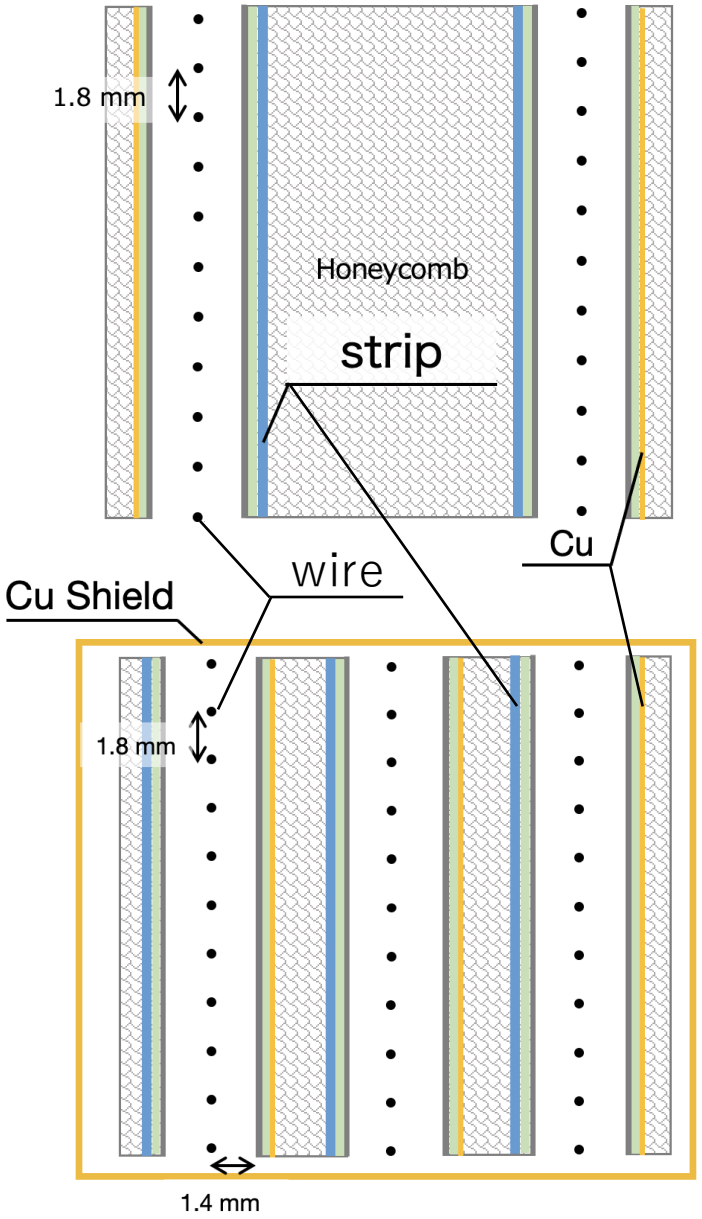
# Changes to the EIL4 TGC

## Until 2025 (end of Run 3)

- Two detection layers (doublet)
- Requires hits in at least one of the two layers,
  but only in areas where both layers are operational.
- Read out the OR of 8 channels

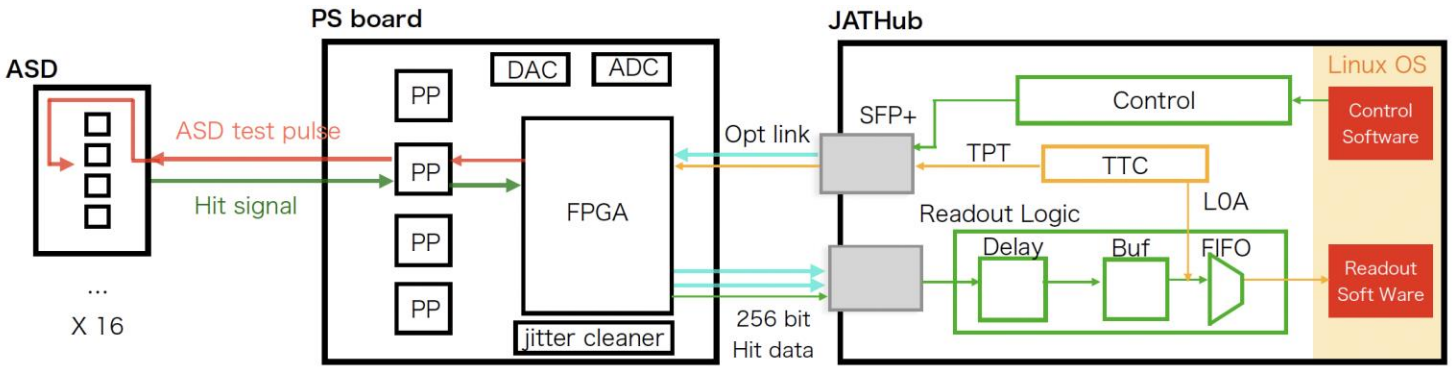
## From 2029 (start of HL-LHC)

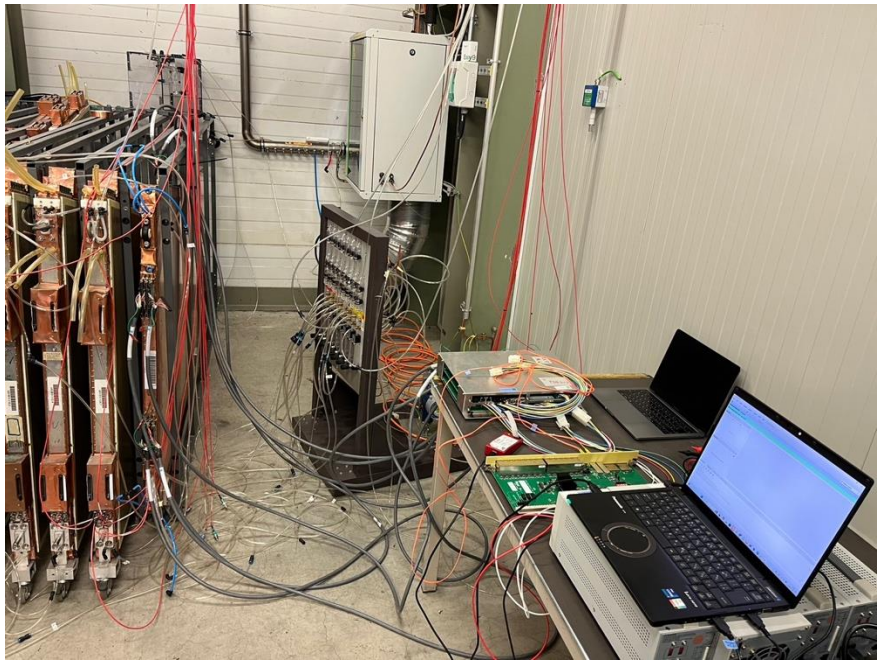
- Three detection layers (triplet)
- Triple-layer structure fits within the same envelope
  as the previous doublet
- Hits in at least two of the three layers are required.
- Read out each channel individually
- Robustness allows operation as a doublet even if one layer fails.



# EIL4 DAQ system for evaluation

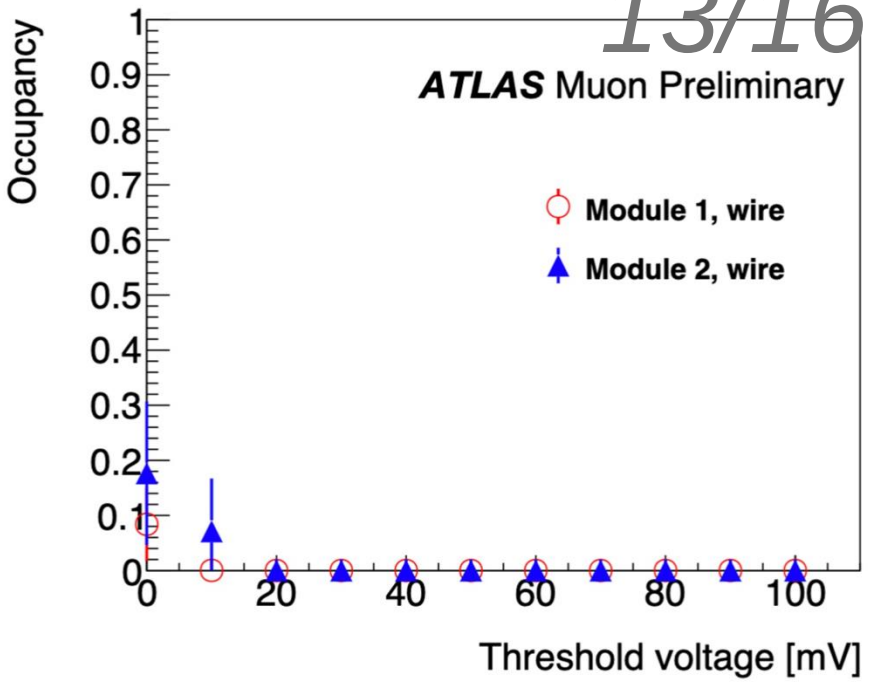
- Using phase II trigger readout electronics for the evaluation
  - ASD board, PS board, JATHub
- Trigger logic using TGC hits added in JATHub for data taking of cosmic muons

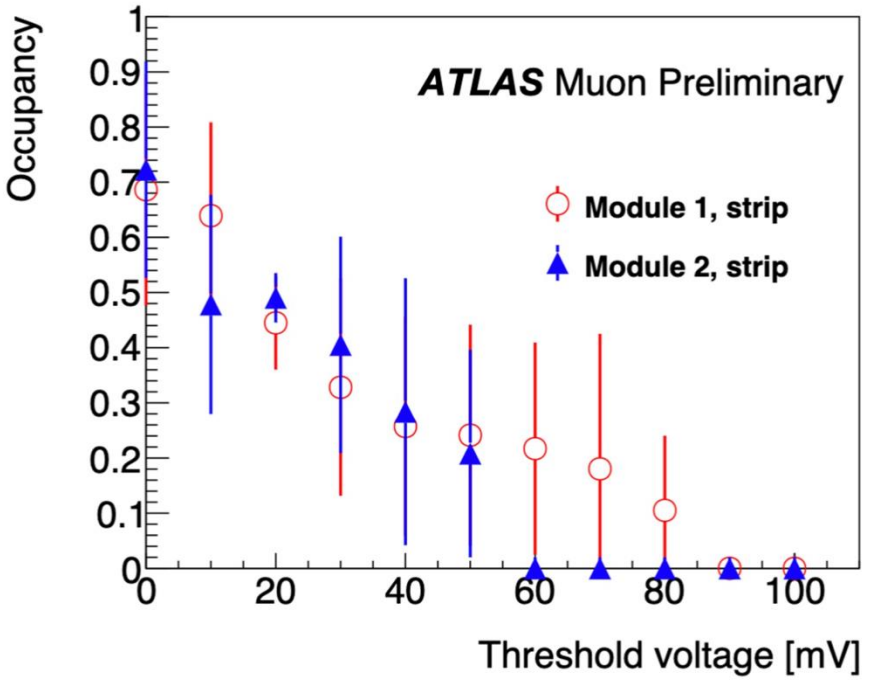


# Noise rate of normal chamber

- The hit data was taken with random trigger (11 kHz)
  - Module 1: 11k events
  - Module 2: ~1M events
- The ASD discriminator threshold (Vth) scanned
- Using CO2 gas




**Nominal Vth at Point 1: 60 mV (wire), 70 mV (strip)**
**with exceptions (up to ~300 mV) for ~1% chambers**

| Zero occupancy | Module 1 | Module 2 |
|---|---|---|
| wire | Vth ≧ 20 mV | Vth ≧ 20 mV |
| strip | Vth ≧ 90 mV | Vth ≧ 60 mV |

**Noise level fine for the operation**

# Efficiency of normal chamber

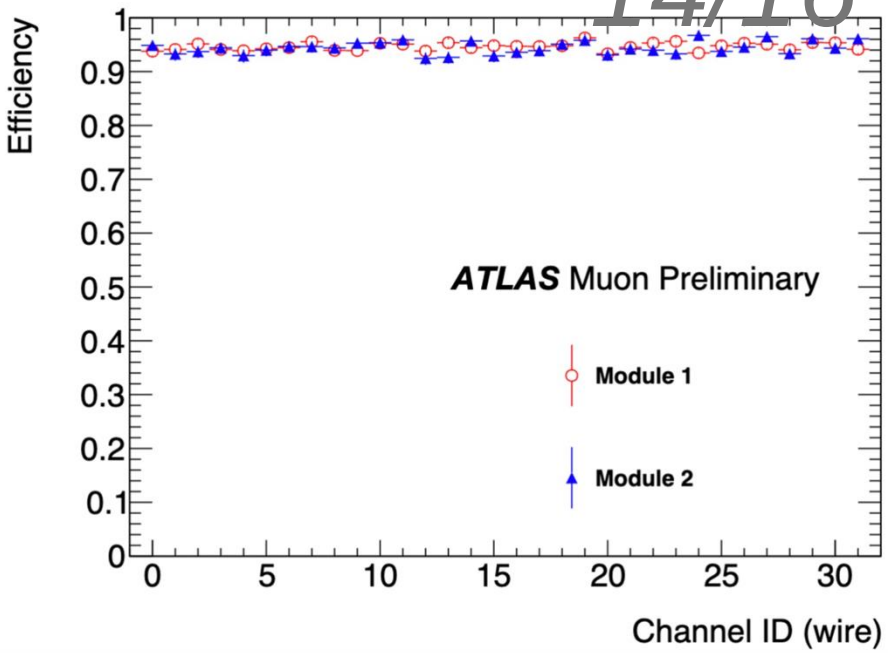
- The data taken when at least two layers have a hit
- Using cosmic muon and Vth = 100 mV
  (low noise but still fine for minimum ionizing particles)
- Nominal gas CO2+n-pentane and nominal HV (2.8 kV) supplied

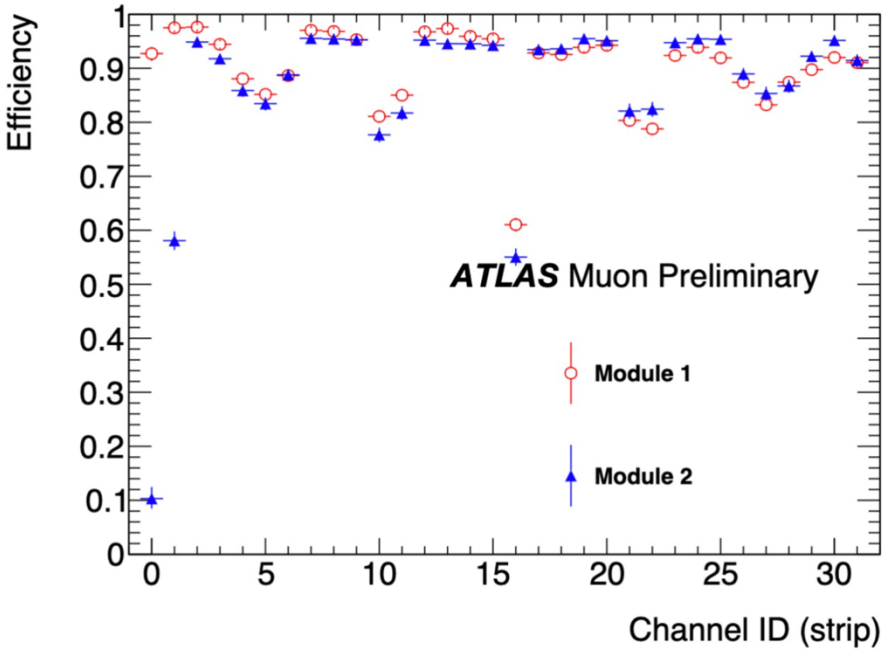
- The efficiency for the layer 1 was evaluated by:

$$\text{Efficiency} = \frac{(\text{Number of events with hits on layers 0, 1, and 2})}{(\text{Number of events with hits on layers 0 and 2})}$$

**Module 1: (94.0±0.1)% (wire), (92.2±0.1)% (strip)**

**Module 2: (93.8±0.1)% (wire), (93.3±0.1)% (strip)**



# Summary

- In the ATLAS experiment, the TGC is responsible for the muon trigger
- With the Phase II upgrade, both TGC and the trigger DAQ circuits will be updated.
  - Many readout circuits will use SoC, allowing high data collection with good acceptance even in high-luminosity environments
- The EIL4 TGC will have 3 detection layers instead of 2, making it more robust
  - Performance evaluations were conducted using several circuits for Phase II TDAQ
  - Both noise and efficiency were confirmed to be within acceptable limits for operation