SiPM readout electronics

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ASICs summary

- Two main architectures used for SiPM readout;
  - Charge amplifier input.
  - Common base input and current mirroring.
- After first stage most solutions use different paths for timming (high bandwidth) and charge (limited bandwidth) information.
- For speed and power consumption seems to be better the common base input stage.
- Differential or single ended input are reasonable, but in the first case some external components are needed.
- Most designs use an input stage that can modify SiPM operation voltage by around 1V, to equalize gain and compensate temperature.
- Low input impedance is desirable to increase SiPM current signal at the input.

ASICs summary

Design	Measurement	Aplication	Input	Techno	Year
FLC_SiPM	Charge	ILC	current	CMOS 0,8	2004
MAROC2	Charge, trig	ATLAS	current	SiGe 0,35	2006
SPIROC	Charge, trig, time	ILC	current	SiGe 0,35	2007
NINO	Trigger, pulse width	ALICE	differential	CMOS 0,25	2004
PETA	Charge, trig, time	PET	current	CMOS 0,18	2008
BASIC	Height, trig	PET	current	CMOS 0,35	2009
VATA64	Height, trig, time	RICH	current		2009
RAPSODI	Height, trig	SNOOPER	current	CMOS 0,35	2008

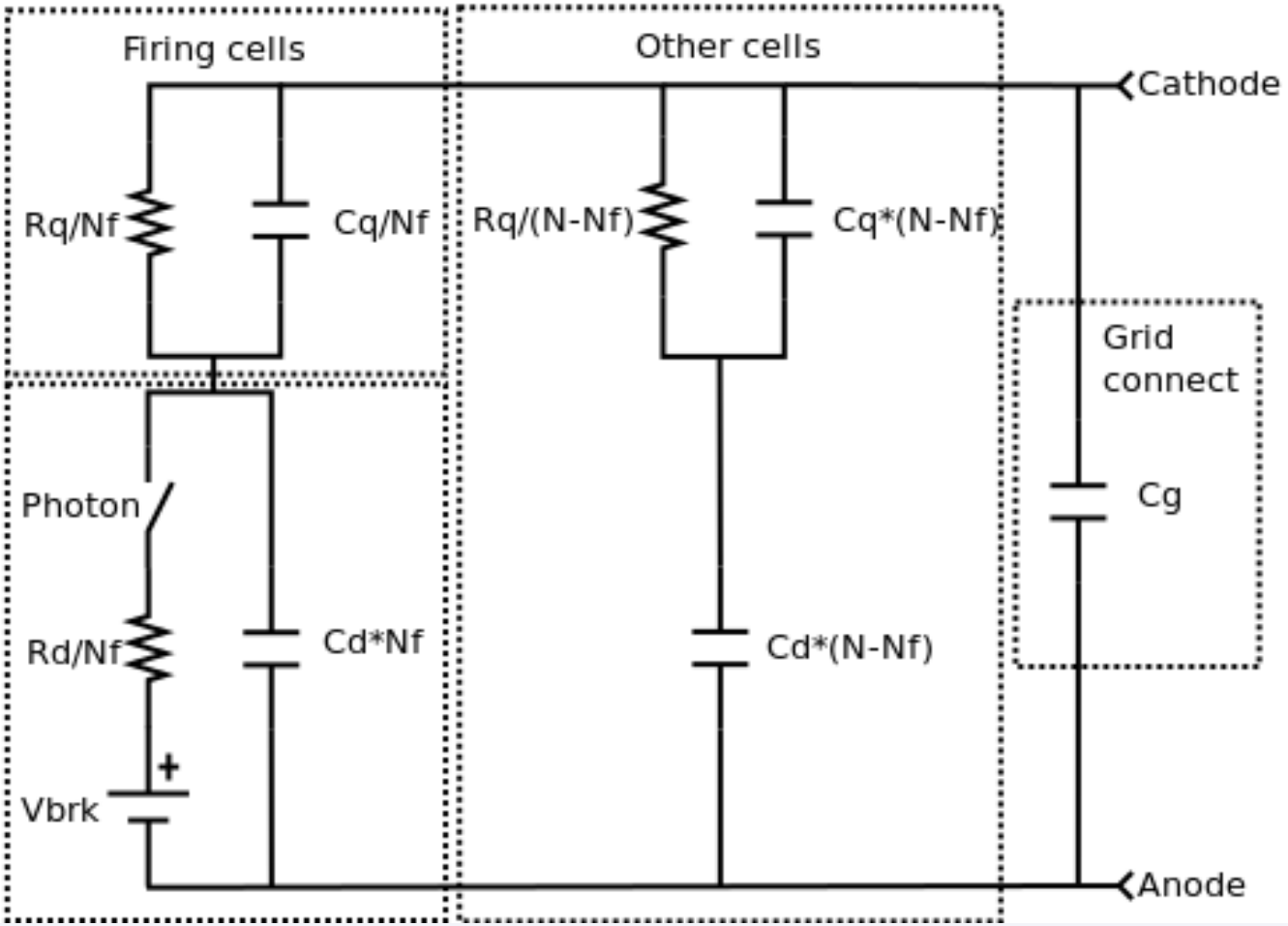
ASICs summary

Design	Chans	Power[1]	Area[2]	Range	Rin	Digital out
FLC_SiPM	18	11	0.55			n
MAROC2	64	2	0.25	80pC	50Ω	y
SPIROC	36	2.5	0.89			y
NINO	8	30	1	2000pe	20Ω	n
PETA	40		0.625	8bit		y
BASIC	32	6.6	0.22	70pC	17Ω	y
VATA64	64	15	1	12pC		n
RAPSODI	2	100	4.5	100pC	20Ω	y

[1] Total power divided by number of channels without power down during idle times (mW).

[2] Total area divided by number of cahnnels (mm^2).

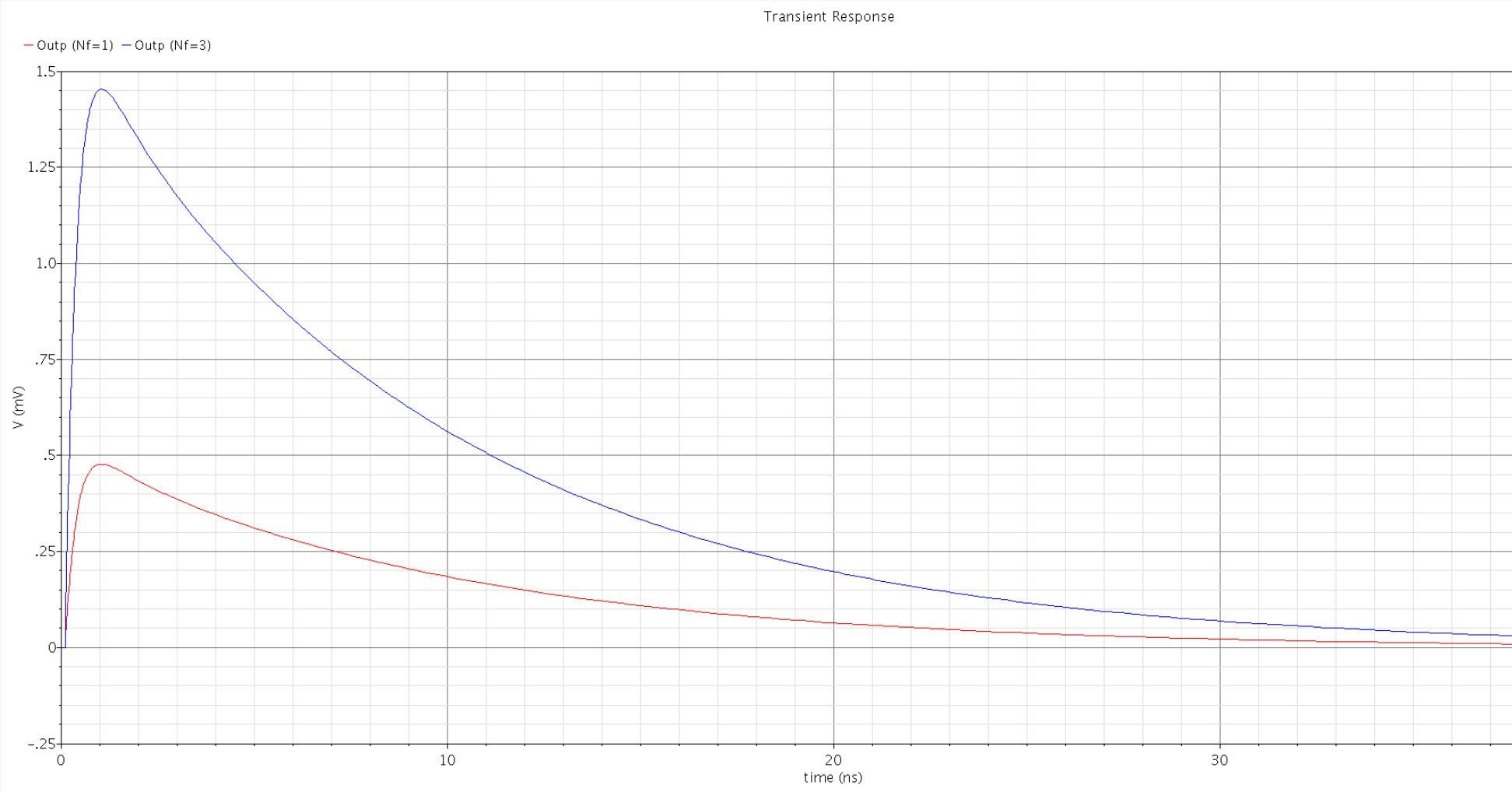
SiPM Model



Rq Quenching resistor value
Cq Parasitic capacitance of Rq
N Number of cells
Nf Number of firing cells
Cd Diode capacitance
Rd Diode resistance
Vbrk Breakdown voltage
Cg Grid connect capacitance

SiPM Model

Parameters fixed to have a similar shape as in measurements;
Peak of 400 $\frac{\mu V}{cell}$ and 20ns recharge time (with 50Ω load).



SiPM Model

Model used as input signals of the designed circuits: