Some ideas about a FE for a SciFi tracker based on SiPM

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Outlook

I. Introduction

II. Measurements with SiPM + CTA preamplifier

III. Simulations with a FE designed for PET

IV. Simulations with ICECAL FE stage (LHCb Calo upgrade)

V. Discussion

I. Introduction

- Two basic approaches for the input stage:
  - Charge sensitive amplifier
  - (Super) common base/gate stages
- Our developments are focused on the later: speed and power ! :
  - SiGe AMS 0.35 um BiCMOS technology
  - But no serious problem to adapt to CMOS for this application
- We will present an overview of our developments related to SiPM readout:
  - Preamplifier for CTA project (tested)
  - FE stage for PET application (simulation)
  - Version (simulation) of the ICECAL chip (tested)

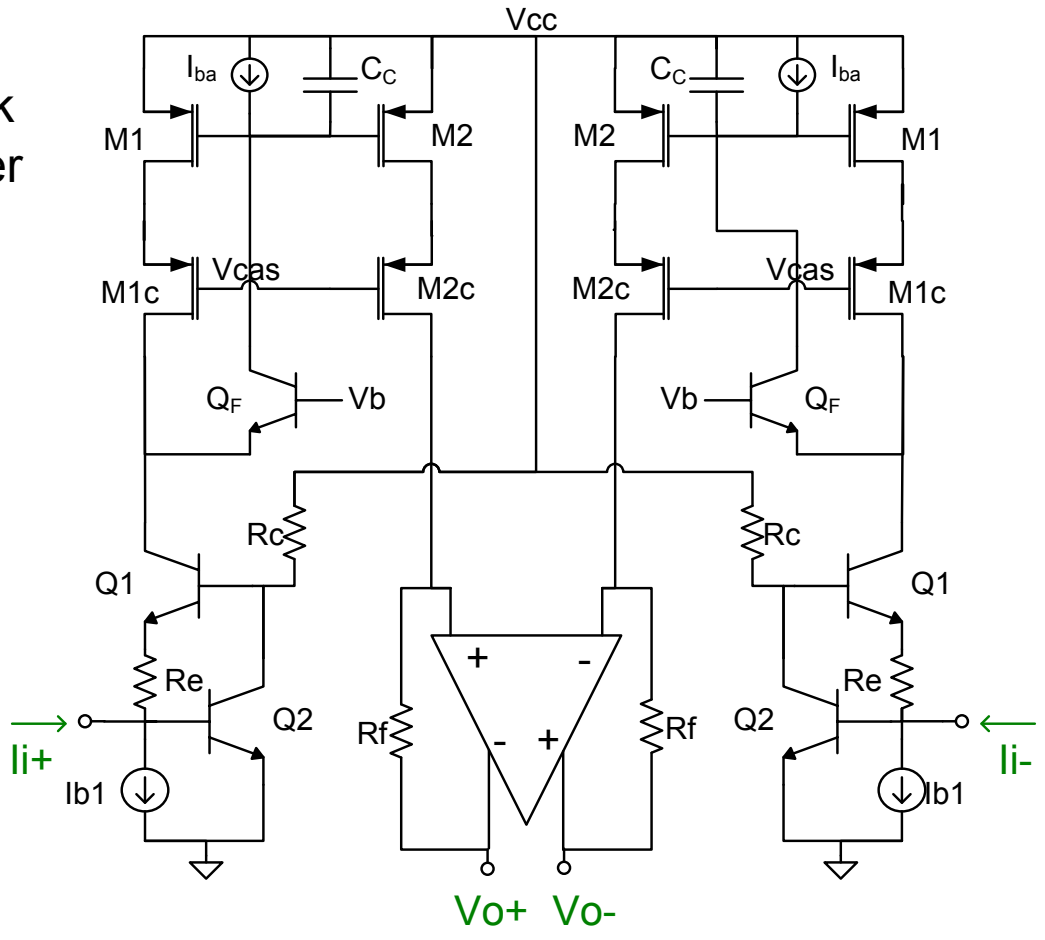
- Signal processing ?
  - Peak detector
  - Integration
  - ToT

- Measurements and simulations using SiPM model will be shown

II. Measurements with SiPM + CTA preamplifier

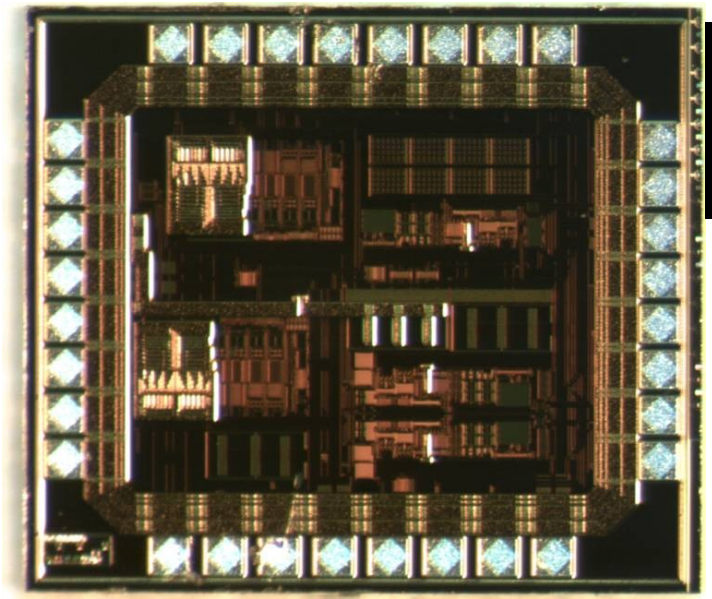
- Basic circuit:
  - Super common base input
  - Cascode current mirror with CB feedback
  - Fully differential transimpedance amplifier
- Performances
  - BW > 500 MHz
  - Low Zi < 10 Ohm up to > 500 MHz
  - Low noise (in=10 pA/sqrt(Hz))
  - Differential: optimal CMRR and PSRR
- But the current mirror can not stand a 1000 phe pulse
  - Saturation at 500 to1000 phe
- Not enough for 16 bit…

Simplified schematic

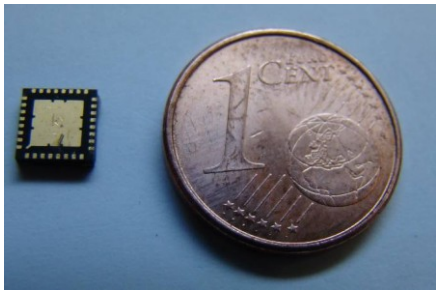


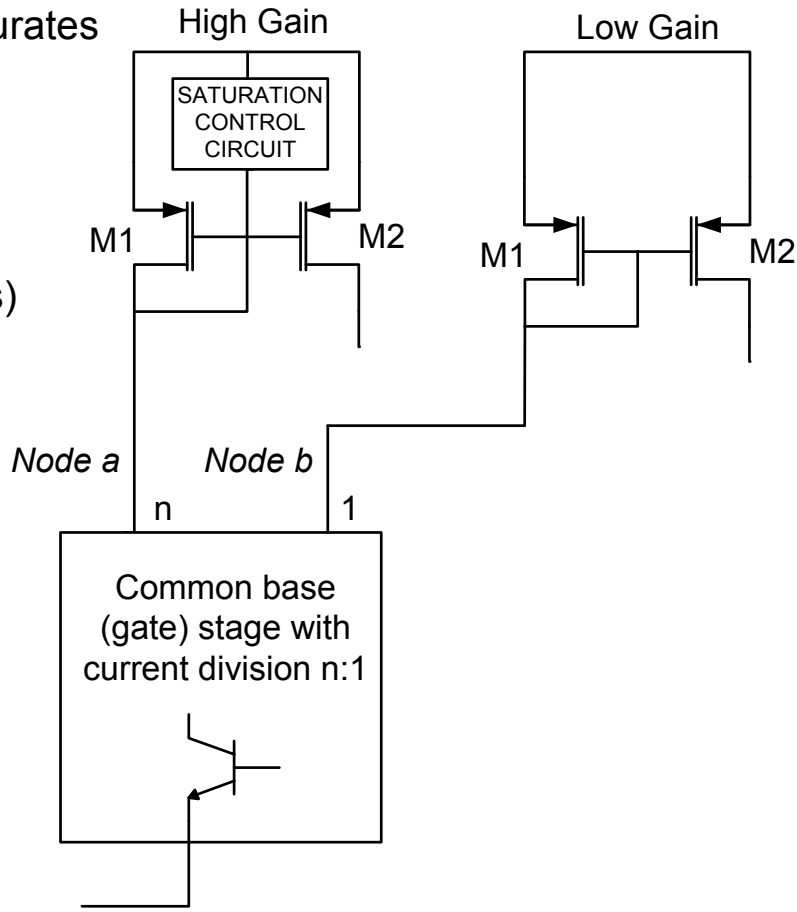
II. Measurements with SiPM + CTA preamplifier

- Previous circuit is modified to split the input current by a novel technique:
  - Current is divided in the common stage
  - Different current mirrors for high and low gain
    - Each can be optimized for BW / linearity
  - Dedicated saturation control circuit is added to the HG mirror
    - Current division remains operational even if HG mirror saturates
    - Saturation threshold of HG mirror can be controlled
  - Range: > 6000 phe
    - True delta pulse with 500 MHz BW
    - No arrival time effect considered
  - Patent pending (cur. splitting has other possible applications)



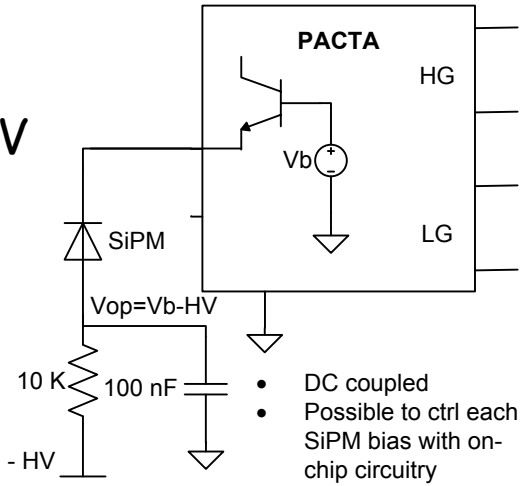
PACTA chip
SiGe BiCMOS 0.35um
AMS 2 mm²
QFN32 package

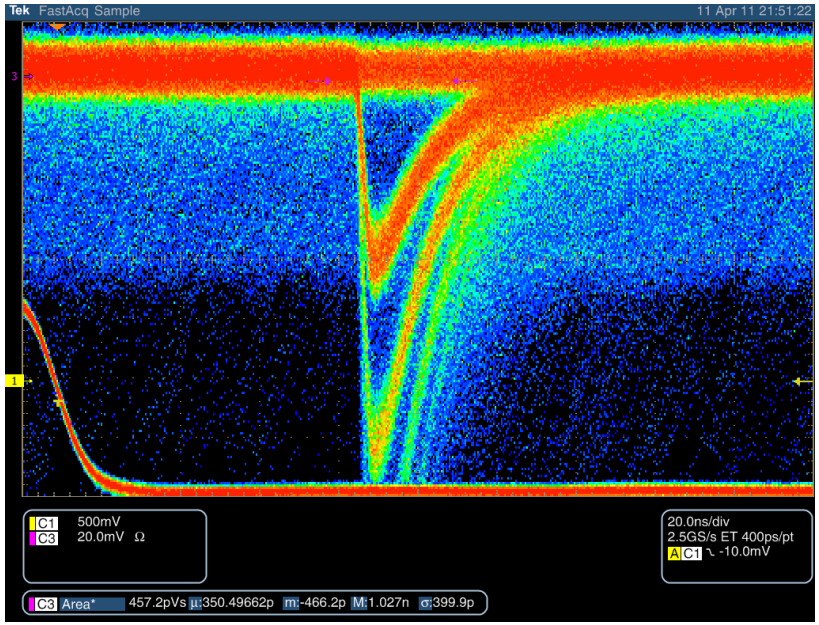


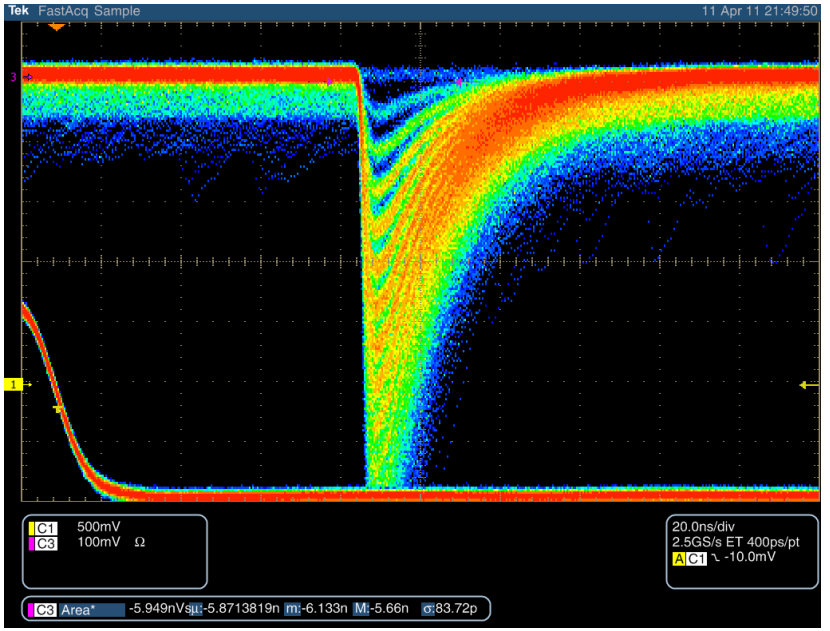


II. Measurements with SiPM + CTA preamplifier

- Preliminary tests with SiPM
  - Low Zin current mode circuit are well suited for SiPM readout
  - We just took an available MPPC (S10931-050P), operated at 1 V overvoltage
  - Recovery time seems to be dominated by internal SiPM time constant
    - Rq(Cq+Cd) = 18 ns, with (Cq+Cd) about 90 fF and Rq about 200K
    - PACTA Zi related time constant is below 1 ns (15 Ohm x 40 pF)

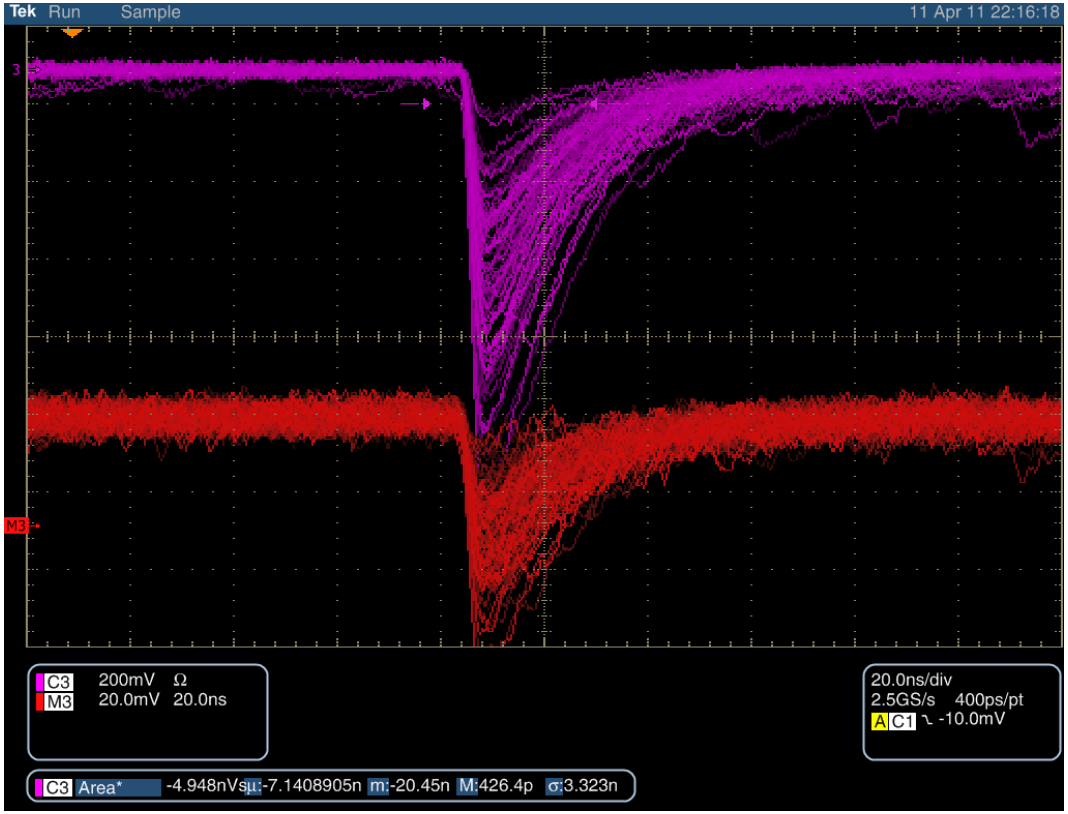


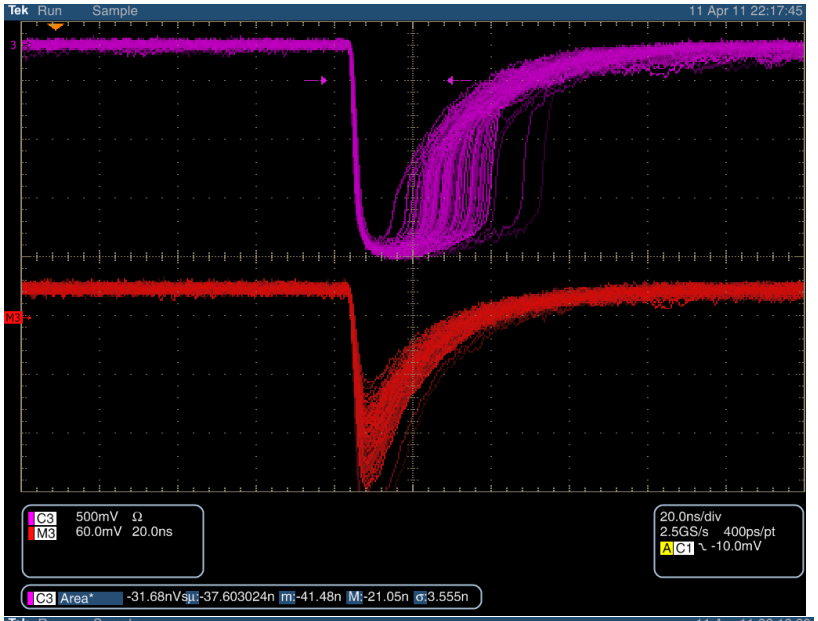


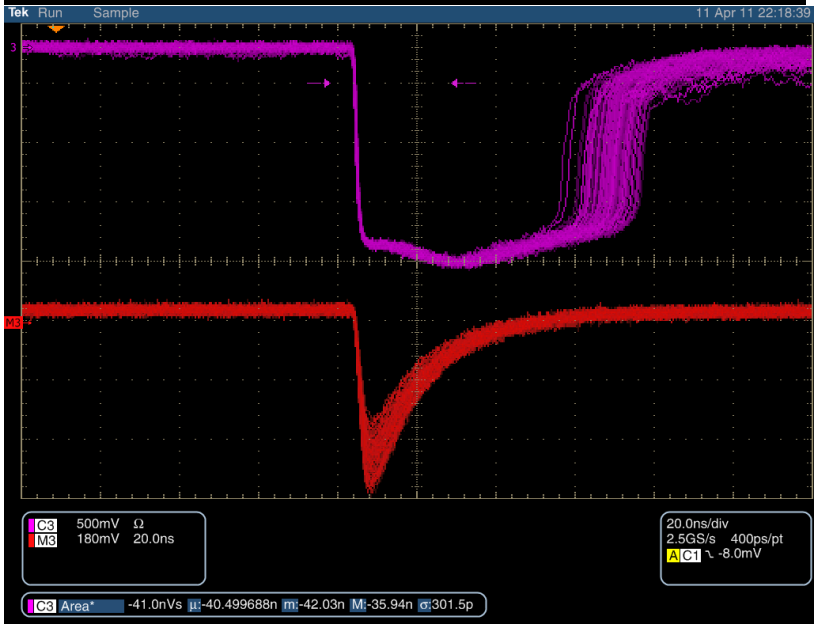


II. Measurements with SiPM + CTA preamplifier

- Preliminary tests with SiPM
  - Bi-gain is also working

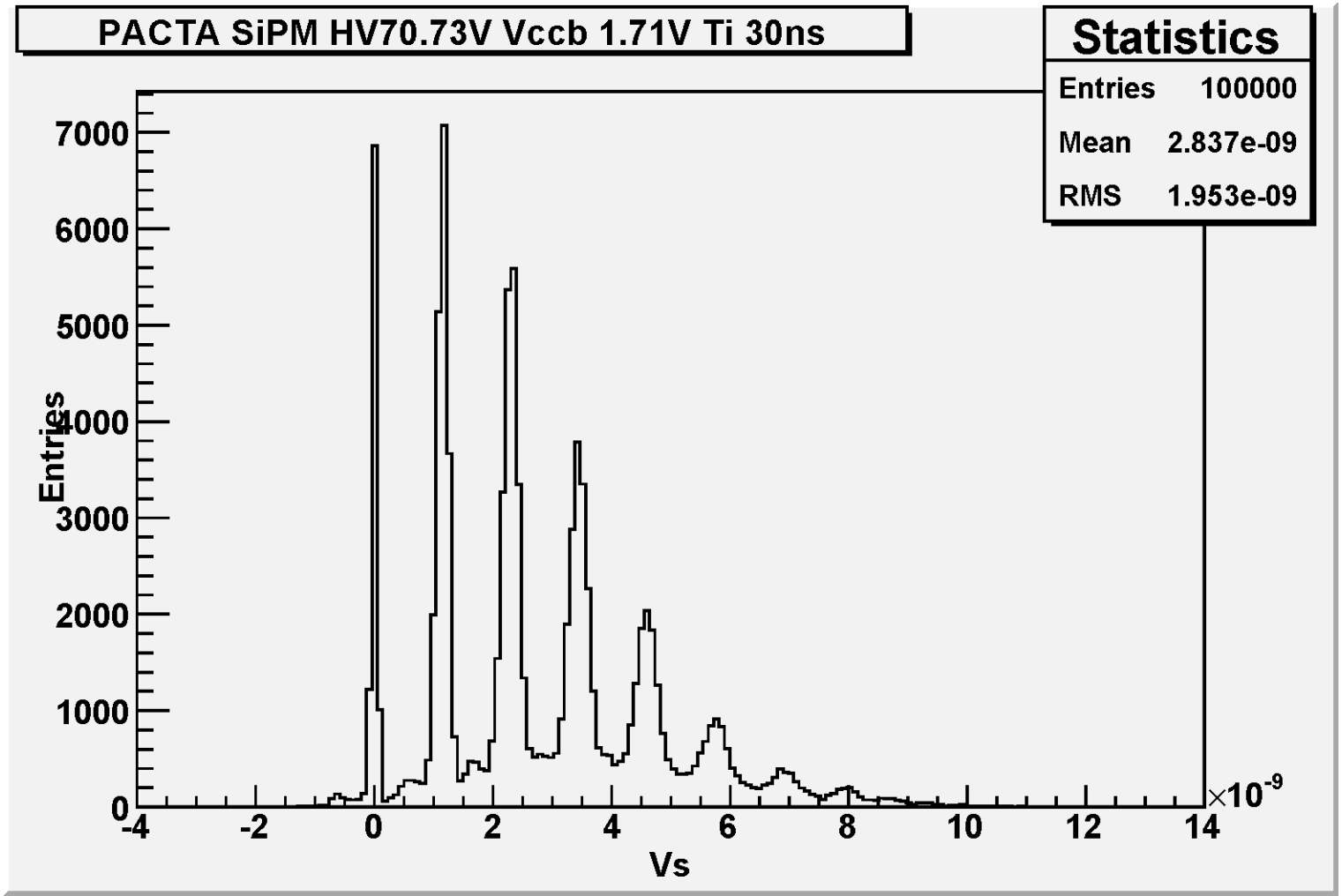






II. Measurements with SiPM + CTA preamplifier

- Preliminary tests with SiPM
  - Charge spectrum

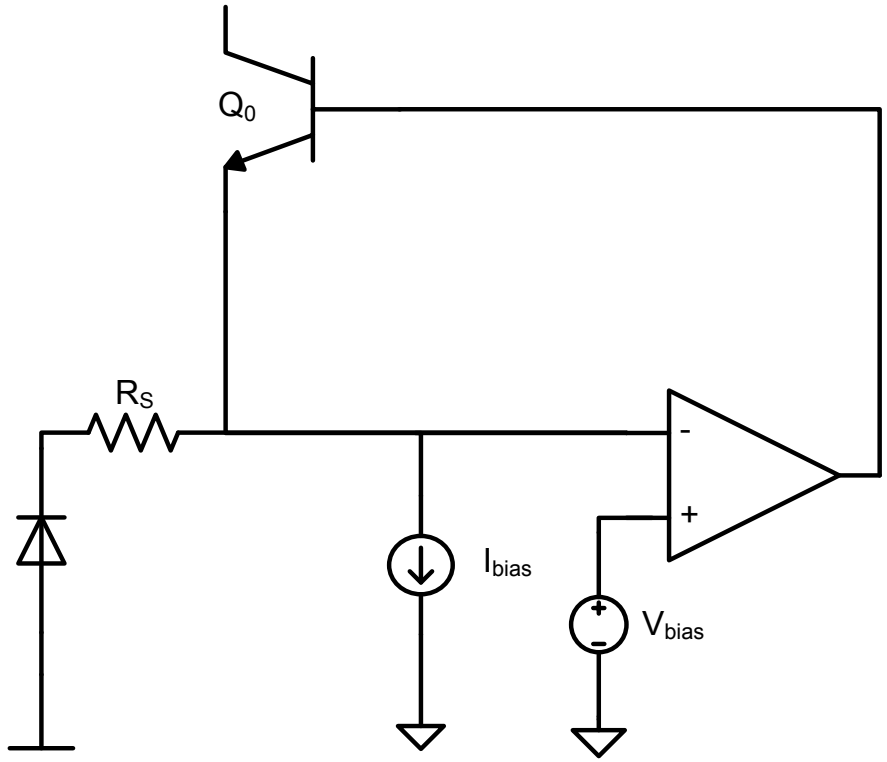


III. Simulations with a FE designed for PET

- PACTA preamplifier could perform well as a VFE but some drawbacks:
  - Current division seems not necessary in this application, could be removed.
  - Limited voltage swing for SiPM adjustment:
    - Major problem
    - Related to common emitter amplifier feedaback to decrease Zi
- Alternative feedback techniques:
  - FE for PET applications: OpAmp with input negative rail swing capability
  - ICECAL chip (LHCb calo upgrade): current mode feedback
    - Also used in BASIC chip for PET applications
- FE for PET applications
  - High gain with fast leading edge current discriminator
  - Low gain with TIA (on the long term, integrator)
  - Input impedance is 20 Ohm
  - Input ref. noise is 2-3 uA rms
  - Max. signal is > 9 mA peak
  - Power conssumption about 5 mW / ch

III. Simulations with a FE designed for PET

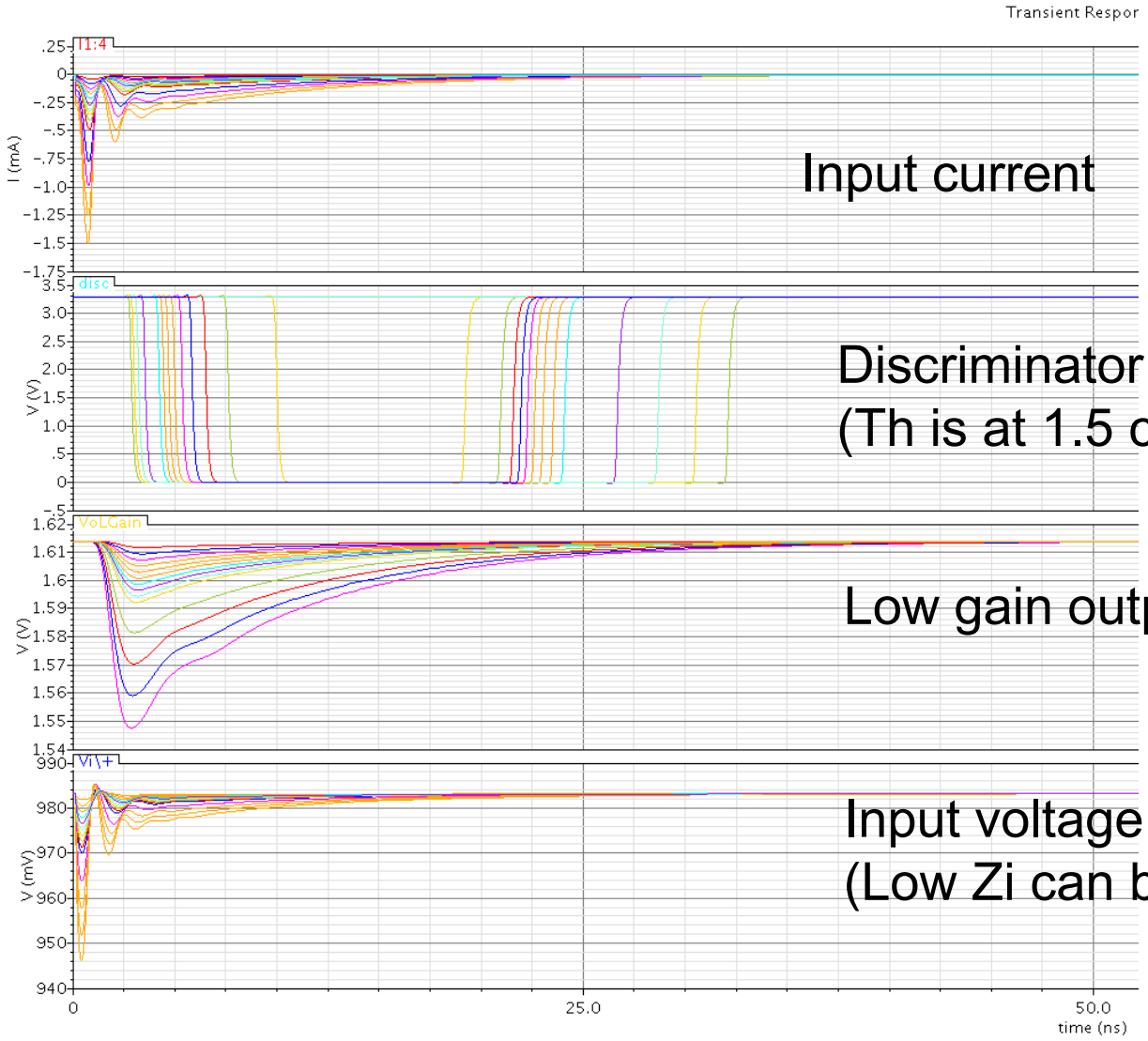
- Simplified schematic of the input stage:
  - OpAmp with input negative rail swing capability to decrease Zi and control SiPM cathode
  - Input impedance is about 20 Ohm
  - SiPM cathode voltage can be tuned: 0 - 1 V



III. Simulations with a FE designed for PET

- Transient response for 1 to 30 fired cells

SiPM model adjusted to fit Guido's measurements



Input current

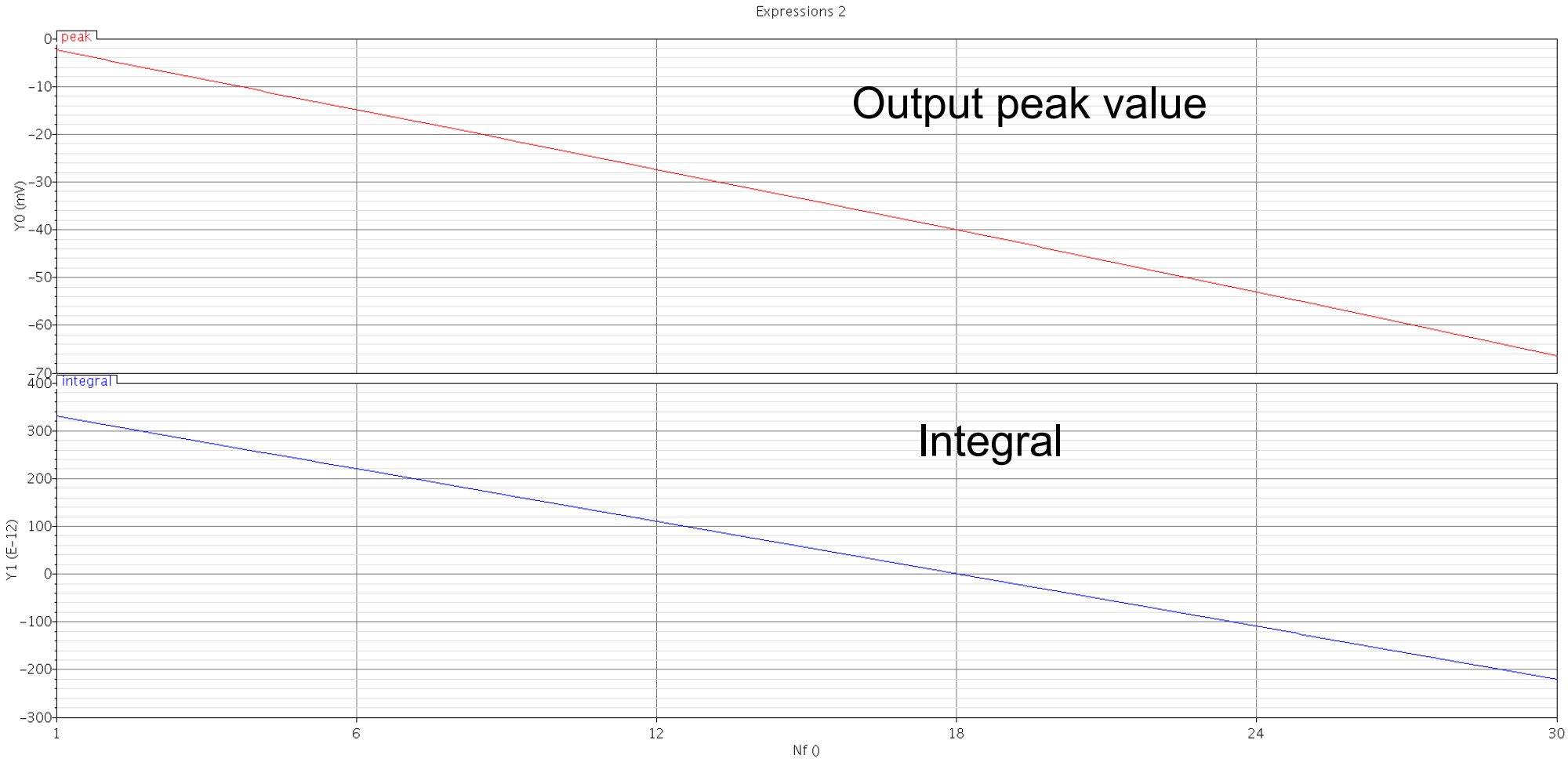
Discriminator output
(Th is at 1.5 cells)

Low gain output

Input voltage
(Low Zi can be noticed)

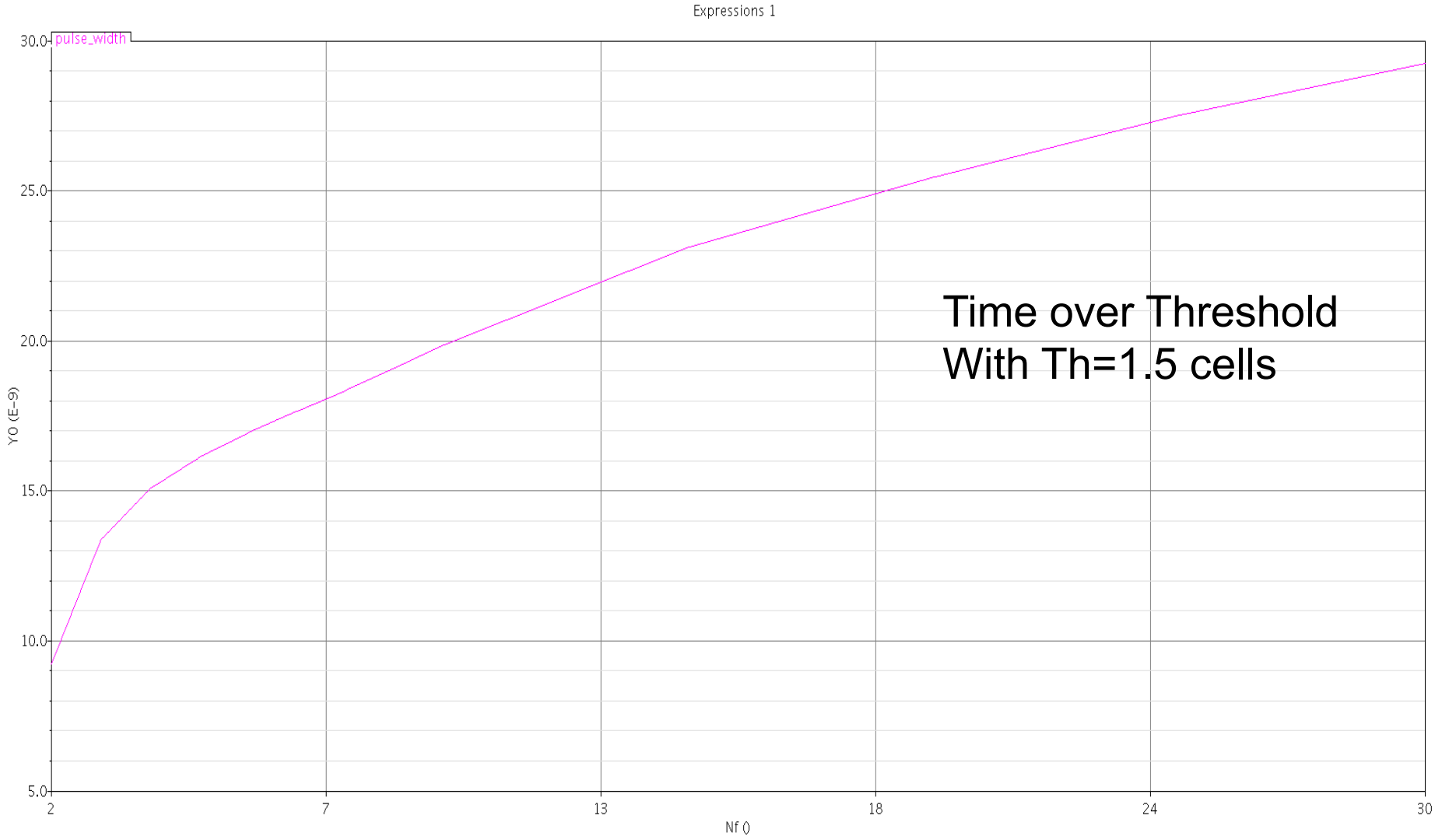
III. Simulations with a FE designed for PET

- Peak or integral measurements are ok



III. Simulations with a FE designed for PET

- Is ToT feasible? What resolution (clock) is needed?

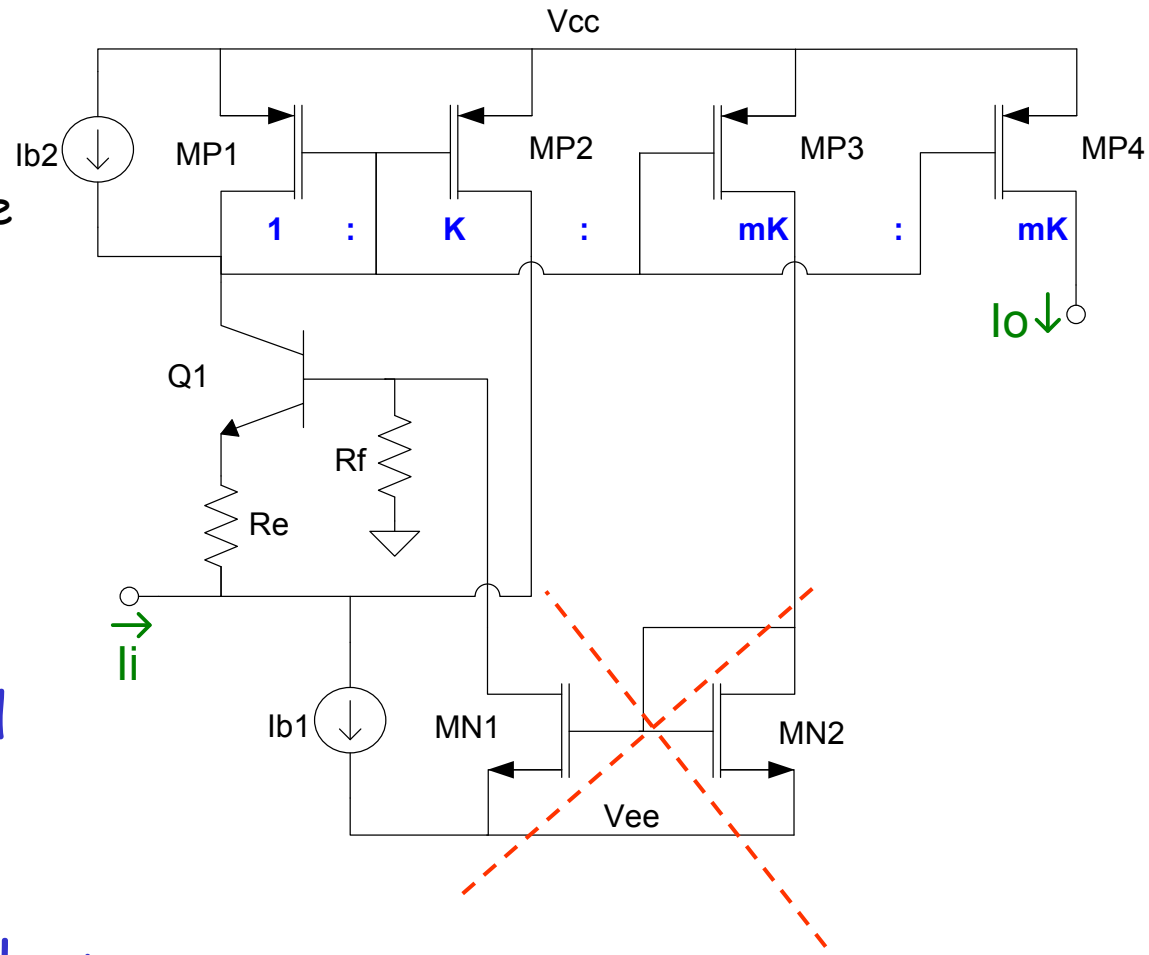


III. Simulations with ICECAL FE stage (LHCb Calo upgrade)

- Current mode feedback:
  - Inner loop: lower input impedance
    - Current feedback (gain): mirror: K
  - Outer loop: control input impedance
    - Current feedback: mirror: m
- Current gain: m
- Input impedance

$$Z_i \approx \frac{1/g_m + R_e}{1+K} + \frac{K}{1+K} m R_f$$

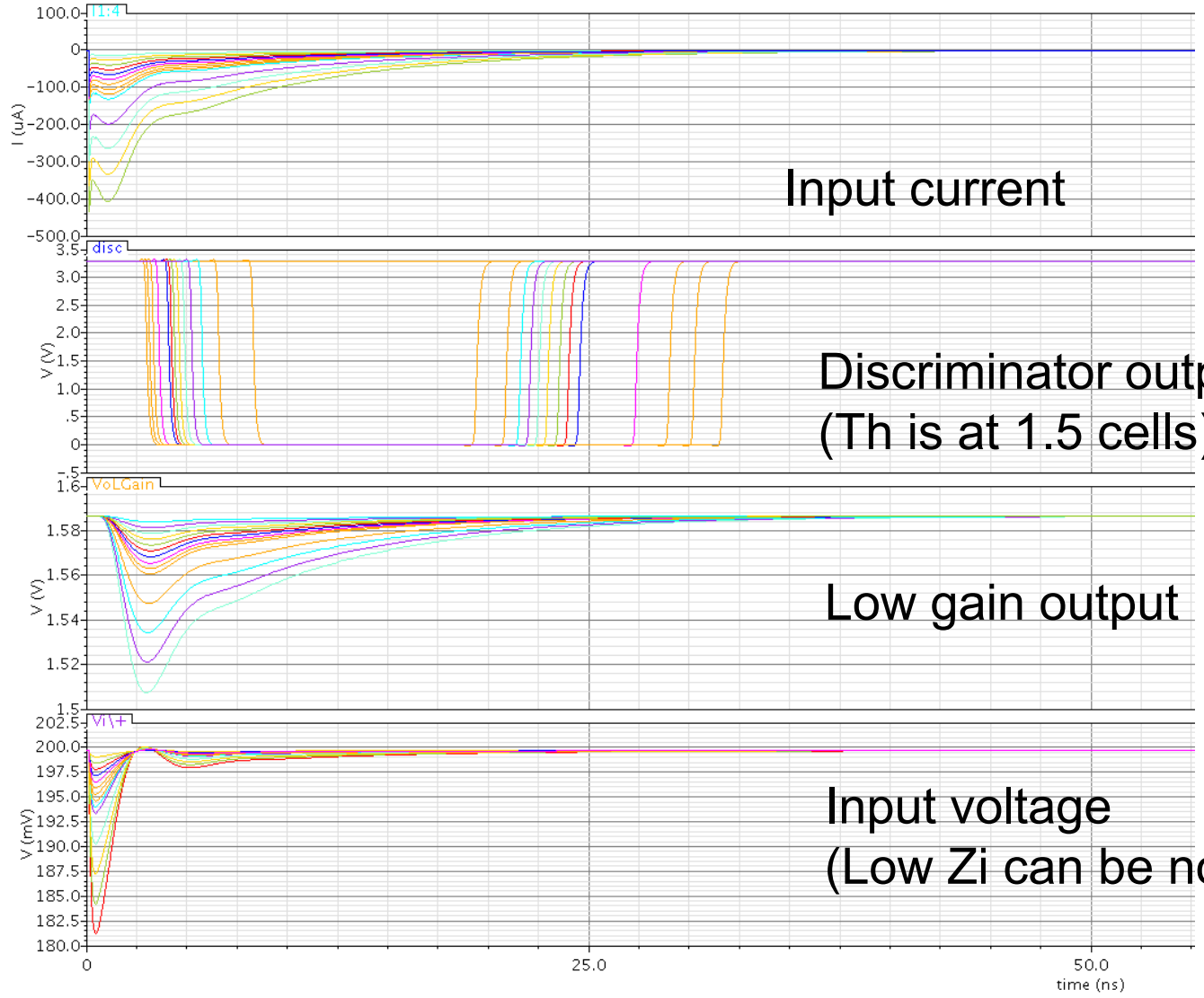
- Current mode feedback used
  - Optical comunications
  - SiPM readout
- For SciFi just remove outer loop
  - SiPM cathode can be tuned from 0 to 1 V
    - Base of Q1
  - Input impedance < 20 ohm



POWER 5 mW

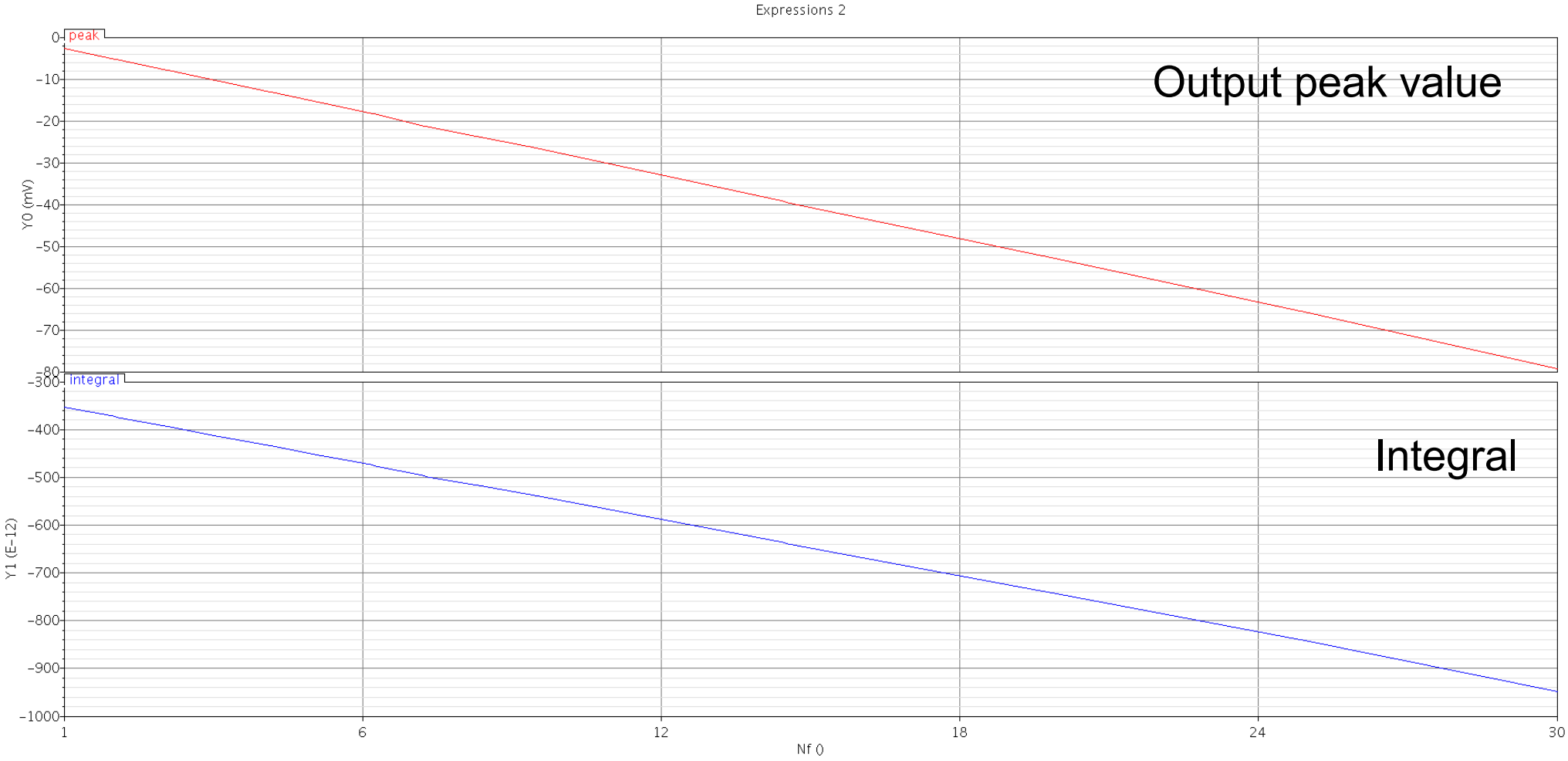
III. Simulations with ICECAL FE stage (LHCb Calo upgrade)

- Transient simulation (1 to 30 cells)



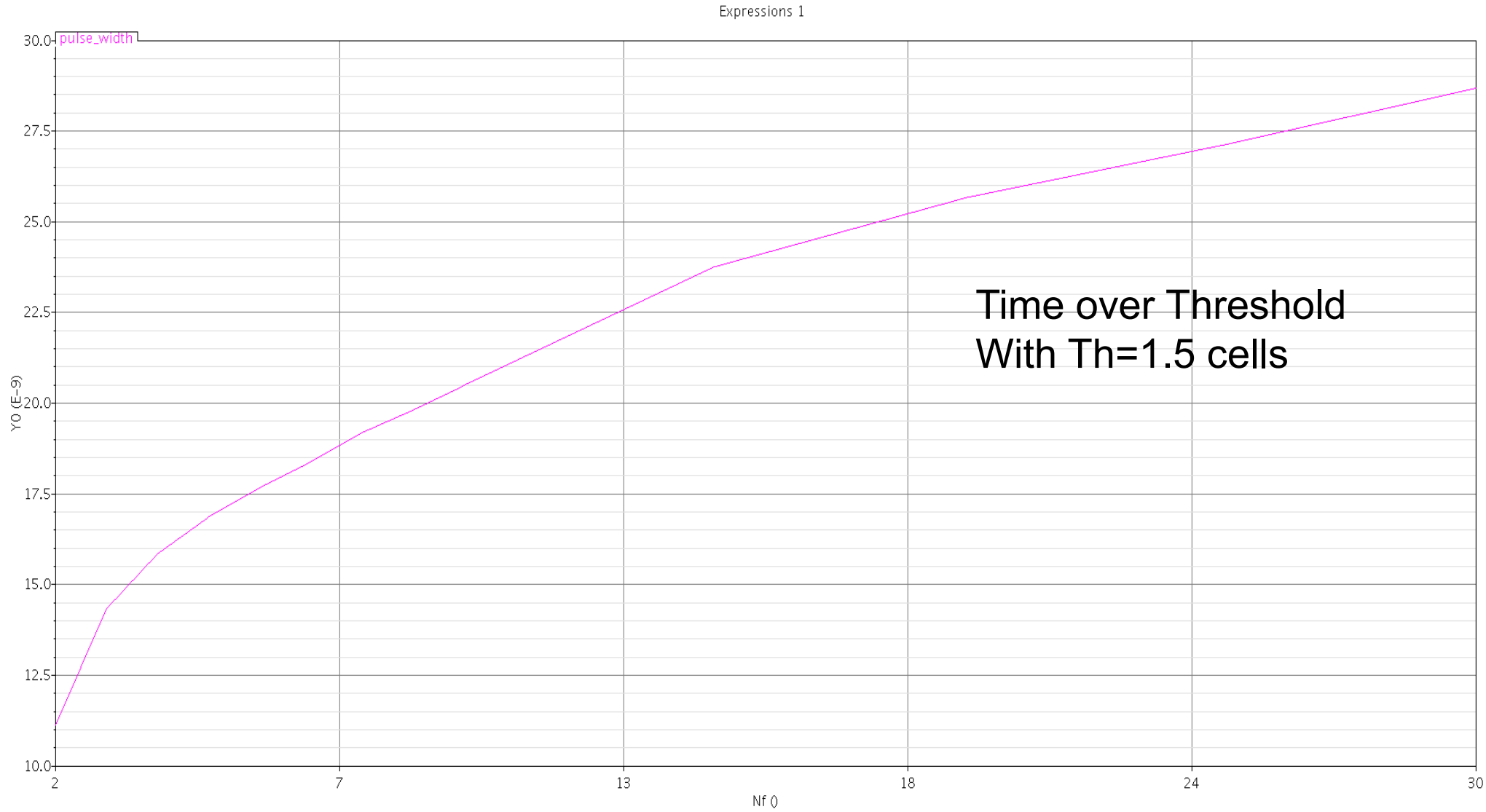
III. Simulations with ICECAL FE stage (LHCb Calo upgrade)

- Peak or integral measurements are ok as well



III. Simulations with a FE designed for PET

- Similar results for ToT



IV. Discussion

- Current mode input stage seems a good choice
  - Low input impedance and fast: minimize pile-up
  - As long as 5 mW/ch is ok
- Signal processing
  - With peak detection / integration problem is pushed to ADC
  - Is ToT feasible?
    - Detector simulation
    - Resolution needed? TDC implementation
- ADC, possible solutions:
  - Maybe multiplexed SAR 5bits ADC
  - Low power current mode cyclic ADCs
  - See next slides

Feasibility

Fast SAR ADCs

	ADC Flash				
	Choi	Deguchi	Yoo	Verbruggen	Paulus
Precision	6 bit	6 bit	6 bit	5 bit	6 bit
Echantillonnage	5 GS/s	3.5 GS/s	1 GS/s	1.75 GS/s	4GS/s
Technologie	65 nm	90 nm	250 nm	90nm	130 nm
Année	2008	2007	2001	2008	2004
Tension alimentation	1.3 V	0.9 V	2.5 V	1 V	1.5 V
Consommation	320 mW	98 mW	67 mW	7.6 mW	990 mW

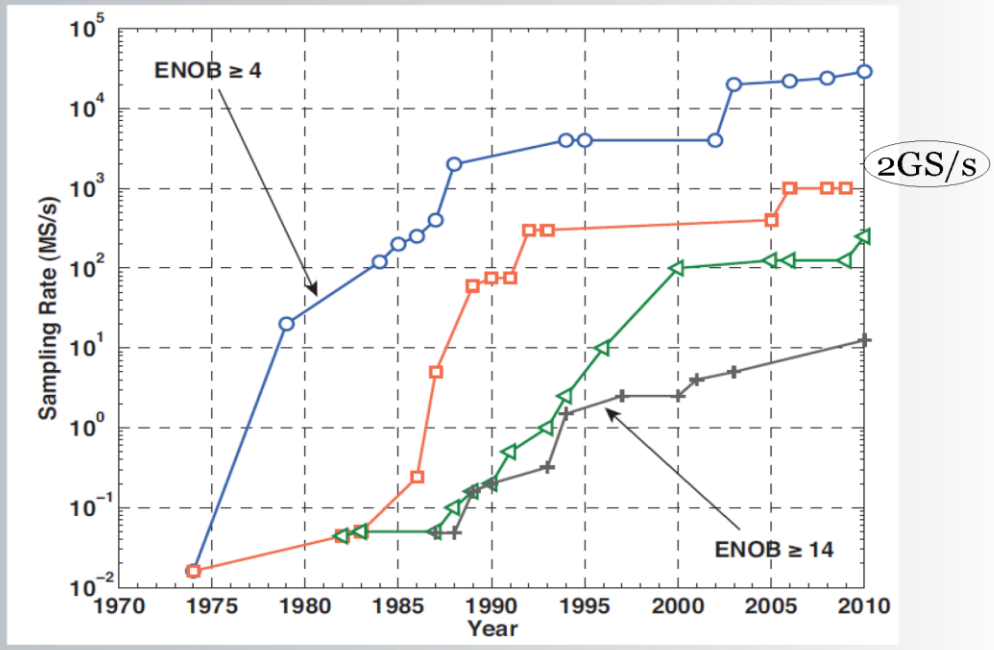
	ADC SAR			
	Draxelmayr	Chen	Ginsburg	Liu
Precision	6 bit	6 bit	5 bit	10 bit
Echantillonnage	600 MS/s	600 MS/s	500 MS/s	50 MS/s
Technologie	90 nm	130 nm	180 nm	130 nm
Année	2004	2006	2005	2009
Tension alimentation	1.2 V	1.2 V	1.2 V / 1.8 V	1.2 V
Consommation	10 mW	5.3 mW	7.8 mW	0.92 mW

Target specification:

- BW = 500 MHz
- SR = 2 GS/s
- 6 bit ; ENOB >=5 at 500 MHz

Promising state of the art

- Existing architectures in this range
- Some are power-efficient
- Development required to fit the specif.



B.E. Jonsson 2010, IEEE

B. Joly (LPC)

IV. Discussion

- Current mode cyclic ADC:
  - DCD chip (DEPFET readout): 180 nm CMOS
  - ADC core is 40 um x 55 um and 1 mW
  - Conversion time for 8 bits: 160 ns (fast version): 20 ns/bit
  - To be improved for 5 bits @ 40 MHz, unless analogue sparsification is used

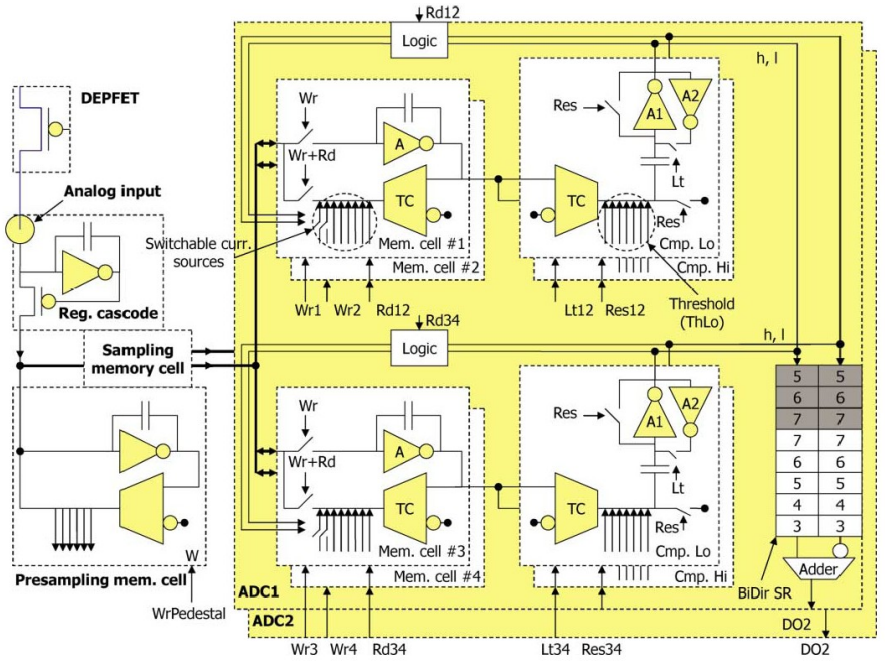


Fig. 2. Block diagram of the DCD channel. The channel consists of a signal receiver (regulated cascode), two current-mode ADCs and two additional sampling cells that allow double sampling. One DEPFET transistor is also shown.