Chieh Lin (National Changhua University of Education)

KOTO and KOTO-II DAQ

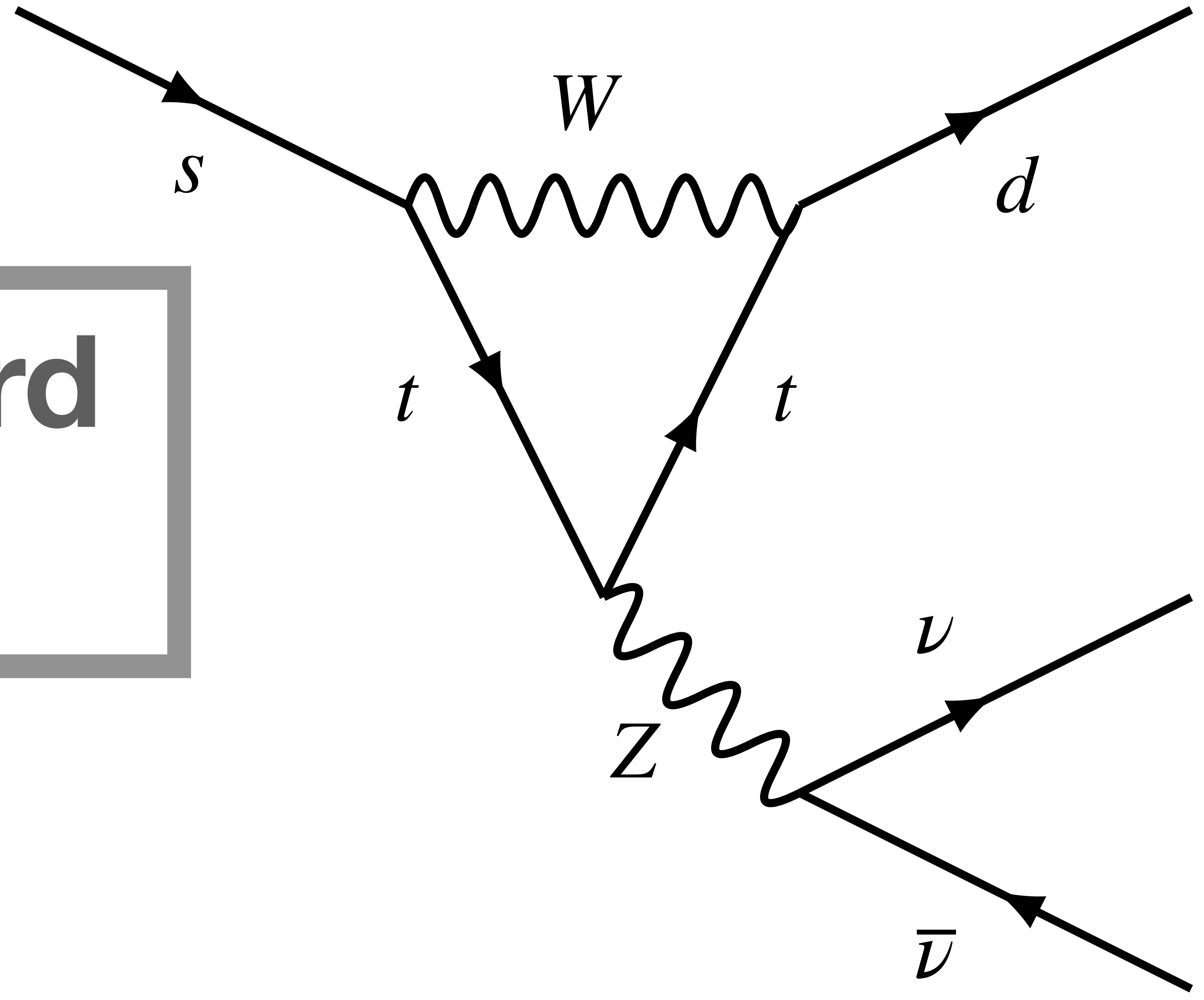
2nd computing challenges workshop (COMCHA)

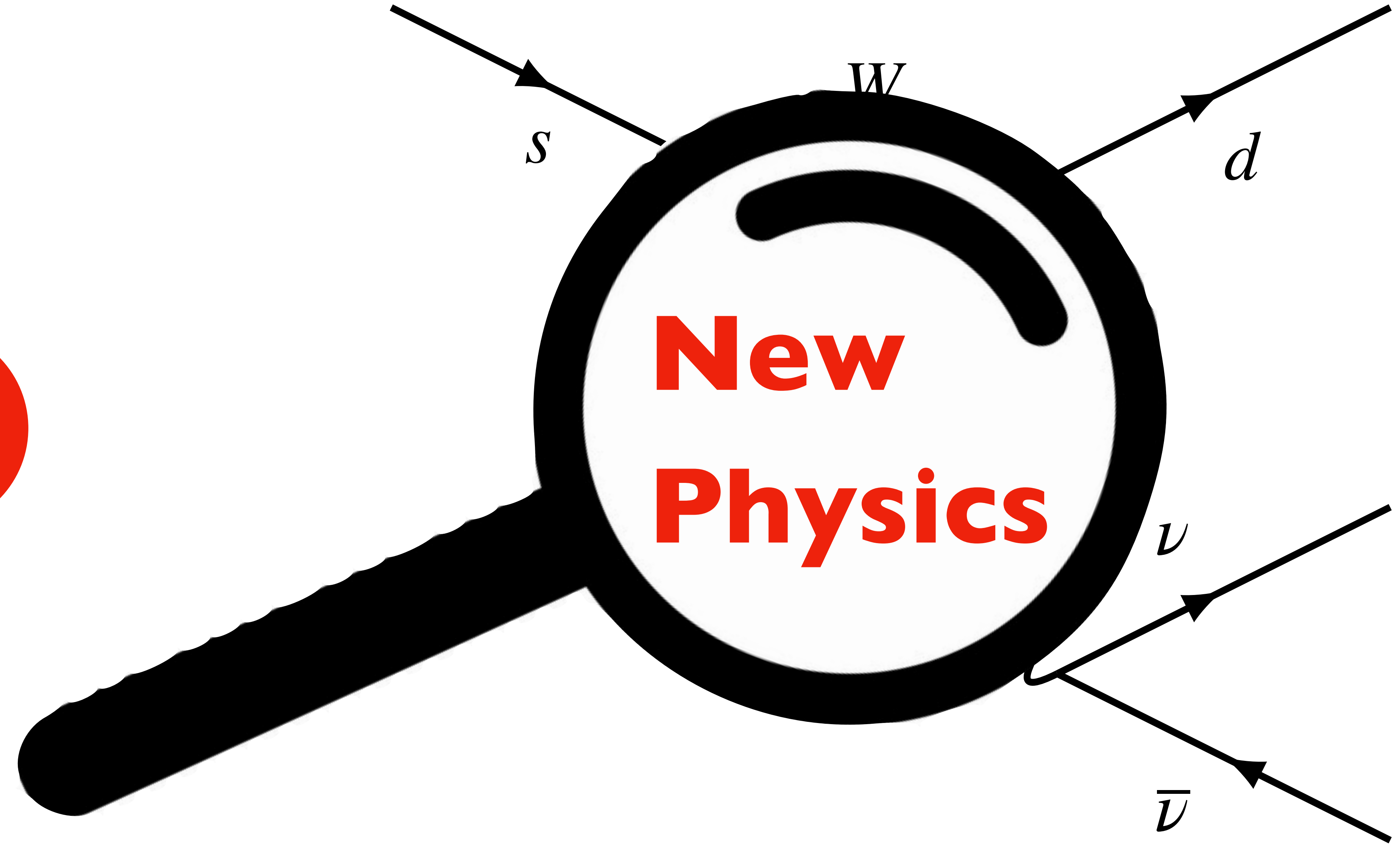
KOTO: Search for new physics via $K_L^0 \to \pi^0 \nu \bar{\nu}$

CP- CP+

$$K_L^0 \to \pi^0 \nu \bar{\nu}$$

Standard Model





$$\mathscr{B}(K_L^0 \to \pi^0 \nu \bar{\nu})_{SM} = 3 \times 10^{-11}$$

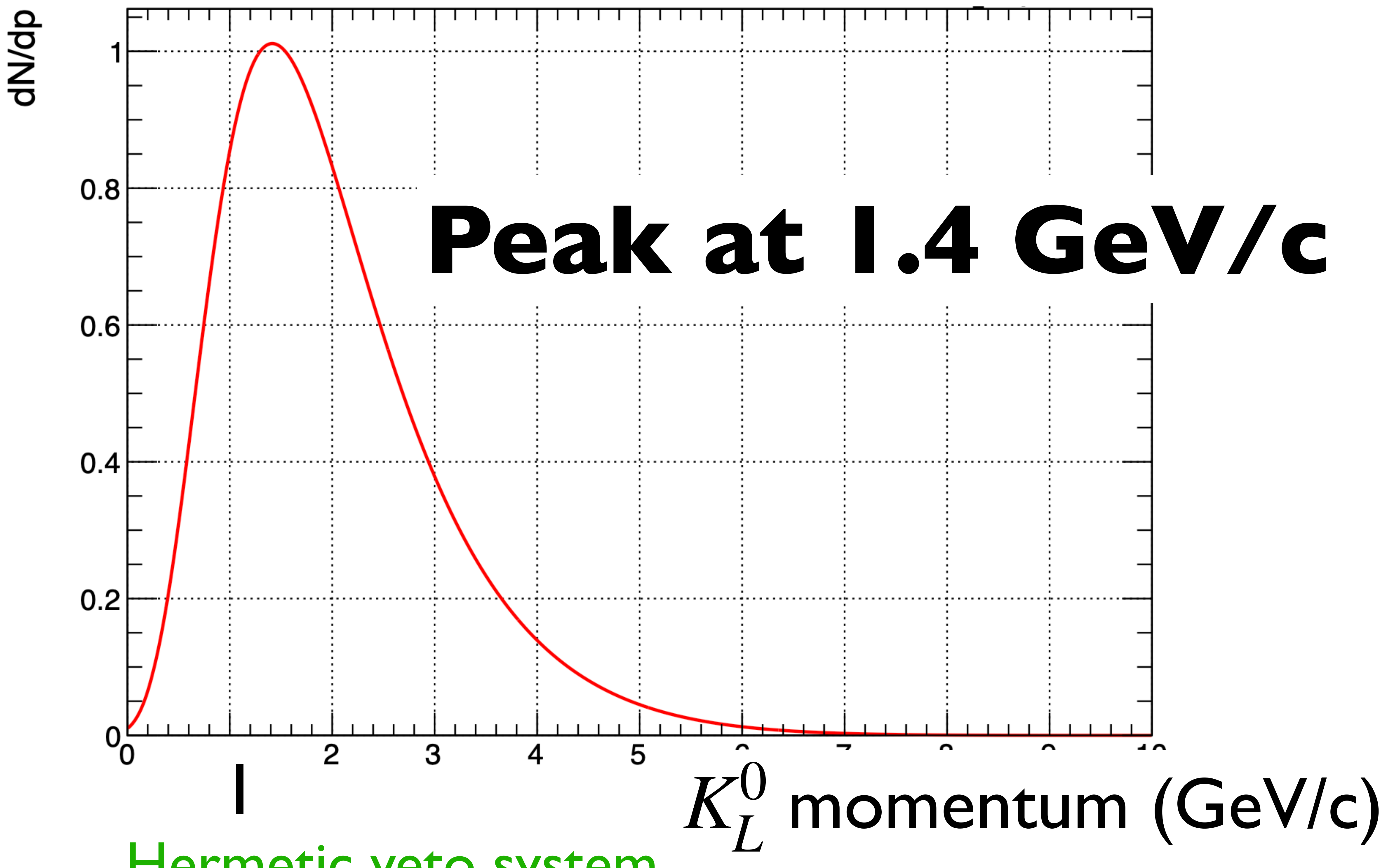
(2% error only)

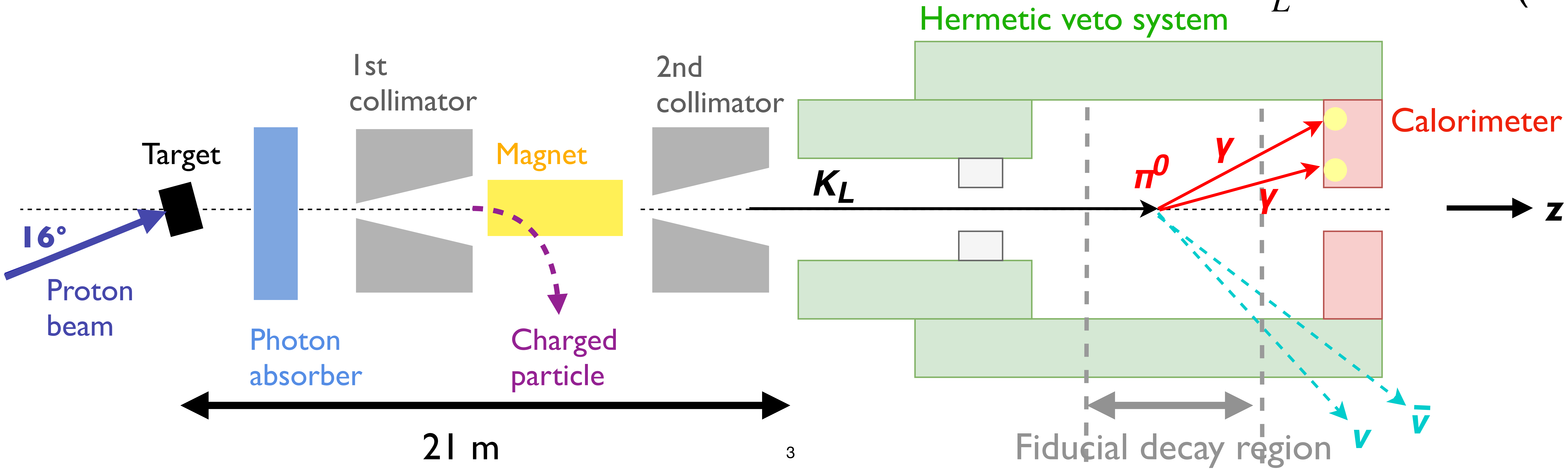
$$\frac{1}{\Lambda_{NP}^2} \to \Lambda_{NP} \sim \mathcal{O}(100) \text{ (TeV)}$$

Rare & Precisely-predicted → Sensitive to New Physics

The KOTO experiment

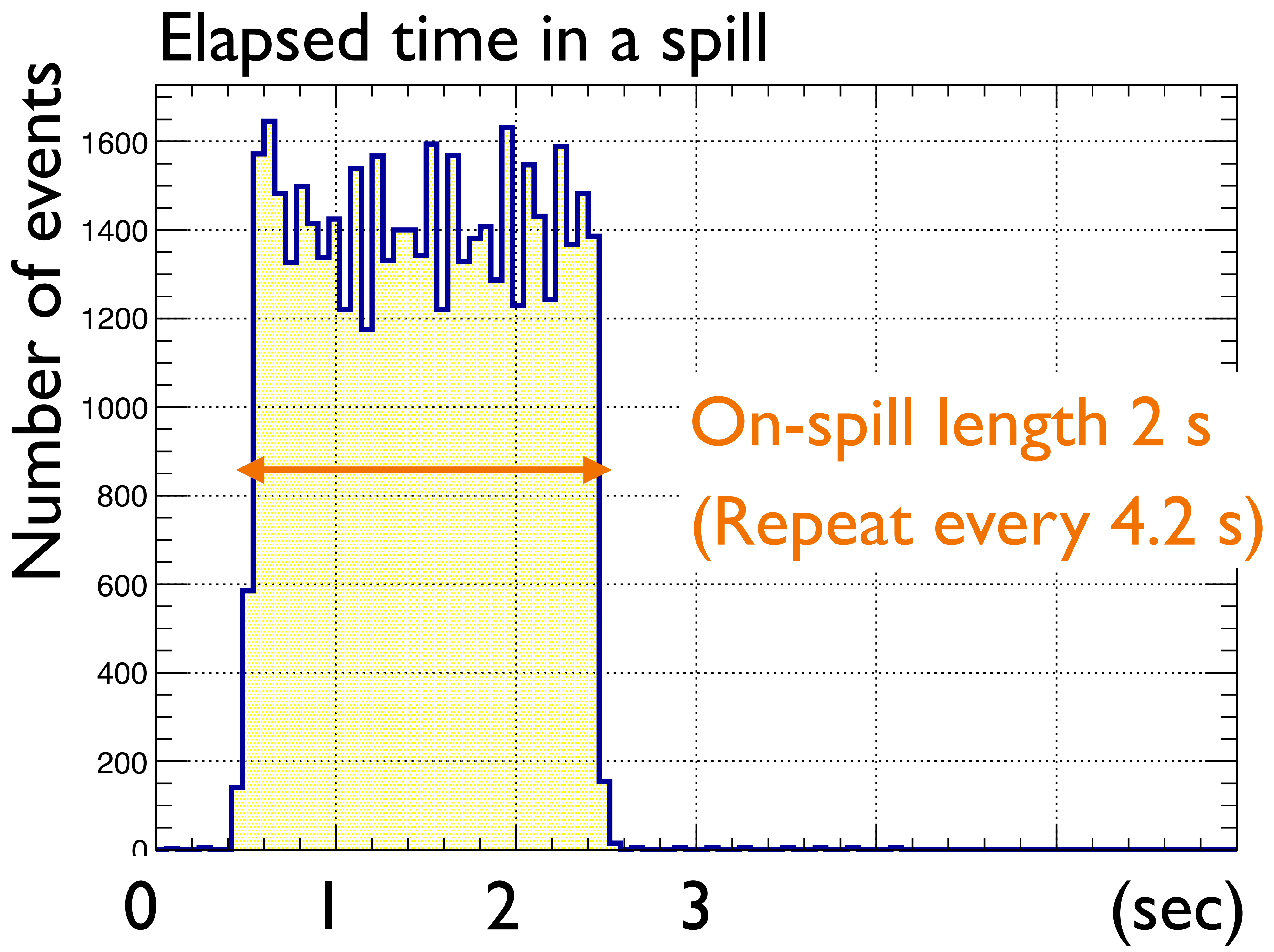
- 21-m-long beamline → Long-lived neutral particles (K_L^0, n, γ) are dominated.
- Two collimators → Sharpen the K_L^0 beam to measure the missing P_T of π^0.

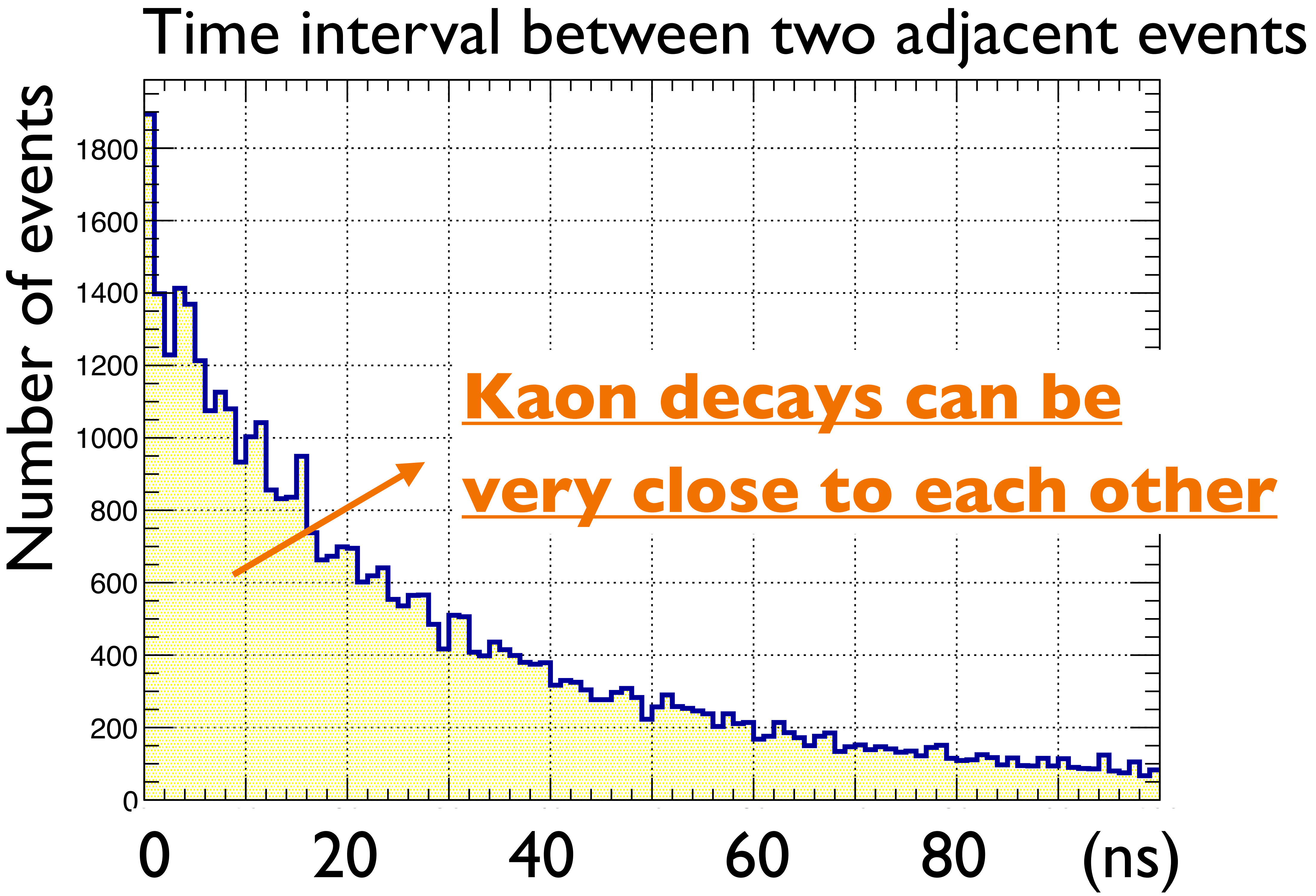




DAQ challenges to study the K_L^0 rare decays

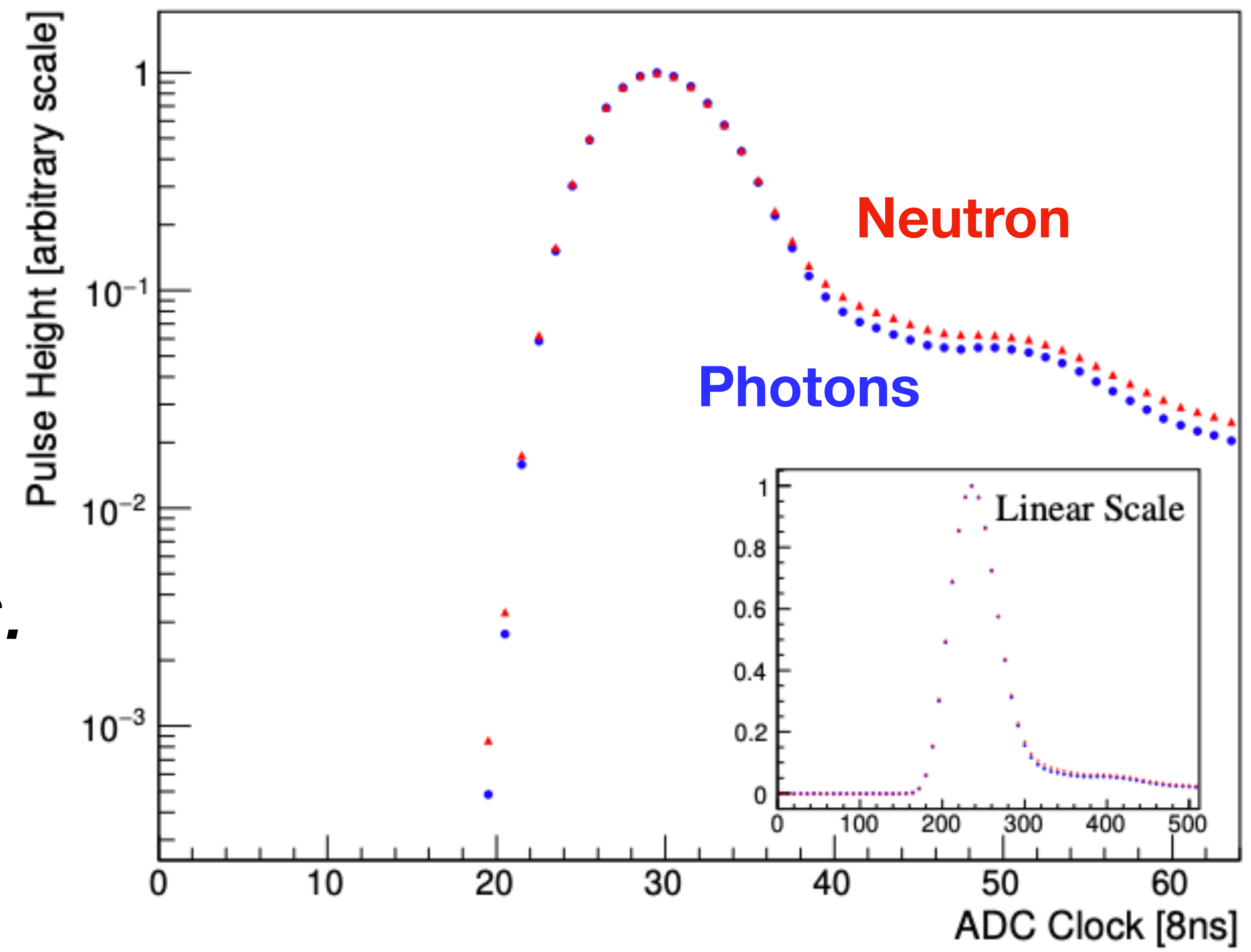
- **High intensity K_L^0 beam is required.**
  → *Triggers need to be processed fast.*





DAQ challenges to study the K_L^0 rare decays

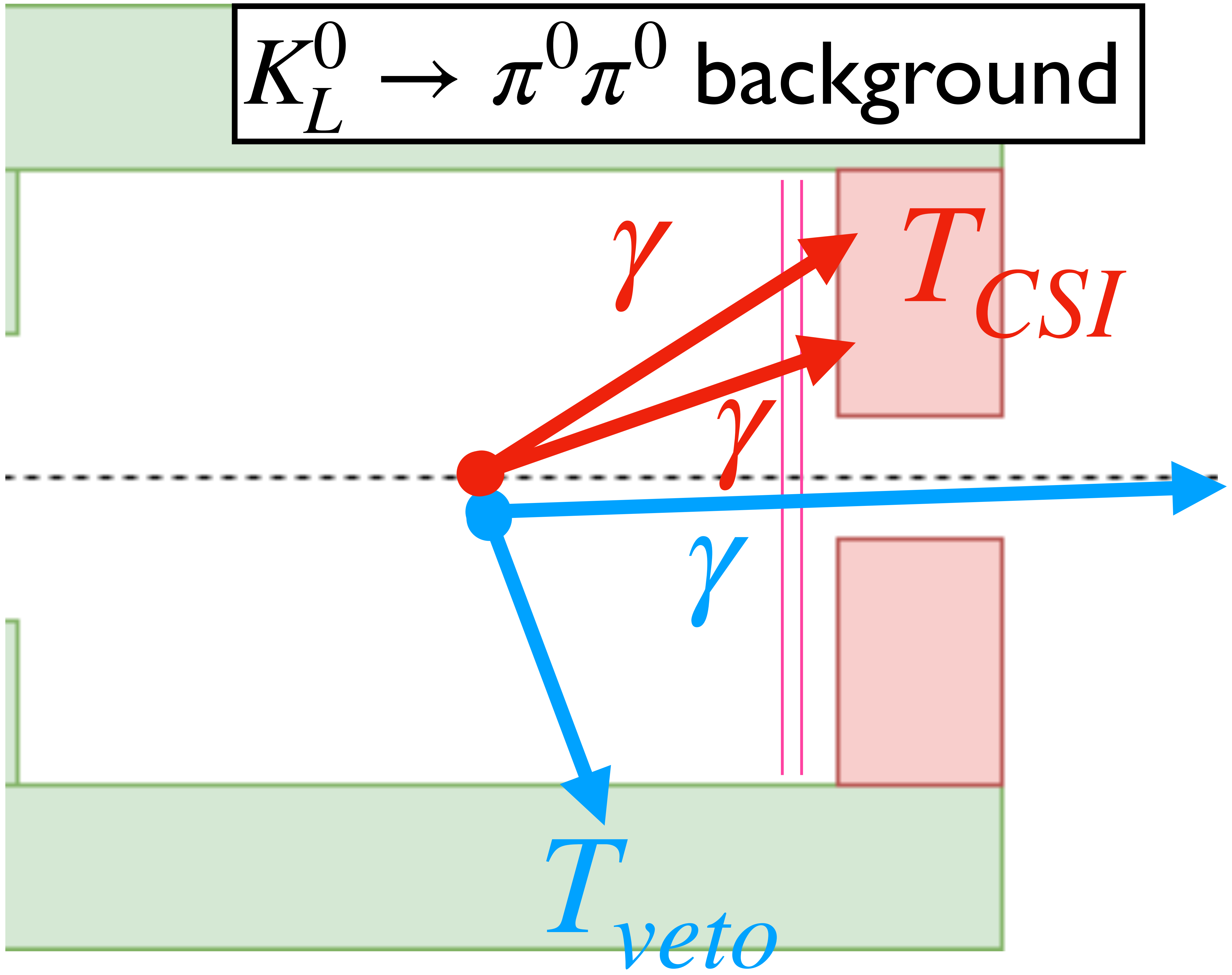
- **Backgrounds are also rare.**
  → *The waveform shapes are utilized to further suppress the rare background events.*
  → *Entire pulses need to be recorded.*

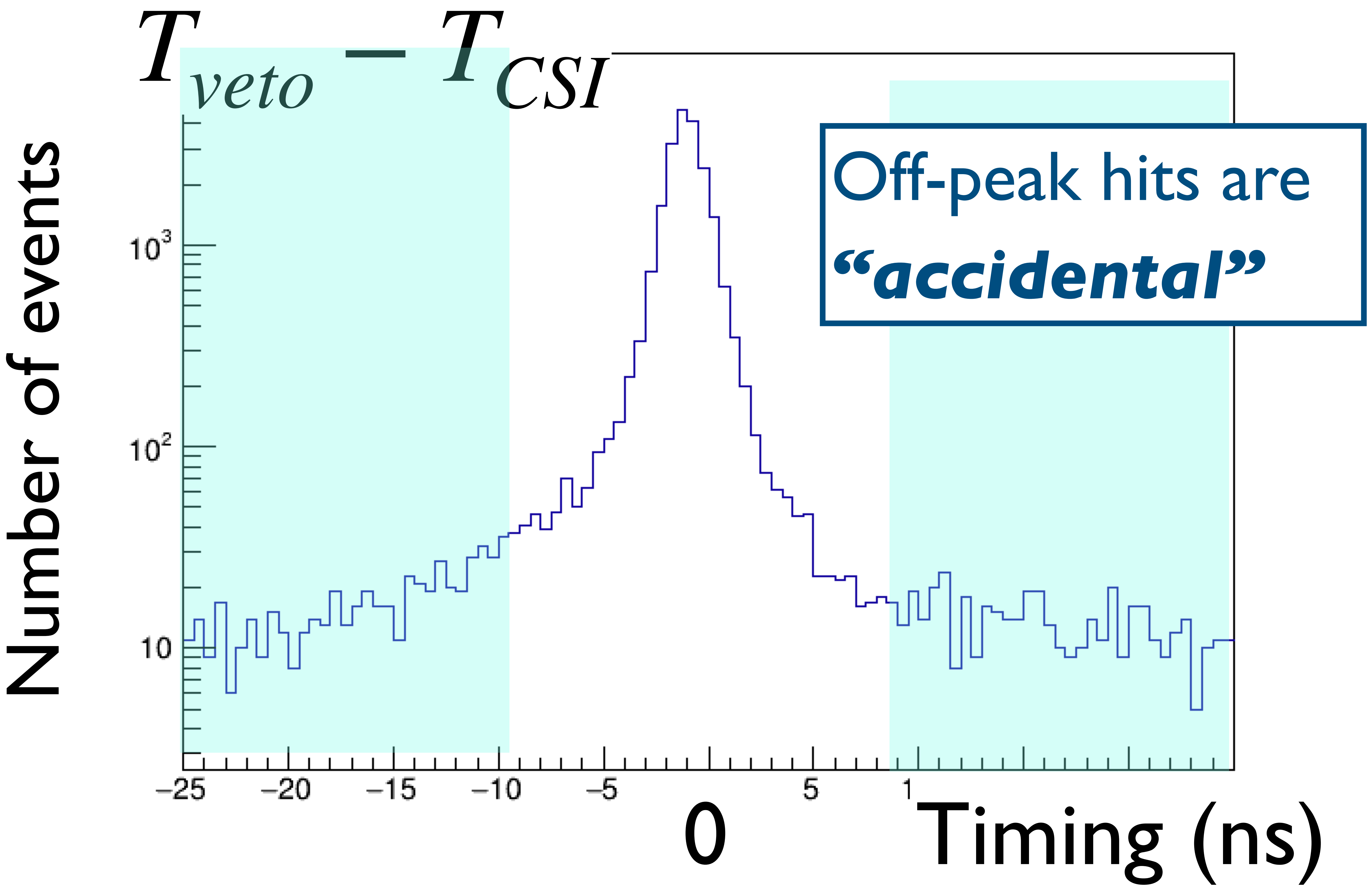


[Y.C. Tung, NIM A,1059 (2024) 169010]

DAQ challenges to study the K_L^0 rare decays

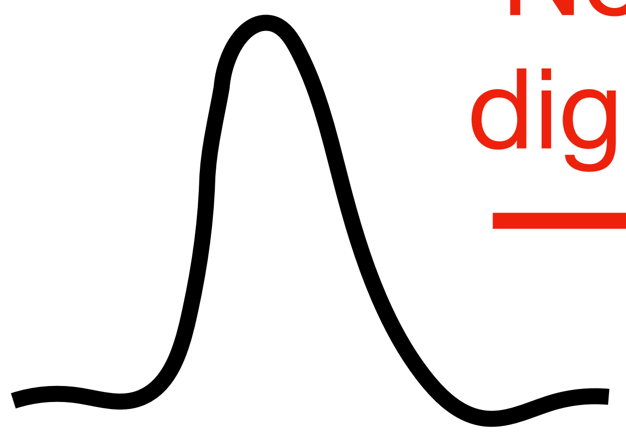
- **Many accidental hits.**
  → *Online timing window needs to be accurate to avoid overkilling signal events.*





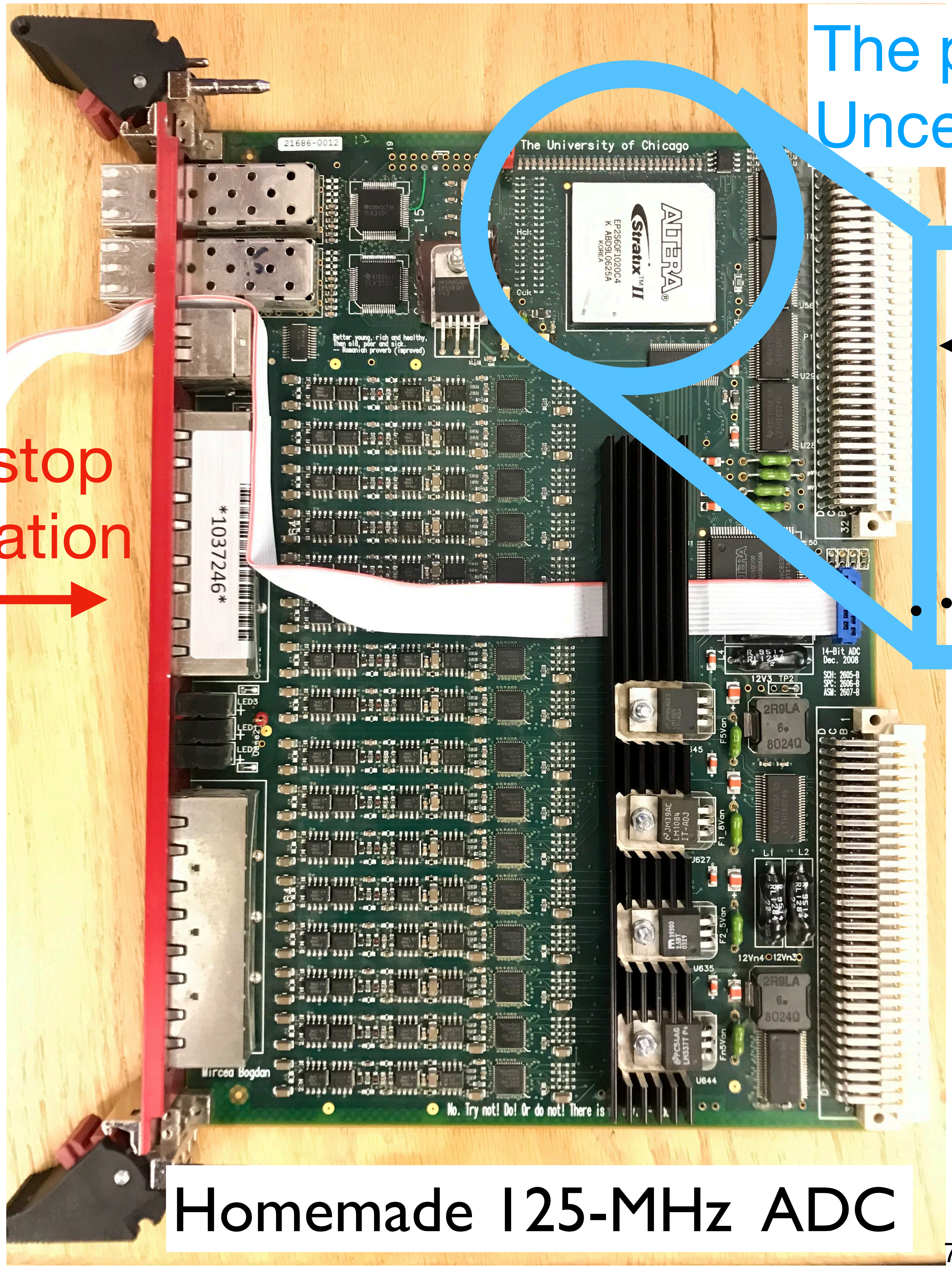
PIPELINE: Keynote of the KOTO trigger design

The pipeline is realized by the on-chip memory (FPGA).
Uncertainties from delay cables are eliminated.

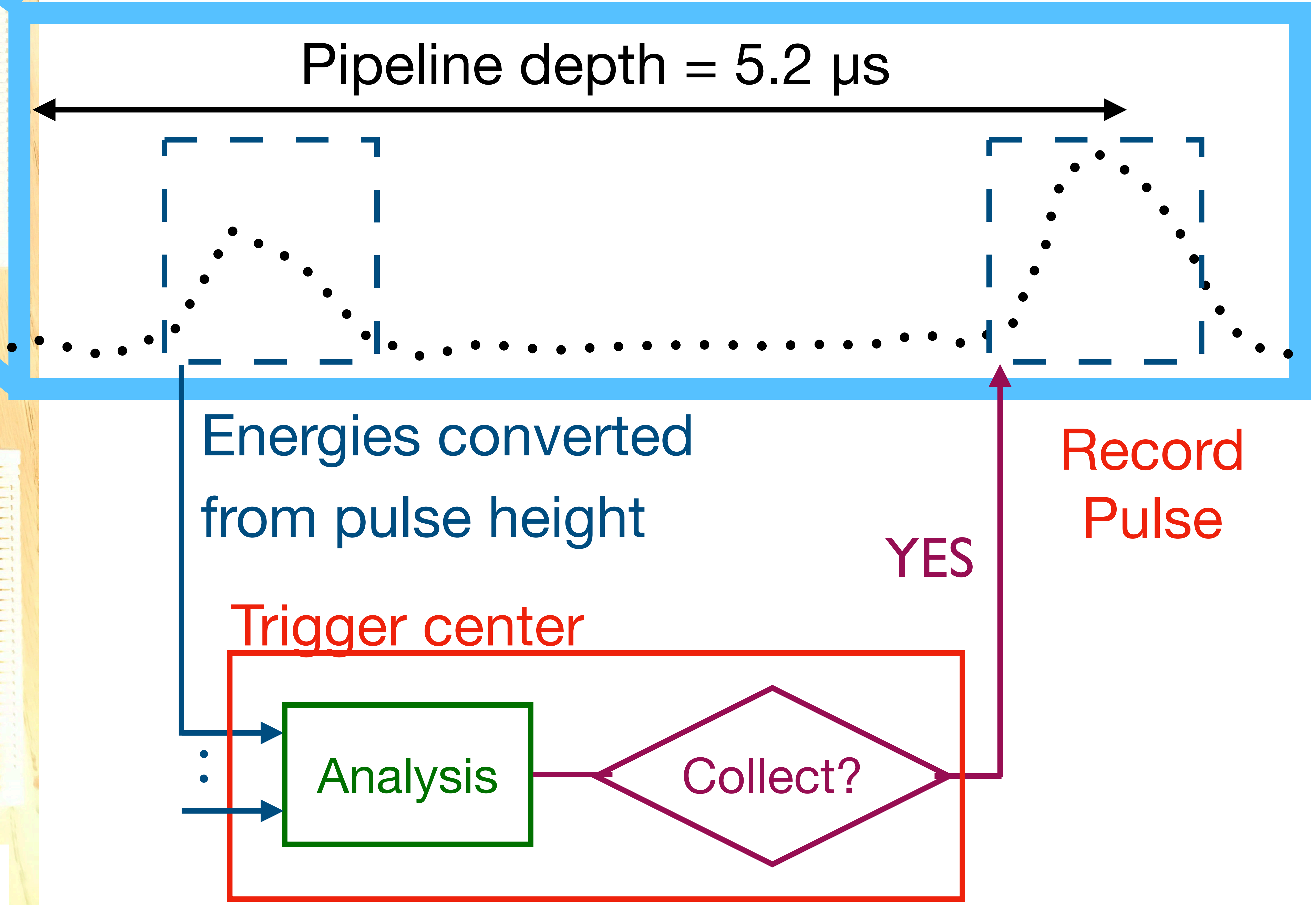


Analog input

Non-stop digitization



Homemade 125-MHz ADC



Upstream two-level trigger system

Evaluated every 8 ns.

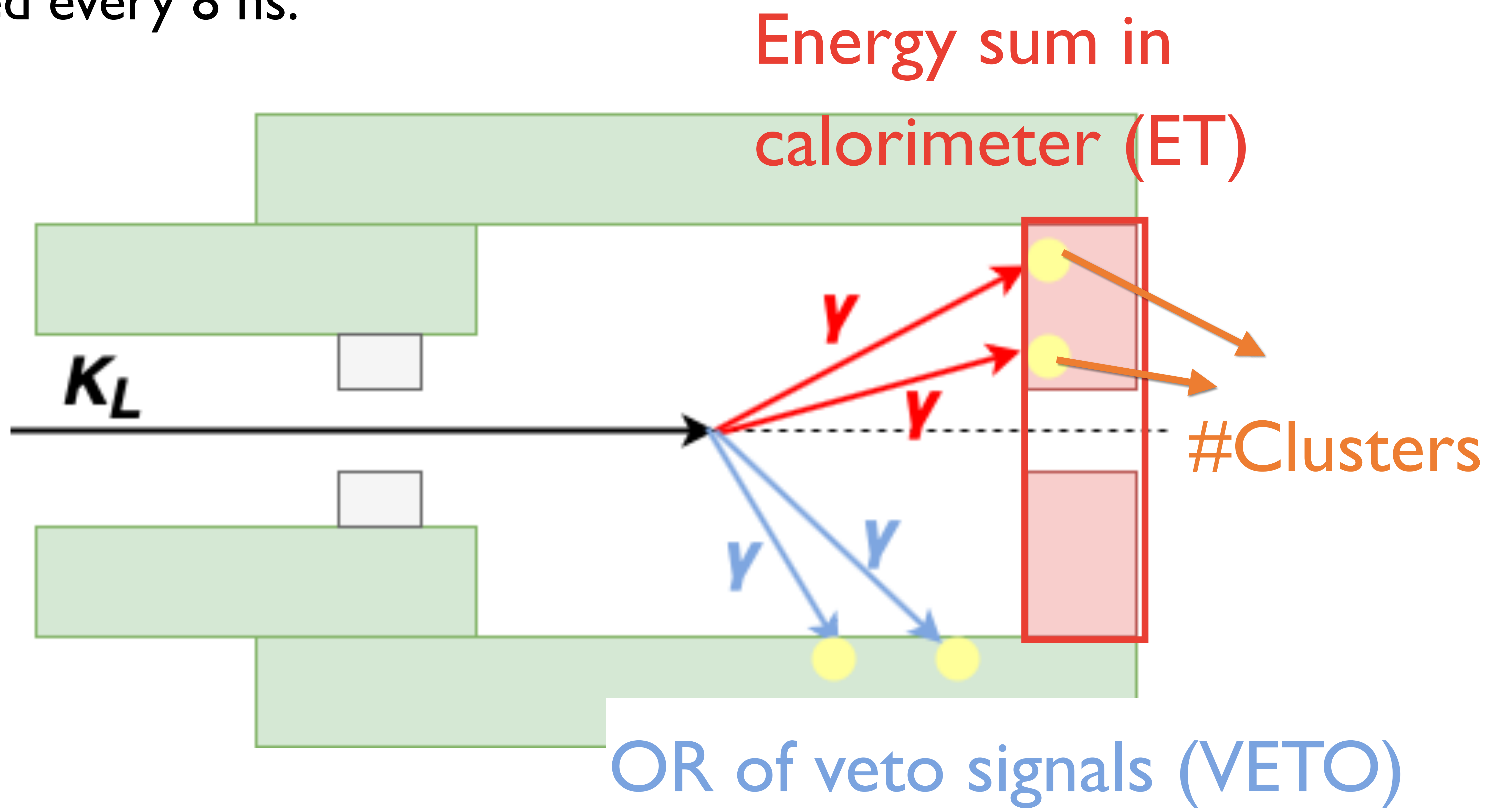
Level-1 trigger
ET & !VETO

↓ **Fulfilled?**

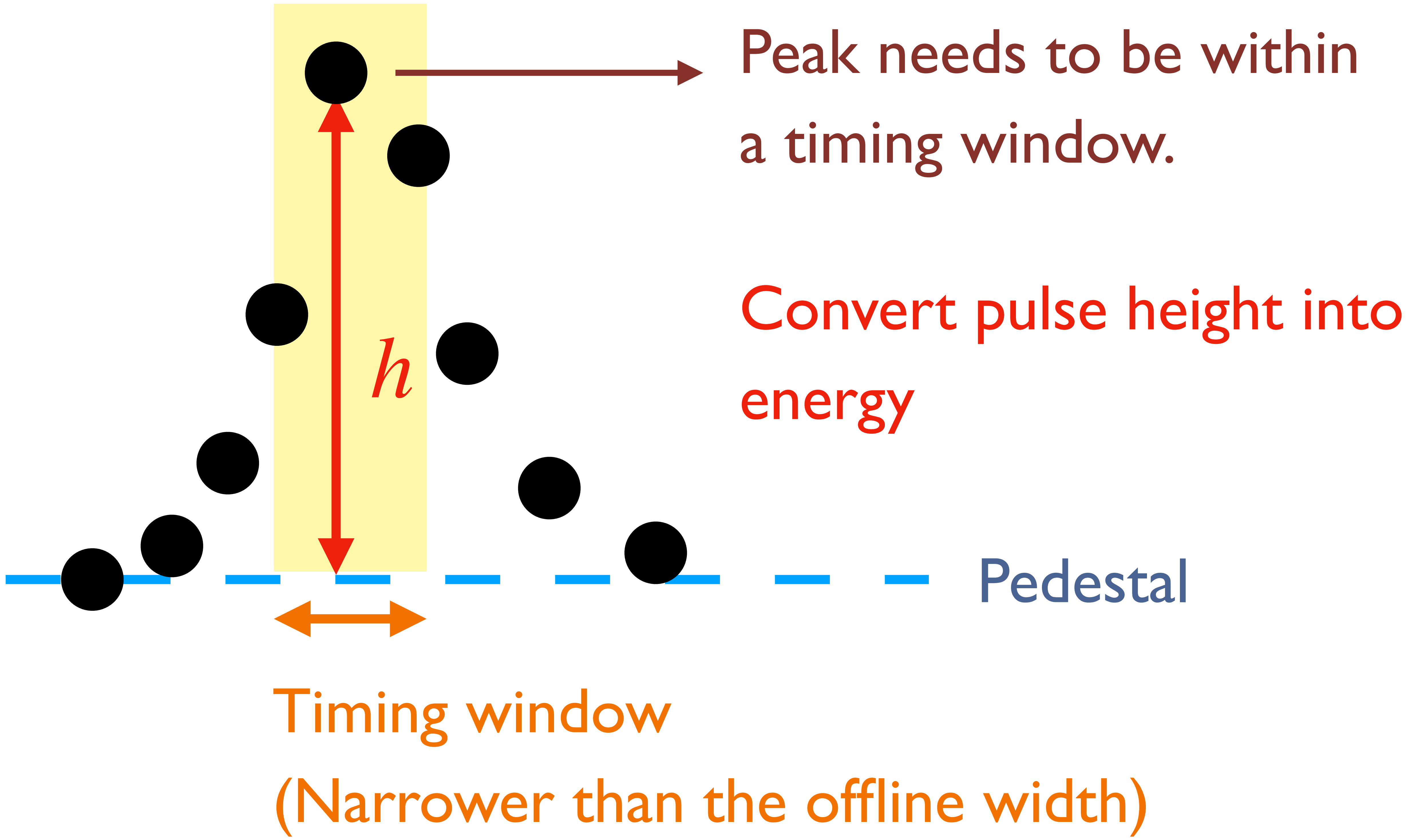
Level-2 trigger
#Cluster = 2

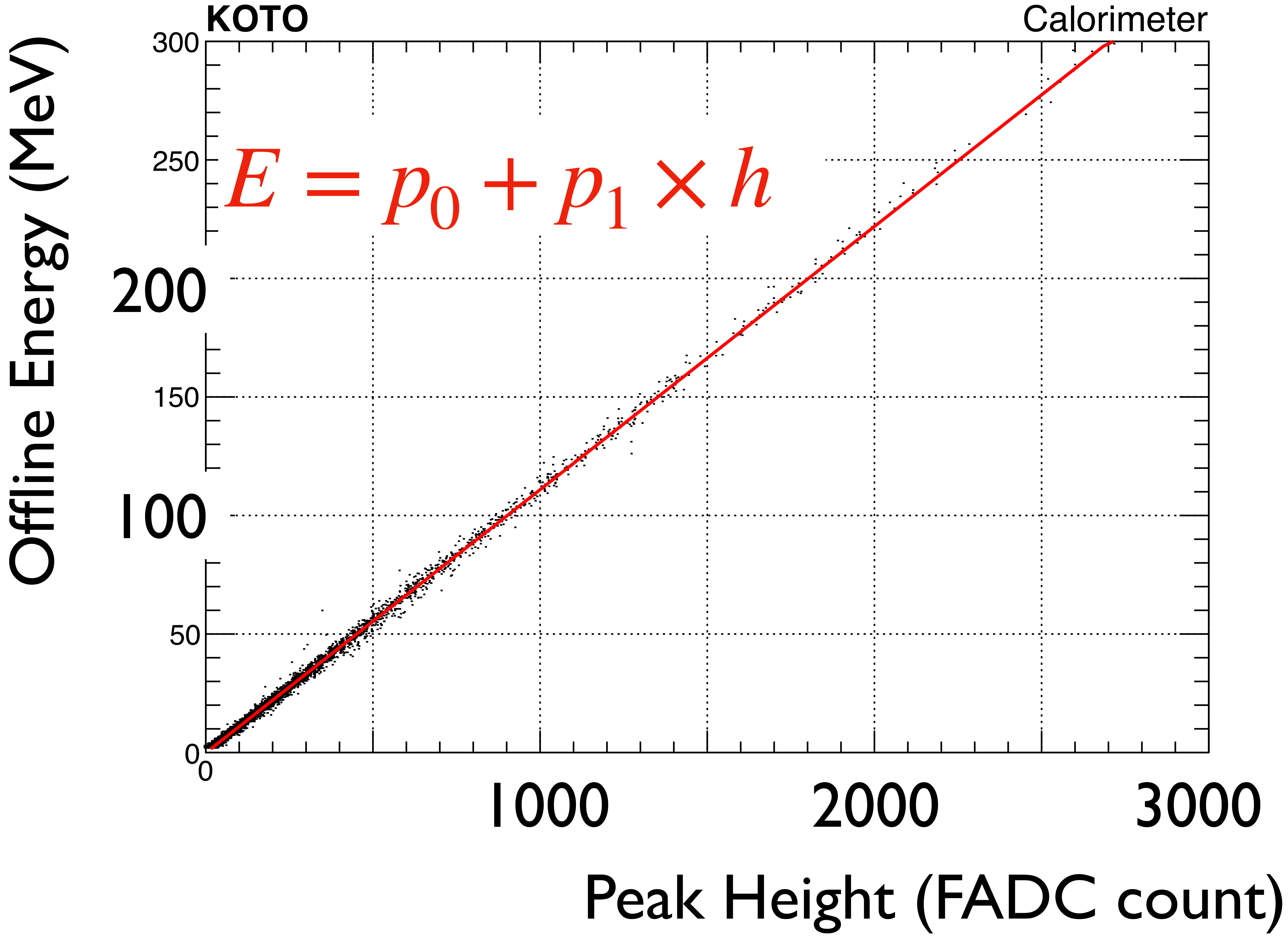
↓ **Fulfilled?**

Send to PC

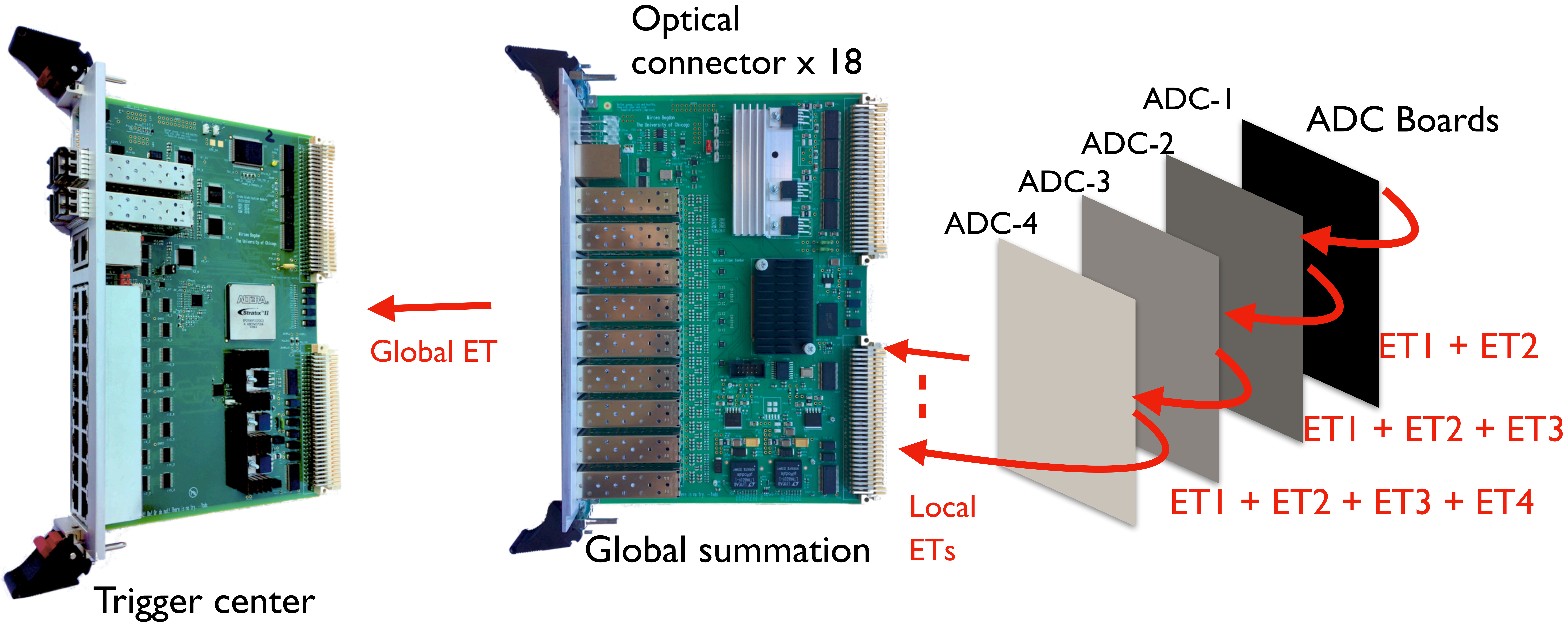


Level-1 trigger algorithm





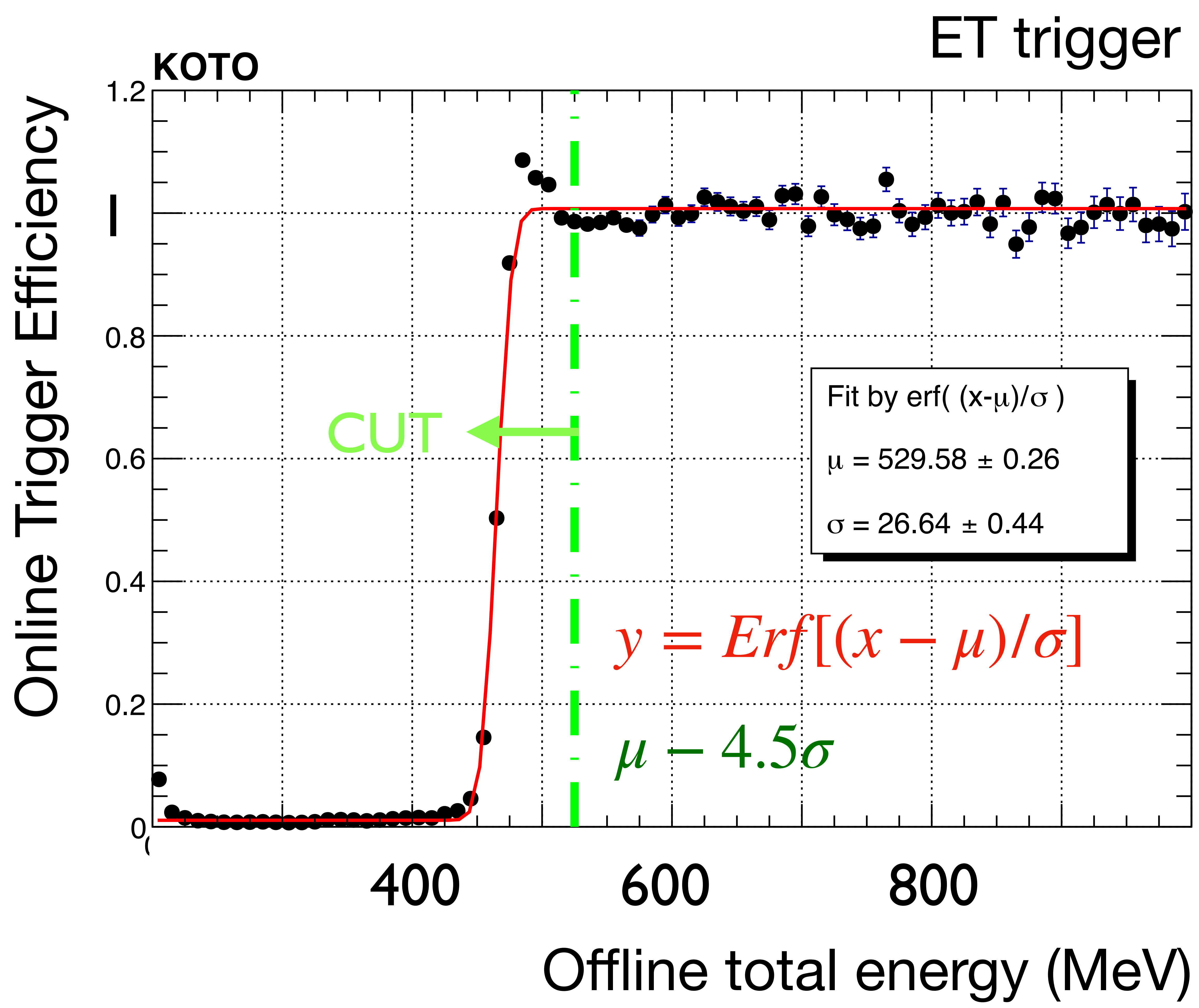
Total energy (ET) calculation

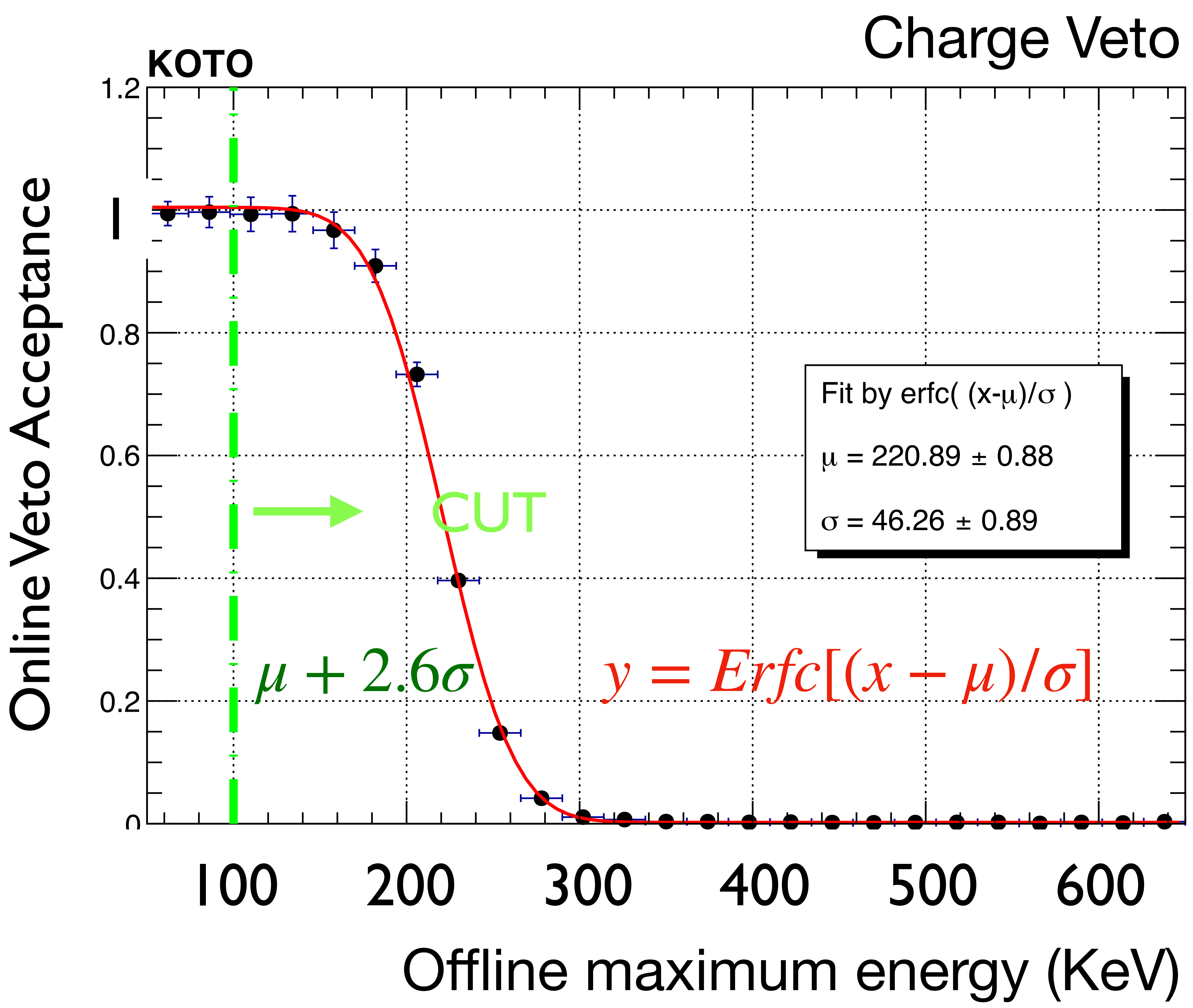


Total energy is aggregated through Daisy Chains.

Level-1 trigger performance

- ET Loss is negligible. Veto loss is <1%.

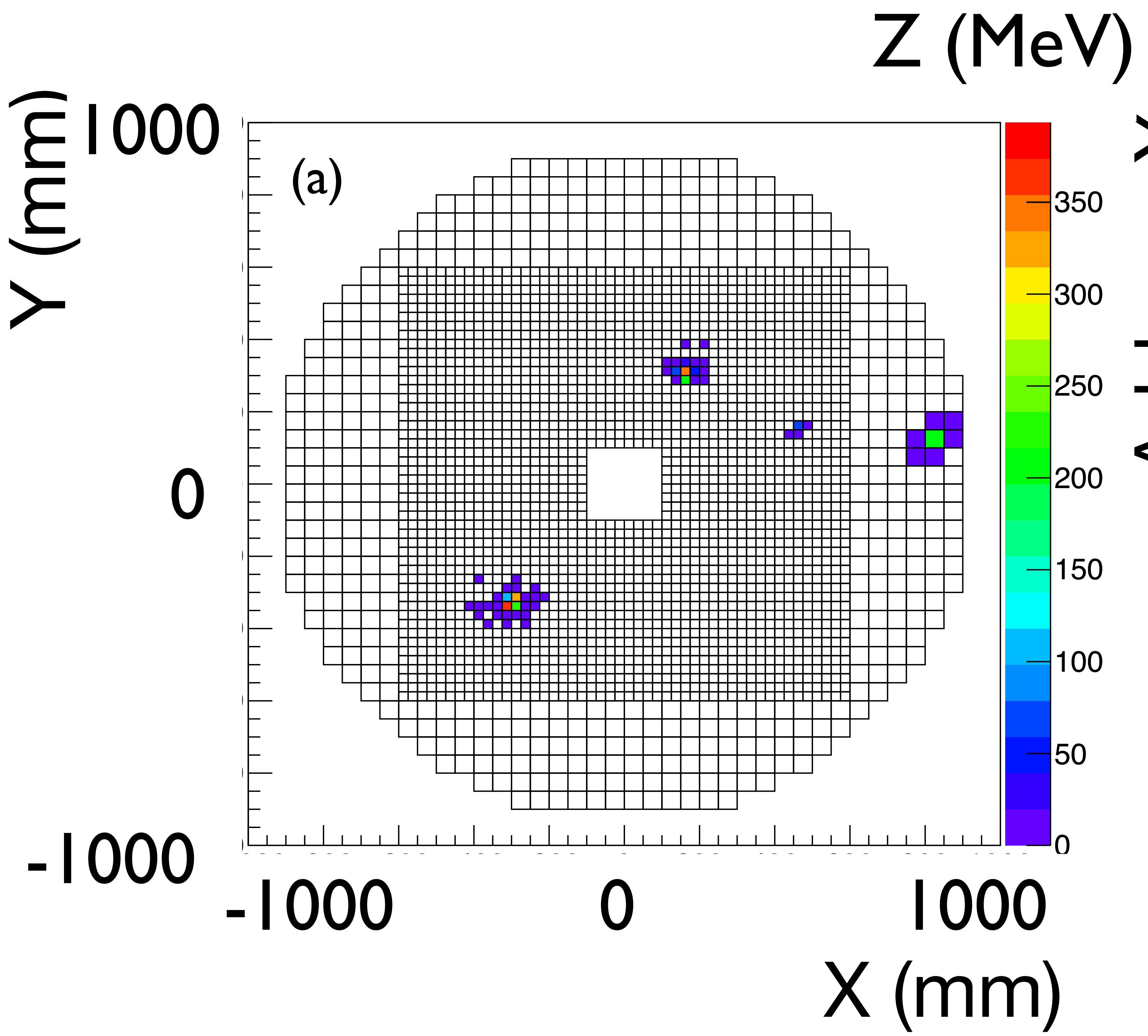




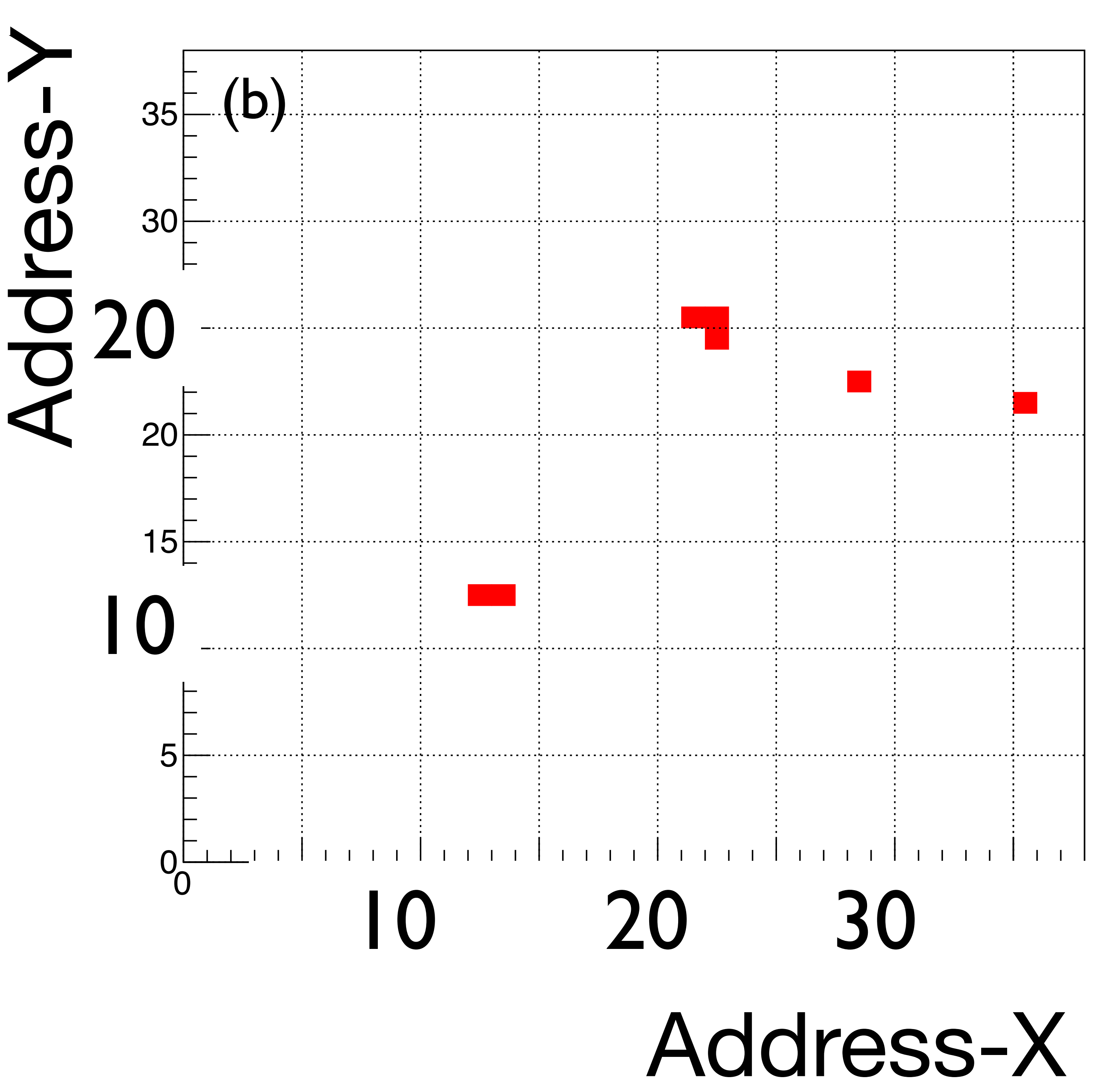
Level-2 trigger: cluster-counting

System dead time = 0.16 μs ⟹ Loss < 2% due to congestion (2024 run).

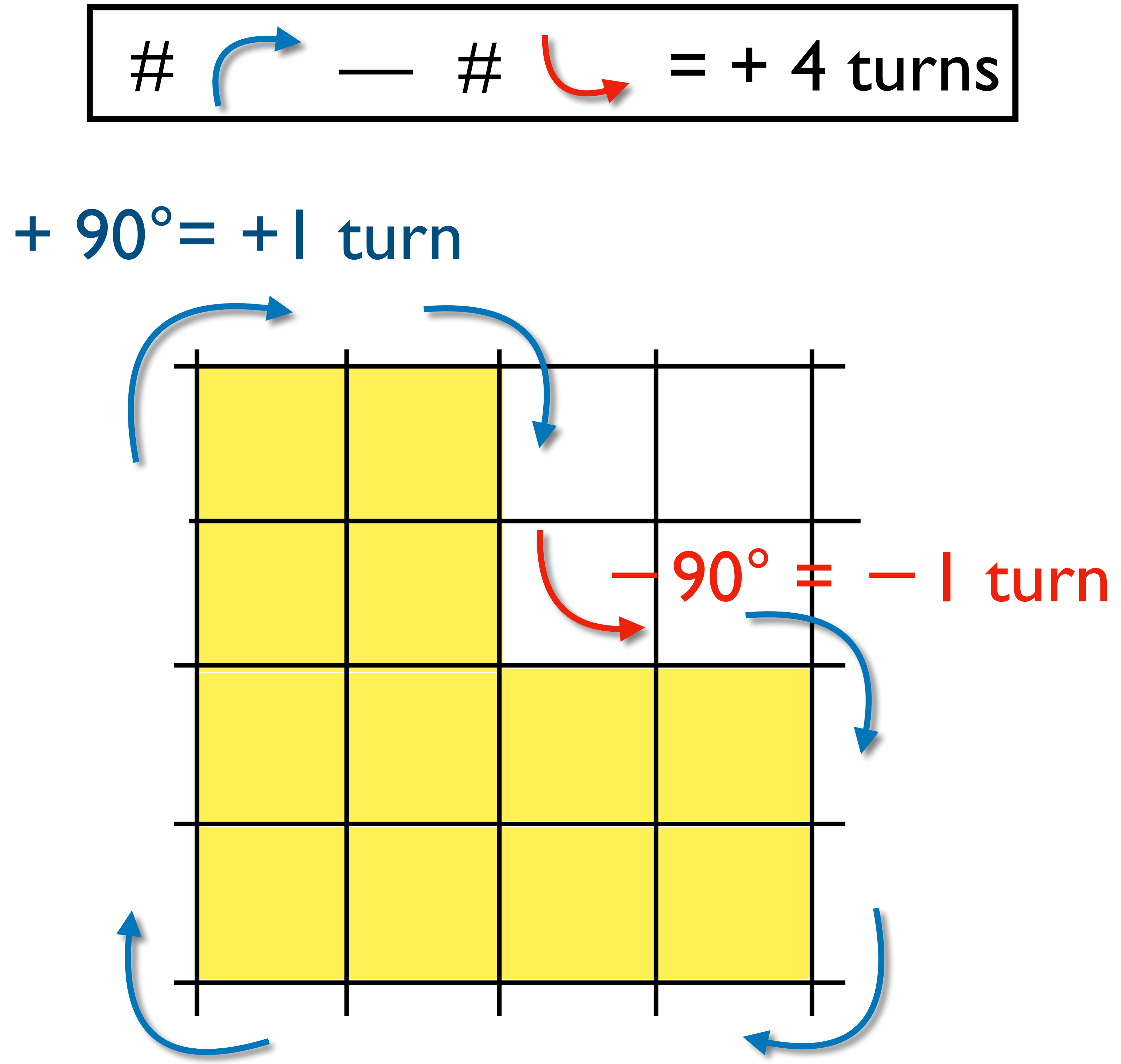
Energy distribution of an event with four hits.



Online hit map (38 x 38 bits) for cluster-counting



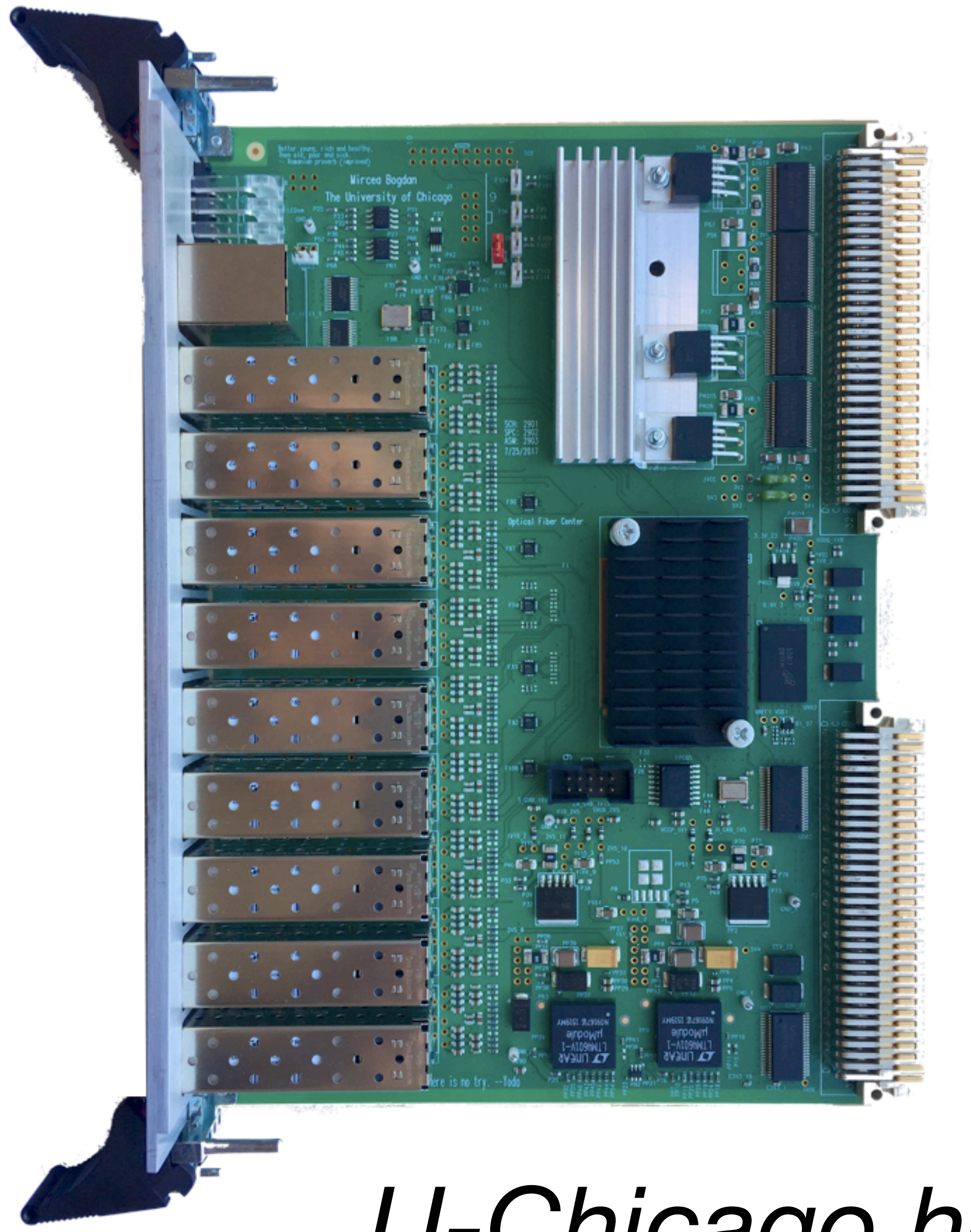
Count turns / 4 = #clusters



Architecture of the KOTO DAQ System

Event-building modules

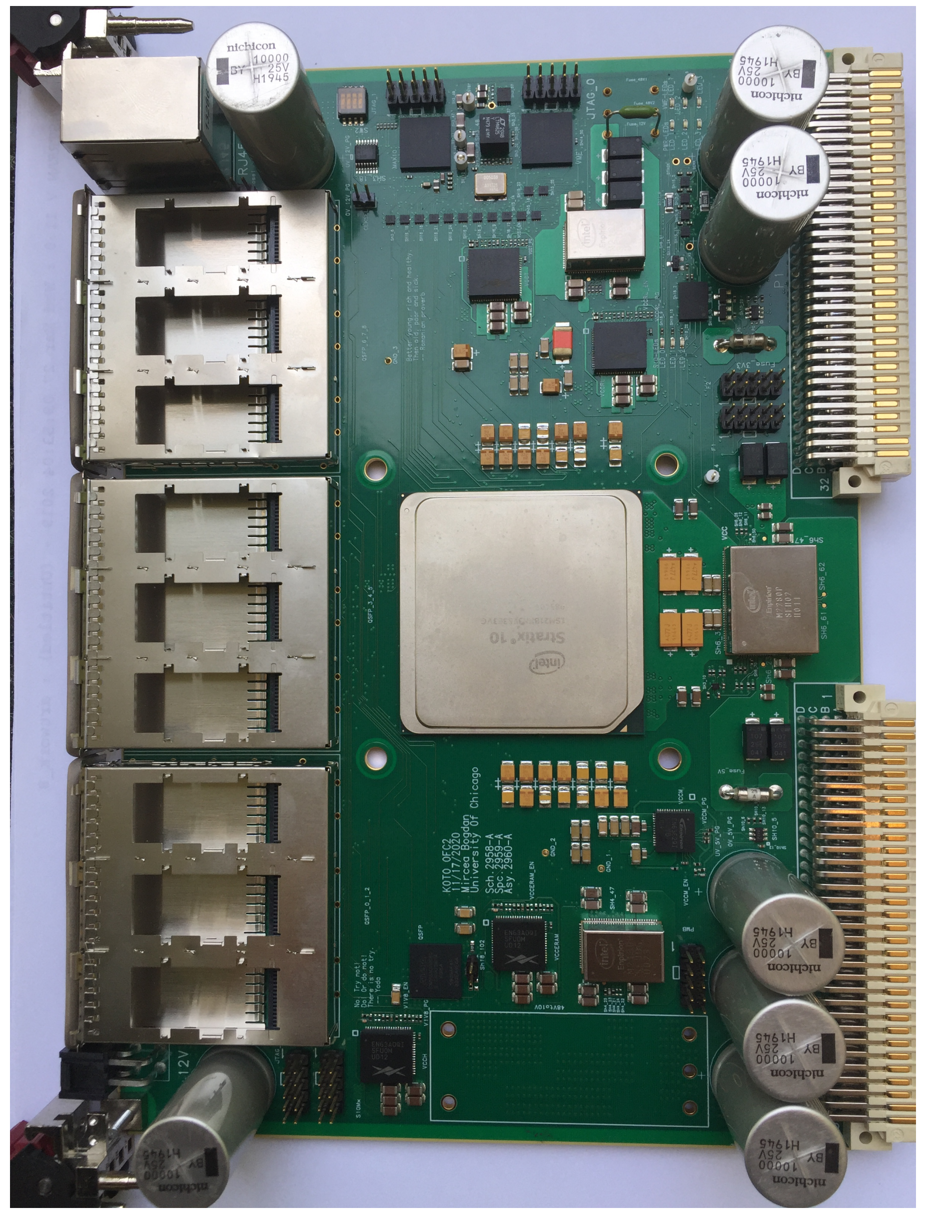
- The board equipped with high-speed numerous optical links are commissioned to build KOTO events.
- The OFC-I board is expected to be the bottleneck of the system.
- With two OFC-II boards, the loss is expected to be <1% if the trigger rate is < 50k / (spill = 4.2 seconds).



OFC-I

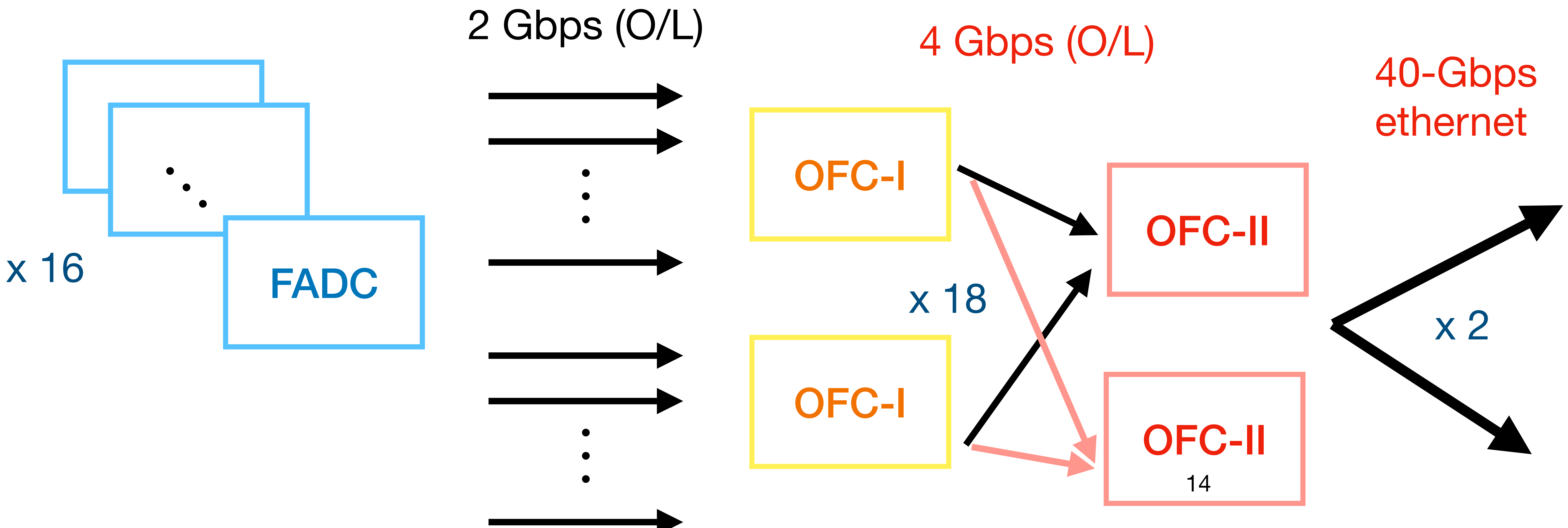
18 SFPs

U-Chicago homemade

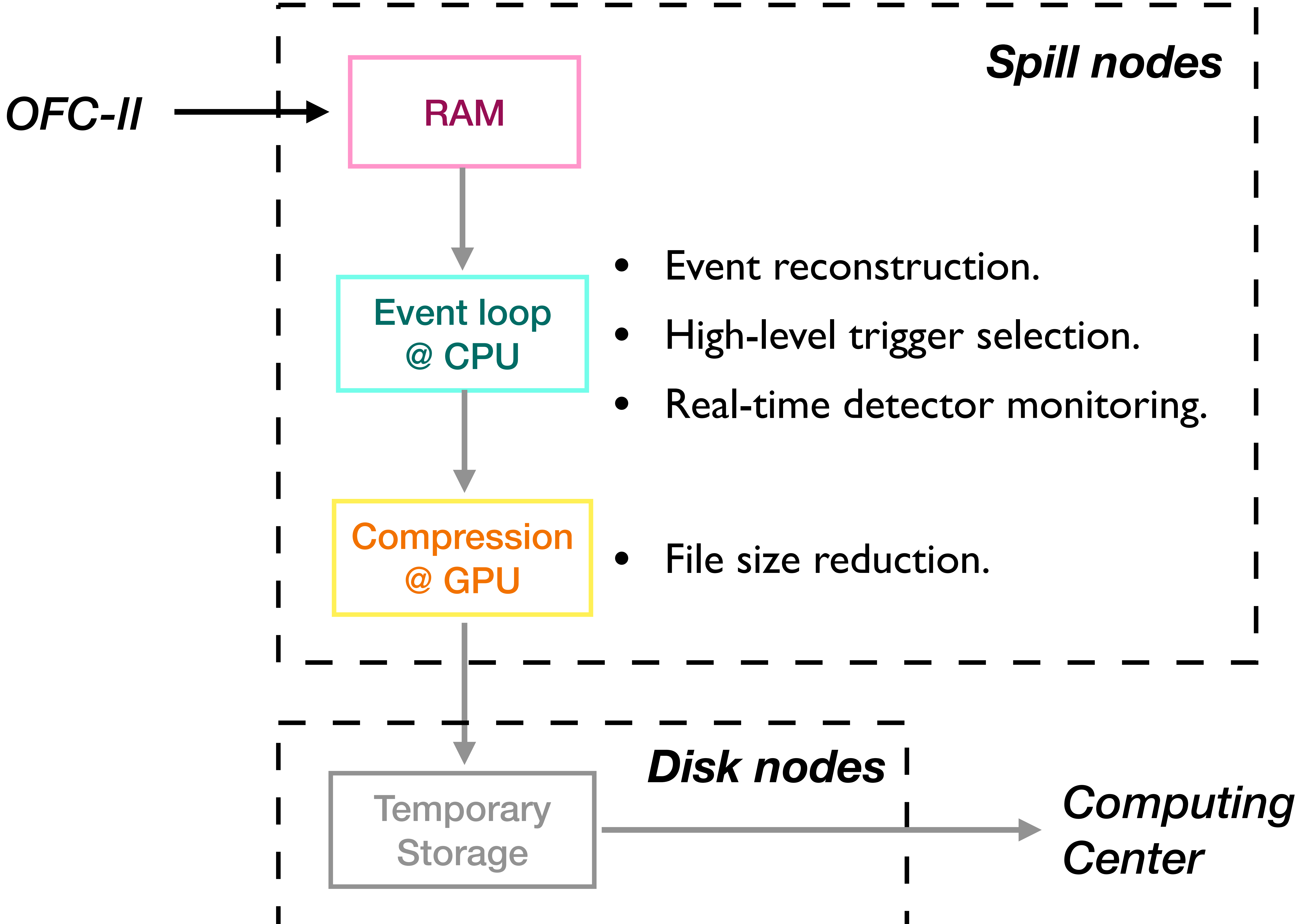


OFC-II

9 QSFPs



GPU-based high-level trigger (HLT)



High-Level Trigger (HLT) Performance

Implemented in spring 2024

Have a large room to be further tightened.

Trigger	HLT-input rate (Spring 2024 physics runs)	Rate after event selection	rate after compression and ped. suppression
$K_L \to \pi^0 \nu \overline{\nu}$	1.5 k/spill	Unchanged	/ 3.2
$K_L \to 3\pi^0$ (6 clus.)	2.0 k/spill	Unchanged	/ 5.3
$K^+ \to \pi^+ \pi^0$	5.7 k/spill	/ 1.25	/ 5.4
$K_L \to 3\pi^0$ (5 clus.)	4.2 k/spill	/ 1.30	/ 5.3
$K_L \to \pi^0 e^+ e^-$	2.4 k/spill	/ 1.20	/ 5.3
Others	1.9 k/spill	Unchanged	/ 4.1
Total	**17.7 k/spill (20.0 Gbps)**	**17.2 Gbps**	**3.6 Gbps**

(Average over 4.2-sec spill)

[Table courtesy of M. Gonzalez (ICHEP 2024)]

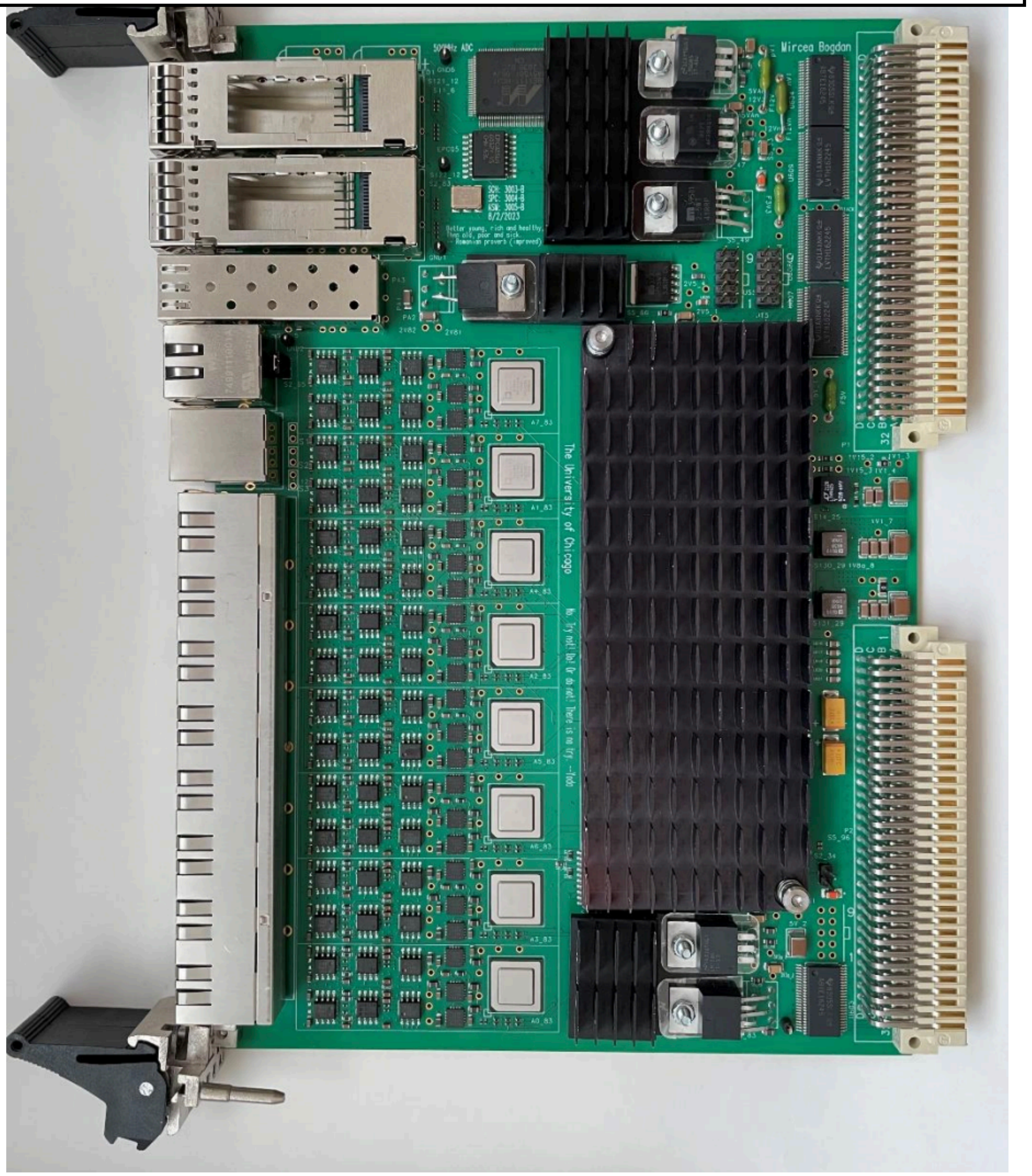
KOTO-II DAQ

Prototype of the KOTO-II ADC

A preliminary thought of the KOTO-II DAQ is to simply expand the KOTO DAQ architecture.

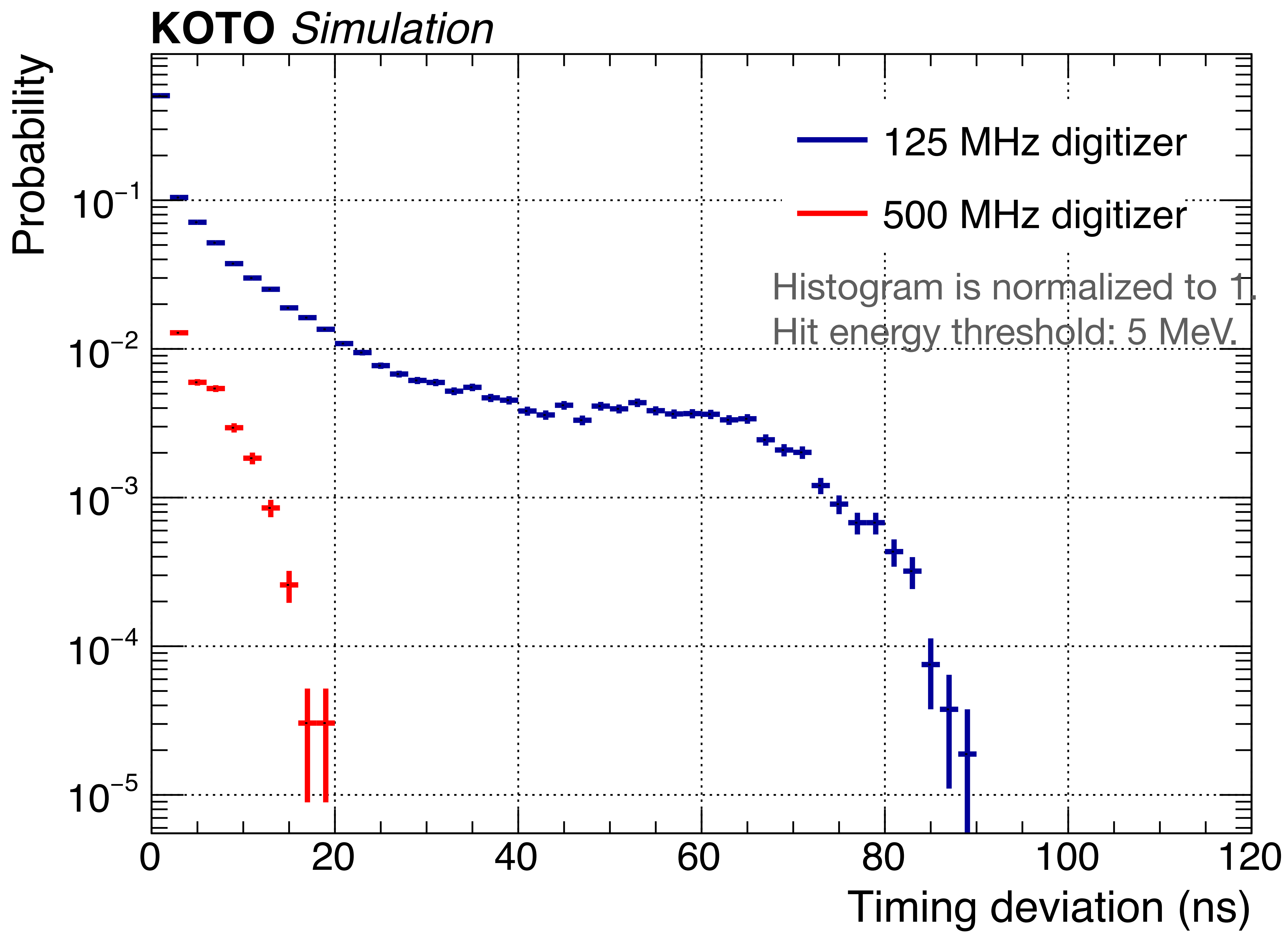
	KOTO		KOTO-II (R&D)
Digitization frequency & dynamic range	125-MHz & 14-bit (majority) 500-MHz & 12-bit		500-MHz & 14-bit
FPGA	Stratix II (Depth = 5.2 μs)	**> x 2** →	Arria V (Depth > 10 μs is expected)
Optical links	2 x 2 Gbps (2 SFP)	**x 9** →	9 x 4 Gbps (2 QSFP + SFP)
#analog inputs	16 channels		

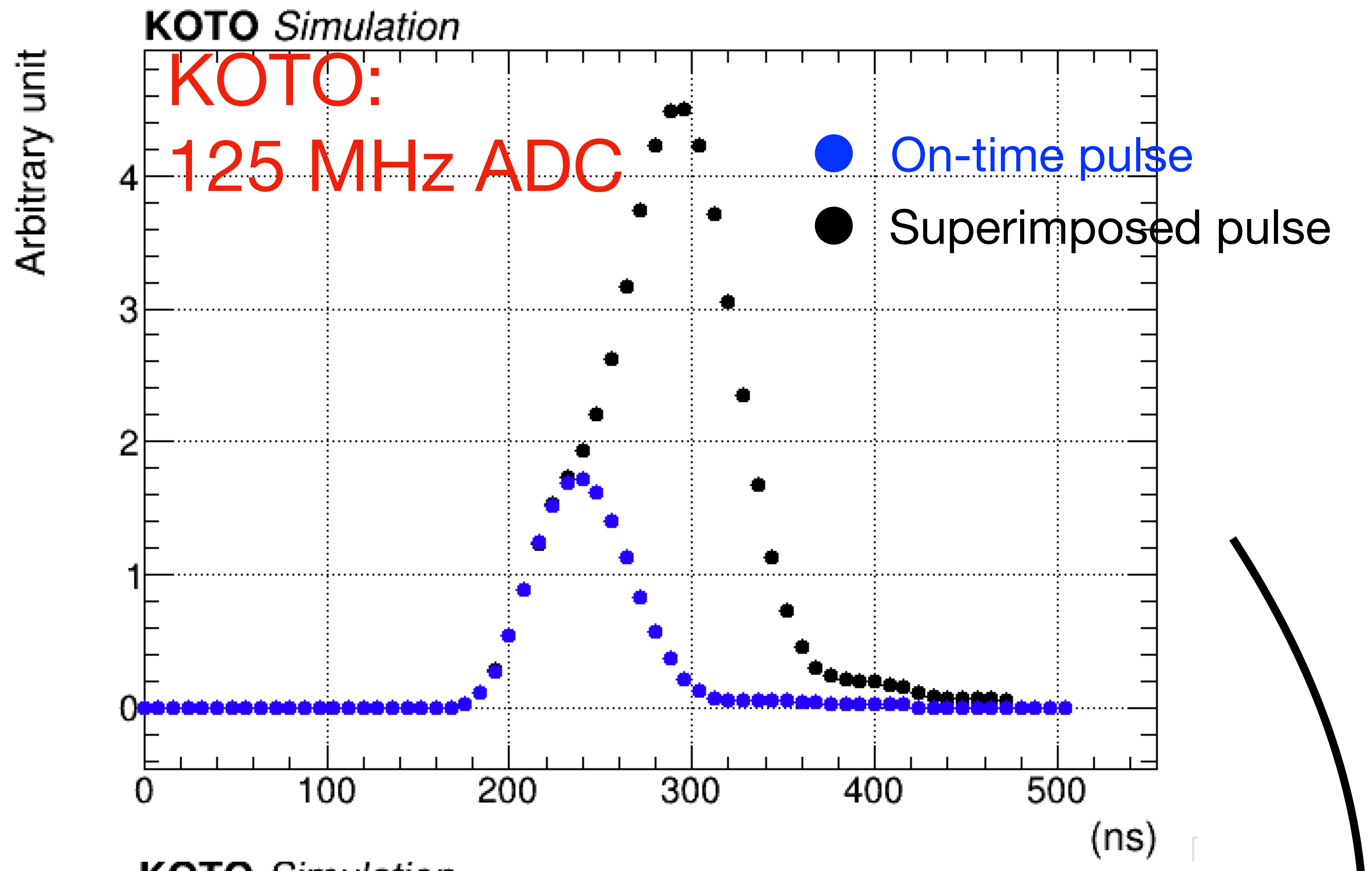
Prototype KOTO-II ADC (R&D at U-Chicago)

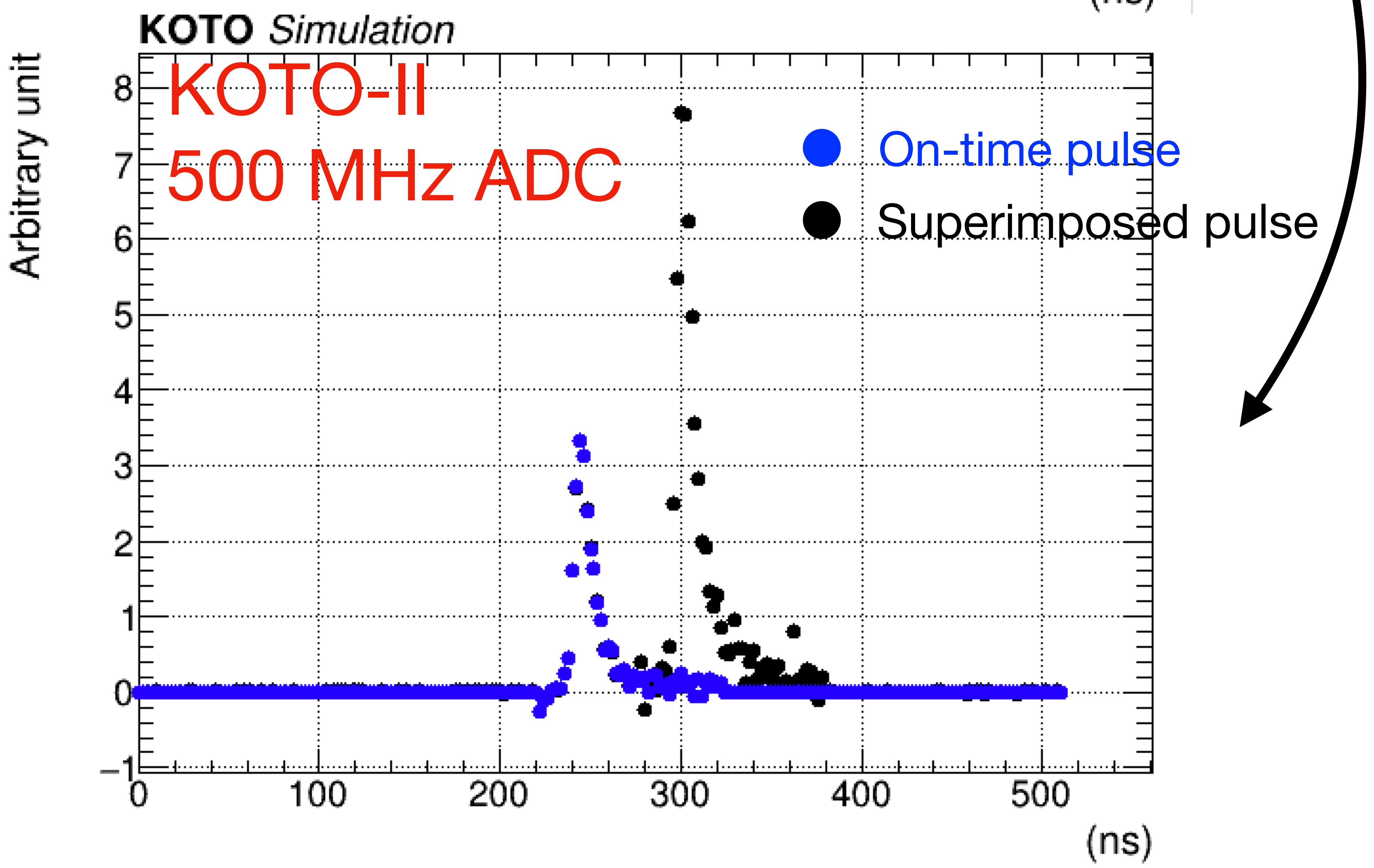


Better pulse separation in KOTO-II

The pulse shaper was introduced for the KOTO 125-MHz ADC boards in order to measure the timing.







Narrow pulses separate the two near hits.

Summary

- The KOTO experiment adopts the pipeline design to accurately determine the triggers.
  - The loss of <2% at 17.7k events/(spill-on = 2 sec) was achieved in spring 2024 (80kW beam).
- The 500-MHz ADC boards are vital to have a better pulse separation.