

#### SERVICES

# Smash HDL bugs on the fly!



#### What added value we can bring to you

We help leading-edge teams write bug-free VHDL and Verilog code.

By automating deep code checks on commits and pull requests.



# Why you should use our approach and tooling

Write bug-free, secure and highly maintainable code

Comply with standards

Reduce hardware development costs

Improve productivity and reduce time to market

Cut down technical debt

Attract and keep top-level designers



# Linty for everyone

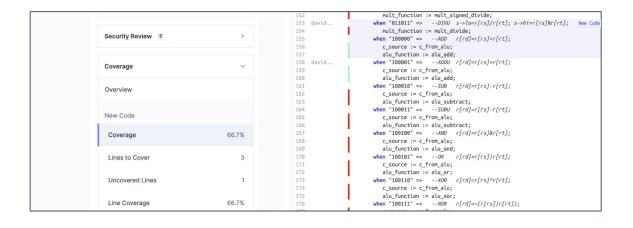
- Manager and Team Leader
  - Keep your developers happy
  - Rework less, innovate more
  - Minimize risks, maximize reputation
  - Gated quality
  - Configure rules
  - Set requirements
  - Define quality gate
  - Monitor Technical Debt

✓ Passed	New Code Overall Code					
	Security	Reliability		Maintainability		
r=¢.	2 Open issues A 2 H 0 M 0 L	80 Open issues	E 3 M OL	1.1k Open issues		
	Accepted issues	3	Coverage			
Enjoy your sparkling clean code!	Valid issues that were not fixed		On <b>O</b> lines to cover.			
	Duplications 3.1% on 4k lines.	۲	Security Hotspots	a		
	ACTIVITY					
	Issues v 1.2k 1k			— Issues 🗌 New Cod		
	800 600 400 200					
	o August september october	mber mber	2024	warch April Way		



## Linty for everyone

- Architect and Senior Designer
  - Protection of the main branch
  - CI/CD pipeline under GitHub, GitLab
  - MR/PR decoration
  - Peer reviews assistant
  - Safety-critical standards evidences (DO254, IEC61508,...)
  - Code coverage "on new code"



	sonarqube-linty-cloud bot commented on Sep 20, 2023 • edited 👻		•••							
	Quality Gate failed									
	Failed conditions									
	<u>3 New Bugs</u> (required ≤ 0)									
	See analysis details on SonarQube									
	$^{\mathbb{Q}}$ Catch issues before they fail your Quality Gate with our IDE extension $^{\Theta}$ SonarLint									
	$\odot$									
	x S racodond deleted a comment from sonarqube-linty-cloud bot on Sep 25, 2023									
,	Add more commits by pushing to the <b>feature/lets_dream</b> branch on Linty-Services/bugfinder-sample.									
> ئ	Approval not required This pull request may be merged without approvals. Learn more about pull request reviews.	Show all r	eviewers							
	A 1 pending reviewer		~							
	All checks have failed 3 failing checks	Hide a	II checks							
	× ( Linty / Linty (pull_request) Failing after 1m	Required	Details							
	× 💽 Linty / Linty (push) Failing after 1m	Required	Details							
	× SonarQube Code Analysis Failing after 23s — Quality Gate failed		Details							
	O Required statuses must pass before merging All required statuses and check runs on this pull request must run successfully to enable automatic mer	ging.								
	Merge without waiting for requirements to be met (bypass branch protections)									
	Merge pull request   You can also open this in GitHub Desktop or view command line instructions.									

## Linty for everyone

- Designers
  - Discover issues from the moment you write code
  - $\circ$  +220 HDL checks in real-time
  - CDC, RDC, FSM graphs
  - Navigation / Auto-completion
  - $\circ$  Code colorisation

	•	$\leftarrow \rightarrow$ (		, <sup>⊖</sup> plasma			
Ф	EXPLORER ···	Preview clock_domain_crossings.md	≣ ddr_ctrl.vhd 9+ ×		™ Preview: 'cdc_9.dot' ×		
	✓ PLASMA	$\equiv$ ddr_ctrl.vhd > $\bigcirc$ logic (ddr_ctrl) > $\bigcirc$	ddr_proc		🖺 ひ 🔎 Search	Aa ∎* ††‡ Bidirectional ∨ Do	ot ~
D	finite_state_mach	252 if command = COMMAND_ 253 refresh_cnt <= ZEF					
9	index.md .scannerwork			THE REAL PROPERTY.			
	✓ .scannerwork	<pre>255 refresh_cnt &lt;= ref 256 end if;</pre>	resh_cnt + 1;				
>	∽ .vscode	257 258 state_prev <= state_c	surrent				
	<ul> <li>{} settings.json</li> <li>≣ alu.vhd</li> </ul>						
כ	≡ bus_mux.vhd			Contraction of the second seco			
¥	≣ cache.vhd	262        rising_edge(clk_2x) dc           263         if reset_in = '1' then		TEXT Transmo TEXT Transmo TEXT Transmo		CDC #9	
ור	≣ code.txt ≣ control.vhd	264 cycle_count <= "000";		And	807 (19713) ++ + u)_d(c.ceaet_in)	- ANET - CLK - SALET - D	¥2_668.03404_604013
l I		265     elsif rising_edge(clk_2)       266    Cycle_count		AND A CONTRACTOR	(10)	ANT CLR 63561 0 ul.ddr.cpile.const	
	≣ eth_dma.vhd ≣ hierarchv.vs	267     if (command = COMMAND       268     cycle_count <= "00	_READ or command = COMMAND_WRI	E) and	0340		
	M makefile	269 elsif cycle_count /=	"111" then	Steller			
	≣ mem_ctrl.vhd	270         cycle_count <= cyc           271         end if;	:le_count + 1;				
	E mlite_cpu.vhd E mlite_pack.vhd	272 273clk_p <= clk;earl		Berlinen and and a second and a			
	≡ milte_pack.vnu ≣ mult.vhd	274		Avera * Sour			
	≣ pc_next.vhd	275        Read data (DLL disa           276         if cycle_count = "100"					

••	•	$\leftarrow$ $ ightarrow$ $ ho$ plasma
Ð	EXPLORER ····	≣ ddr_ctrl.vhd 9+ ×
_	$\sim$ PLASMA	≣ ddr_ctrl.vhd > ⊷ ddr_ctrl > 🖾 SD_UDQS: std_logic
Q	> .linty ∽ .scannerwork	73 SD_CK_N : out std_logic;clock_negative 74 SD_CKE : out std_logic;clock_enable
မို့စ	≣ .sonar_lock ∨ .vscode	75 76 SD_BA : out std_logic_vector(1 downto 0);bank_address 77 SD_A : out std_logic_vector(12 downto 0);address(row or col)
å	{} settings.json ≣ alu.vhd	78 SD_CS : out std_logic;row_address_stroke
₿	≣ bus_mux.vhd ≣ cache.vhd	80     SD_CAS : out std_logic;column_address_strobe       81     SD_WE : out std_logic;write_enable       82
Ň	≡ code.txt ≣ control.vhd	83 SD_DQ : inout std_logic_vector(15 downto 0);data 84 SD_UDM : out std_logic;upper_byte_enable
見	E ddr_ctrl.vhd 9+ E eth_dma.vhd I hierarchy.ys M makefile	85     SD_U005     : inout std_logic;    upper_data_strobe       86     SO_LOM     : out std_logic;    low_byte_enable       87     SO_LOS     : inout std_logic);    low_data_strobe       88     end;    entity ddr    entity ddr
	E mem_ctrl.vhd E mlite_cpu.vhd E mlite_pack.vhd	89 architecture logic of ddr_ctrl is 91Commands for bits RAS & CAS & WE
	≣ mult.vhd ≣ pc_next.vhd ≣ pipeline.vhd	93 subtype command_type is std_logic_vector(2 downto 0); 94 constant COMMAND_URR : command_type := "000"; 95 constant COMMAND_AUTO_REFRESH : command_type := "010"; 96 constant COMMAND_PRECHARGE : command_type := "010";
	≣ plasma_3e.vhd ङ plasma_if.ucf इ plasma_if.vhd	97 constant COMMAND_ACTIVE : command_type := "011"; PROBLEMS 22 OUTPUT DEBUG CONSOLE TERMINAL PORTS
	≣ plasma_S3E.npl	<ul> <li>✓ E ddr_ctrl.vhd 22</li> <li>▲ Remove the useless trailing whitespaces at the end of this line. linty(hdl:HDL003) [Ln 27, Col 1]</li> </ul>
	> OUTLINE	▲ [W-303] Symbol 'SD_UDQS' is defined, but its value is never read. V4P VHDL [Ln 85, Col 7]
	> TIMELINE ~ LINTY HDL DESIGNER IS	A [W-303] Symbol 'SD_LDQS' is defined, but its value is never read. V4P VHDL [Ln 87, Col 7]     A [W-303] Symbol 'COMMAND_LMR' is defined, but its value is never read. V4P VHDL [Ln 94, Col 13]



## Linty ROI from our customers

- ROI less than 3 months
- 3 5 hours per designer per week saved
- Improved designer experience
- Maintained stable designs by reducing technical debt
- HDL code quality standardization across the organization
- Reinforceable coding best practices





Smash HDL bugs on the fly!

#### CONTACT US

Sales - Stephen Rimbault CTO - David Racodon CEO - Vincent Louis stephen.rimbault@linty-services.com david.racodon@linty-services.com vincent.louis@linty-services.com

### Useful links

Website: Demo platform: VHDL checks:

Verilog/SystemVerilog checks:

Coverage of DO254 and CNES standards: Documentation/Installation: Merge Request decoration on GitLab: Pull Request decoration on GitHub: Linty HDL Designer for VS Code: https://linty-services.com https://demo.linty-services.com https://vhdl.linty-services.com https://hdl.linty-services.com https://verilog.linty-services.com https://hdl.linty-services.com https://standards.linty-services.com https://doc.linty-services.com https://gitlab-mr.linty-services.com https://github-pr.linty-services.com https://hdl-designer.linty-services.com

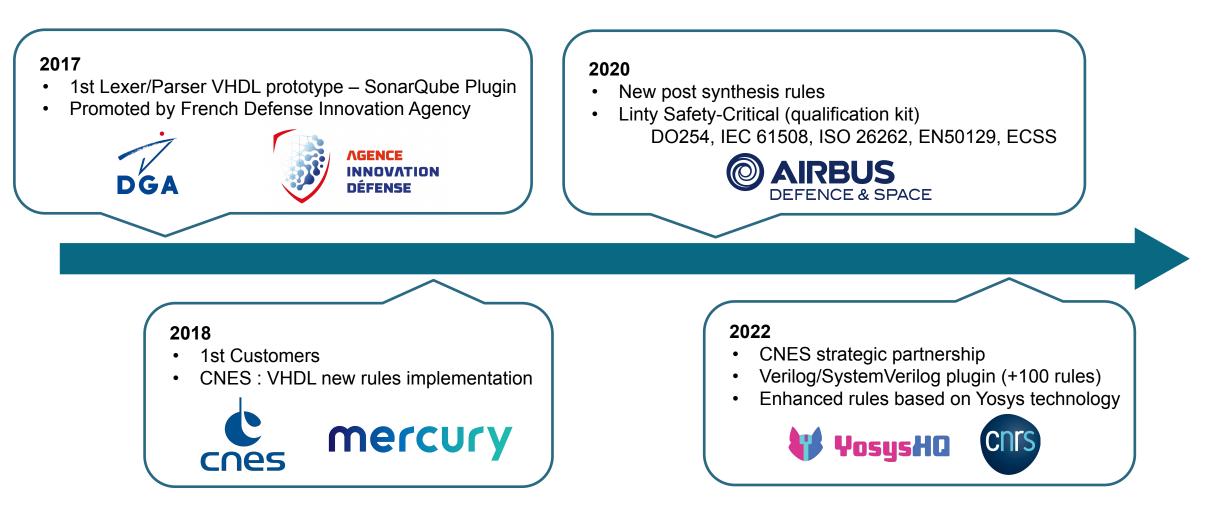


## Linty features

- Easy integration within your continuous integration process (GitHub, GitLab, Bitbucket, etc.)
- Wide range of rules: Conventions, complexity, CDC, FSM and many mores
- Clean as you code with Linty HDL Designer: Powerful VS Code extension
- Cloud platform or on-premise installation
- Automated qualification kit (DO-254, DO-330, IEC 61508, EN 50129, ISO 26262, etc.)
- Focus on new/modified code
- Based on SonarQube, leading platform for continuous code quality control
- Also analyze your C, C++, Python (and many more) code on the same platform



#### Linty Services





## Linty Safety-Critical

Airborne systems:	DO254, DO178C, DO330
Space:	ECSS
Automotive:	ISO26262
Electronic:	IEC 61508
Defense:	Mil-STD-882-E, DGA Technical Note
Naval:	SCAT 12805
Medical:	IEC 62304
Nuclear:	IEC 61513
Railway:	EN5012x

Hardware design audit experience : > 20 years, several hundreds reviews, world wide



## Linty DevOps - Continuous Integration

- Multi-branch analysis Pull request decoration GitLab Bitbucket- GitHub Jenkins
  - You would get the most added value from Linty while it is fully integrated in your DevOps / Continuous Integration process

Add new entities #7

Projects Issues Rules Quality Profiles Quality Gates Administration	다 Open racodond wants to merge 1 commit into master from feature/add_new_e	
☐ GitHub Pull Request ☆ ∦ master -	racodond commented on Oct 5, 2021	ن
Overv Q Search for branches or Pull Requests	No description provided.	
master MAIN BRANCH     Passed	-c- 🛄 Add new entities	✓ b30864e
UAL Pull Requests	sonarqube-linty (bot) commented on Oct 5, 2021	© ···
P <sup>(1)</sup> 7 - feature/add_new_entities Failed Overall Code	Failed	
I feature/add_new_entities	4 New Issues (is greater than 0)	
Manage branches and Pull Requests	Analysis Details	
O jin€ New Bugs	4 Issues	
	• 班0 Bugs	
	• 🔓 O Vulnerabilities	
Multi-branch analysis	• 🕲4 Code Smells	
Multi-branch analysis	Coverage and Duplications	
	<ul> <li>《No coverage information (0.00% Estimated after merge)</li> <li>《No duplication information (0.00% Estimated after merge)</li> </ul>	

Pull request decoration

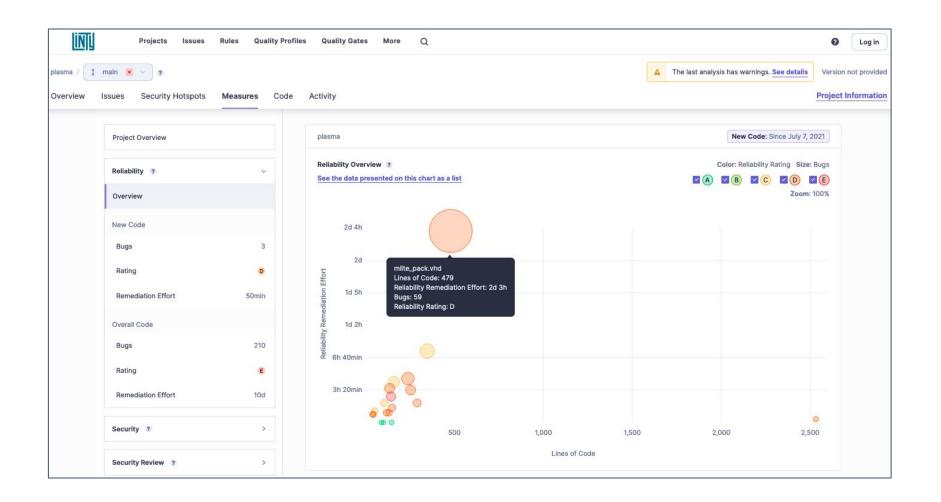


#### Synthetic dashboard

w Issues Security Hotspots Measures Code					
Quality Gate Status ?	Measures				
Conditions on New Code ?	爺 Reliability 3 New Bugs	D	Security     New Vulnerabilities	A	
3 <b>The Bugs</b> is greater than 0	<ul><li>Security Review</li><li>New Security Hotspots ?</li></ul>	A	<ul> <li>Maintainability</li> <li>New Code Smells</li> </ul>	A	
Fix issues before they fail your Quality Gate with <u>SonarLint</u> <del>O</del> in your IDE. Power up with connected mode!	Coverage — Coverage Coverage on <u>O</u> New Lines to cover Estimated after merge		Duplications 0.0% Duplications Duplications on 8 New Lines 0.0% Estimated after merge	۲	



#### Synthetic measures





#### Code coverage on "New code"

<u>lini</u>	Projects Issues Rules	Quality Profiles Qu	uality Gates Administra	ation More Q		0
ModelSim C	Coverage / 🚦 master 🗙 🗸 ?					Version 2
erview I	Issues Security Hotspots M	leasures Code	Activity		Project Settings ~ Project	ect Informati
			146	when otoott		
			146	<pre>mult_function := mult_write_lo; when "011000" =&gt;MULT s-&gt;lo=r[rs]*r[rt]; s-&gt;hi=0;</pre>		
	Project Overview		147	<pre>mult_function := mult_signed_mult;</pre>		
	Project Overview		149	when "011001" =>MULTU s->lo=r[rs]*r[rt]; s->hi=0;		
			150	mult_function := mult_mult;		
			151	when "011010" =>DIV s->lo=r[rs]/r[rt]; s->hi=r[rs]%r[rt];		
	Reliability ?	>	152	<pre>mult_function := mult_signed_divide;</pre>	New Code	
			153 david	when "011011" =>DIVU s->lo=r[rs]/r[rt]; s->hi=r[rs]%r[rt];	Her code	
			154	<pre>mult_function := mult_divide;</pre>		
			155	<pre>when "100000" =&gt;ADD r[rd]=r[rs]+r[rt];</pre>		
	Security ?	>	156	c_source := c_from_alu;		
			157	alu_function := alu_add;		
			158 david	<pre>when "100001" =&gt;ADDU r[rd]=r[rs]+r[rt];</pre>		
			159	<pre>c_source := c_from_alu;</pre>		
	Security Review ?	>	160	alu_function := alu_add;		
			161	<pre>when "100010" =&gt;SUB r[rd]=r[rs]-r[rt];</pre>		
			162	<pre>c_source := c_from_alu;</pre>		
	Maintainability ?	>	163	<pre>alu_function := alu_subtract;</pre>		
	Maintainability	·	164	<pre>when "100011" =&gt;SUBU r[rd]=r[rs]-r[rt];</pre>		
			165	<pre>c_source := c_from_alu;</pre>		
			166	alu_function := alu_subtract;		
	Coverage	~	167	<pre>when "100100" =&gt;AND r[rd]=r[rs]&amp;r[rt];</pre>		
			168	<pre>c_source := c_from_alu;</pre>		
			169	alu_function := alu_and;		
	Overview		170	<pre>when "100101" =&gt;OR r[rd]=r[rs]/r[rt];</pre>		
			171	c_source := c_from_alu;		
			172	alu_function := alu_or;		
	New Code		173	<pre>when "100110" =&gt;XOR r[rd]=r[rs]^r[rt];</pre>		
			174	<pre>c_source := c_from_alu;</pre>		
	0	00.7%	175	alu_function := alu_xor;		
	Coverage	66.7%	176	<pre>when "100111" =&gt;NOR r[rd]=~(r[rs]/r[rt]); c course v= c form alw;</pre>		
			178	c_source := c_from_alu; alu_function := alu_nor;		
	Lines to Cover	3	178	when "101010" =>SLT r[rd]=r[rs] <r[rt];< td=""><td></td><td></td></r[rt];<>		
	Lines to obver	5	180	<pre>c_source := c_from_alu;</pre>		
			180	<pre>alu_function := alu_less_than_signed;</pre>		
	Uncovered Lines	1	181	when "101011" =>SLTU r[rd]=u[rs] <u[rt];< td=""><td></td><td></td></u[rt];<>		
			183	<pre>c_source := c_from_alu;</pre>		
			185	alu_function := alu_less_than;		
	Line Coverage	66.7%	185	when "101101" =>DADDU r[rd]=r[rs]+u[rt];		
			185	c_source := c_from_alu;		
			187	alu_function := alu_add;		
	Conditions to Cover	0	188	when "110001" =>TGEU		



#### Code duplication

Projects Issues	Rules Quality Prof	iles Quality Gates	More Q	0	Log in
na / 🚦 main 🙁 🗸 🤋			The last analysis has warnings. See details	Version	not provided
rview Issues Security Hotspots	Measures Code	Activity		Project I	Information
Project Overview		Duplicated Line	s (%) 10.2%		
Reliability ?	>	1 2 3 4 5	TITLE: Memory Controller AUTHOR: Steve Rhoads (rhoadss@yahoo.com) - DATE CREATED: 1/31/01 FILENAME: men_ctrl.vhd		
Security ?	>	6 7 8 9	PROJECT: Plasma CPU core COYYRIGHT: Software placed into the public domain by the author. Software 'as is' without warranty. Author liable for nothing. DESCRIPTION:		
Security Review ?	>	10 11 12	Memory controller for the Plasma CPU. Supports Big or Little Endian mode.		
Maintainability ?	>	13 14 15 16	library ieee; use ieee.std_logic_1164.all; use work.mlite_pack.all;		
Coverage	>	17 18 <b>Ř</b> 19 <b>Č</b> 20 <b>Č</b>	entity mem_trl is port(clk : in std_logic; reset in : in std_logic; pause in : in std_logic;		
Duplications	~	21 <b>O</b> 22 <b>O</b> 23 <b>O</b> 24	Duplicated By /mlite_pack.vhd Lines: 219 - 238		
Overview		25 🚱 26 🐼 27 🐼	<pre>men_source : in mem_source_type; data write : in std_logic_vector(31 downto 0);</pre>		
New Code		28 衰 <sup>2</sup> 29 衰 <sup>2</sup>	<pre>data_read : out std_logic_vector(31 downto 0); pause_out : out std_logic;</pre>		
Duplicated Lines	0	30 🕹 31 👘 32 👘	address_next : out std_logic_vector(31 downto 2); byte we next : out std_logic_vector(3 downto 0);		
Duplicated Blocks	0	33 34 35 36 $\hat{m}^2$	address : out std_logic_vector(31 downto 2); byte we : out std_logic_vector(3 downto 0); data_w : out std_logic_vector(31 downto 0);		
Overall Code		37 $\Theta^2$ 38 $\Theta^2$	<pre>data r : ist_logic_vector(31 downto 0); end; -entity mem_ctrl</pre>		
Density	10.2%	39 46 🚱	architecture logic of mem_ctrl is "00" = big_endian; "11" = Little_endian		



#### Linty Rules (several hundreds)

- Post-synthesis rules
- Clock Domain Crossing (CDC)
- Finite State Machine (FSM)
- Cyber threats

#### **Coverage of Standards by Linty Rules**

Standard	Number of Rules	Number of Automatable Rules	Overall Coverage of Automatable Rules	Full Coverage	High Coverage	Low Coverage	No Coverage
CNES	73	67	78%	47	5	3	12
CNES CUSTOM	55	43	80%	30	5	1	7
DO-254	49	46	74%	30	2	5	9

