

# Design of an 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS

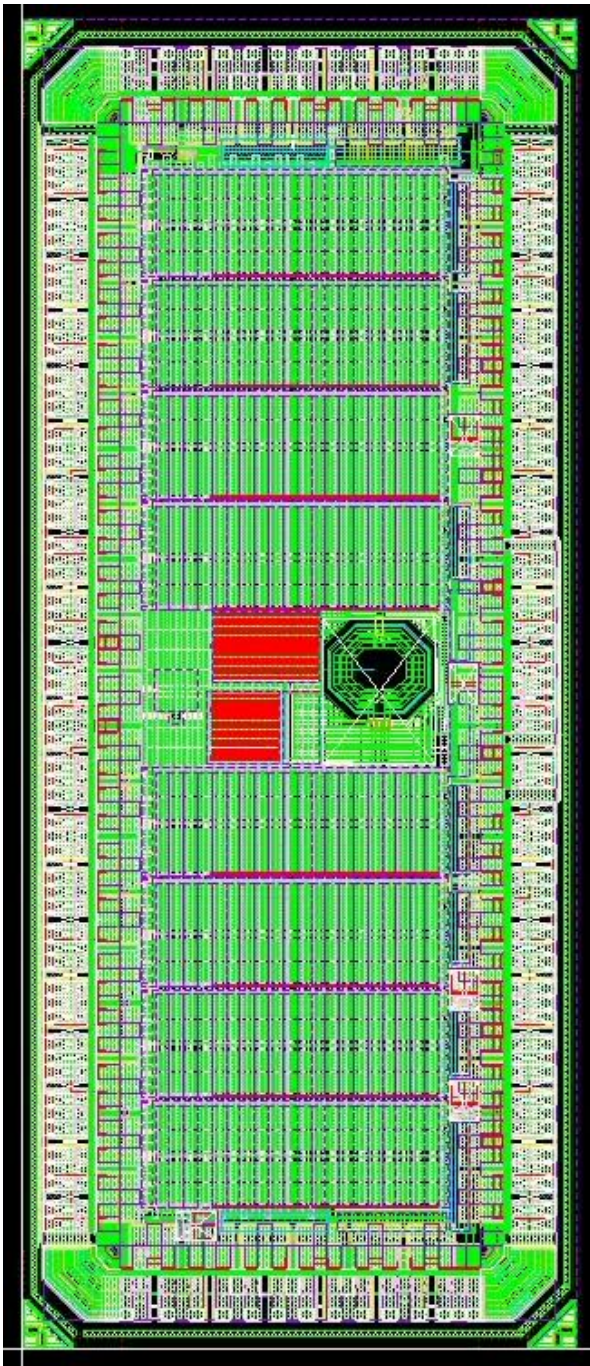
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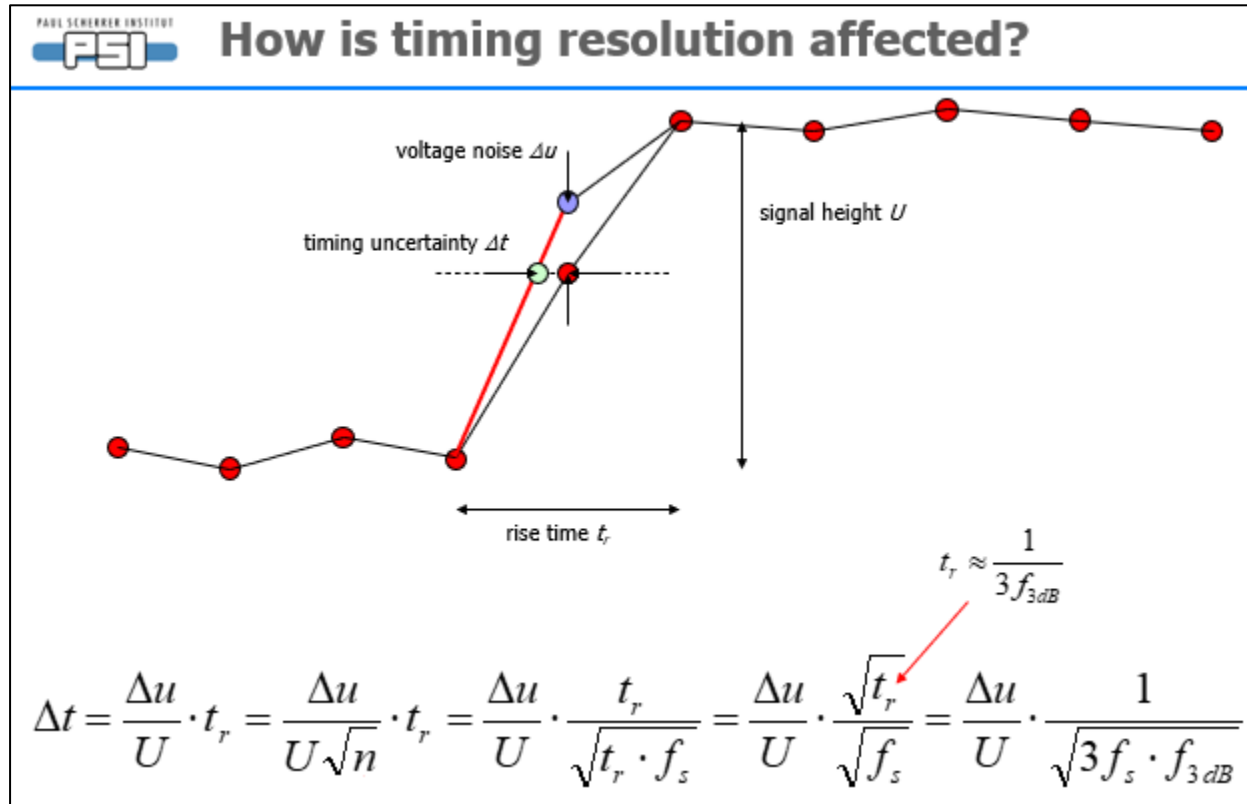
1. Fermi National Accelerator Laboratory 2. University of Chicago 3. Stanford University 4. North Central College



## PSEC5 aims to deliver on a few key features

- Low Power
- Multi-Hit capability
- 40 GS/s Sampling Rate
- 4GHz Analog Bandwidth
- Customizable Buffer Lengths
  - Aims to achieve fast sampling and long analog buffer
- <5ps timing resolution

# Primary goal – picosecond timing resolution



Ref. [1] Stefan Ritt; The role of analog bandwidth and signal-to-noise in timing for waveform digitizing; Timing Workshop, Chicago April 28<sup>th</sup> 2011

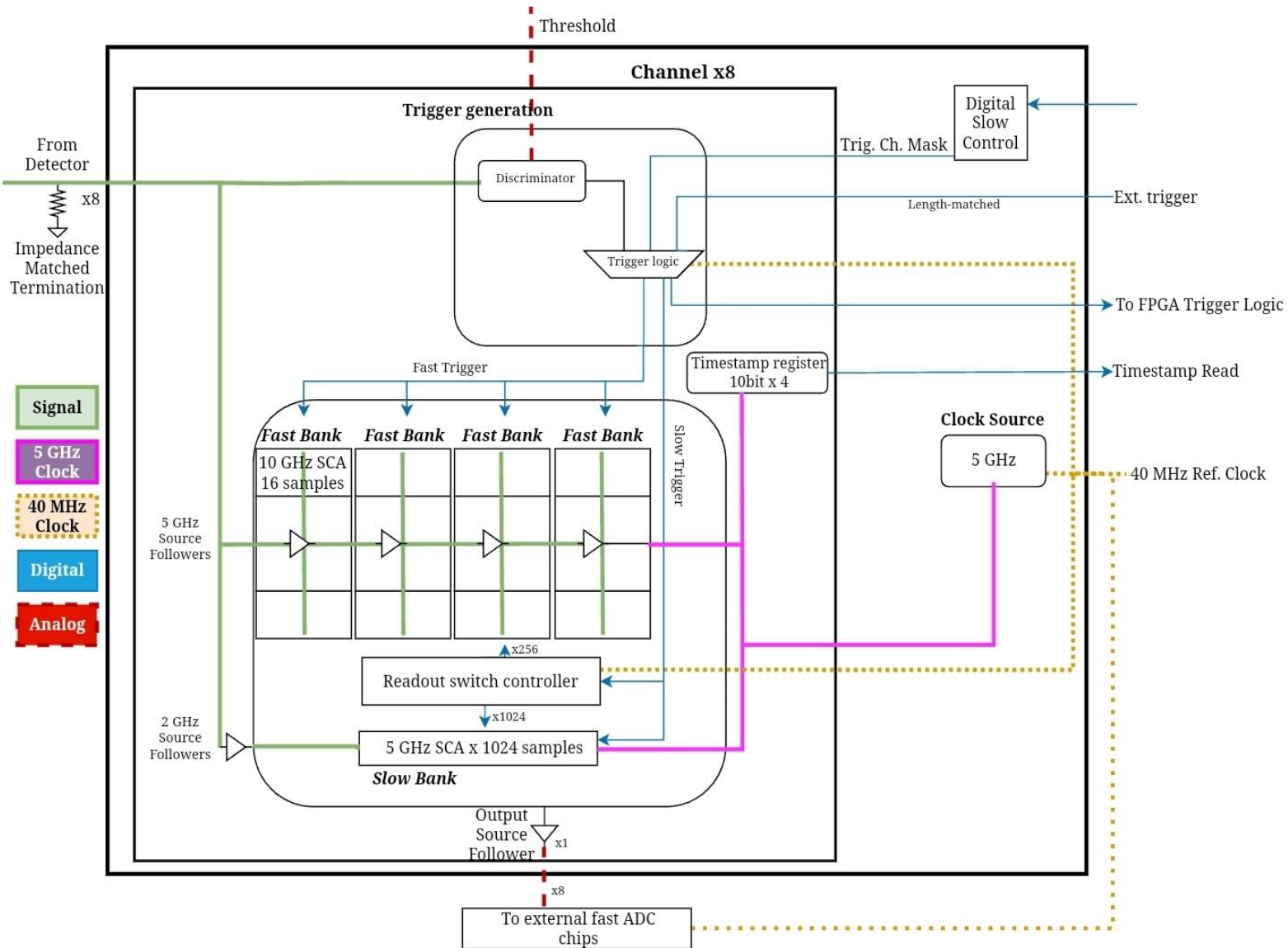
**Therefore, an improved  $\Delta t$  can be achieved by:**

- Low Noise (from samples)
- Minimizing Sampling time jitter
- High Sampling Rate
- High Analog Bandwidth

Where  $f_s$  = Sampling Rate and  $f_{3dB}$  = Bandwidth

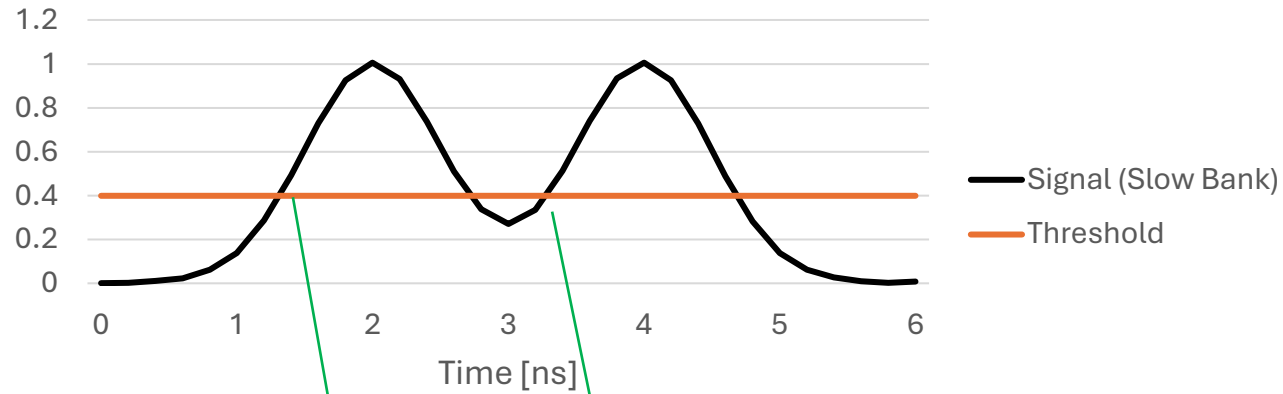
*We intend to deliver a proof of concept at the Fermilab Test Beam Facility (FTBF).*

# PSEC5 Block Diagram and Specs

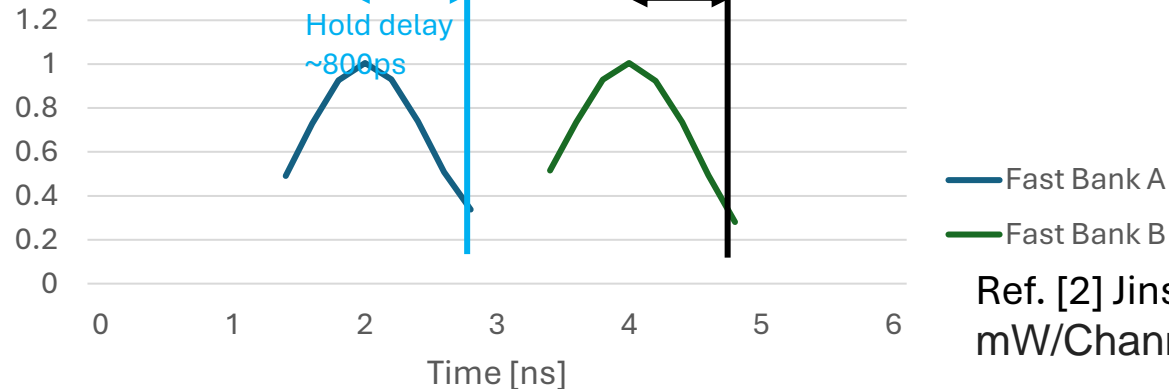
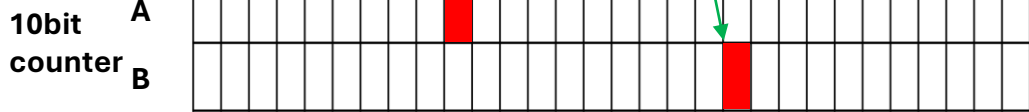


Process	TSMC 65 nm
Dynamic range	10 bits
Sampling Rate	40 GSa/s (5 GSa/s)
Buffer Length	6.4 ns(204.8 ns)
Analog Bandwidth	>4 GHz
Channels/Chip	8
Area	2.4 mm <sup>2</sup>

# Architecture: Fast and Slow SCAs



Propagation delay ~800ps



**A solution to the fast sampling and long analog buffer problem:**

## Fast Banks x4:

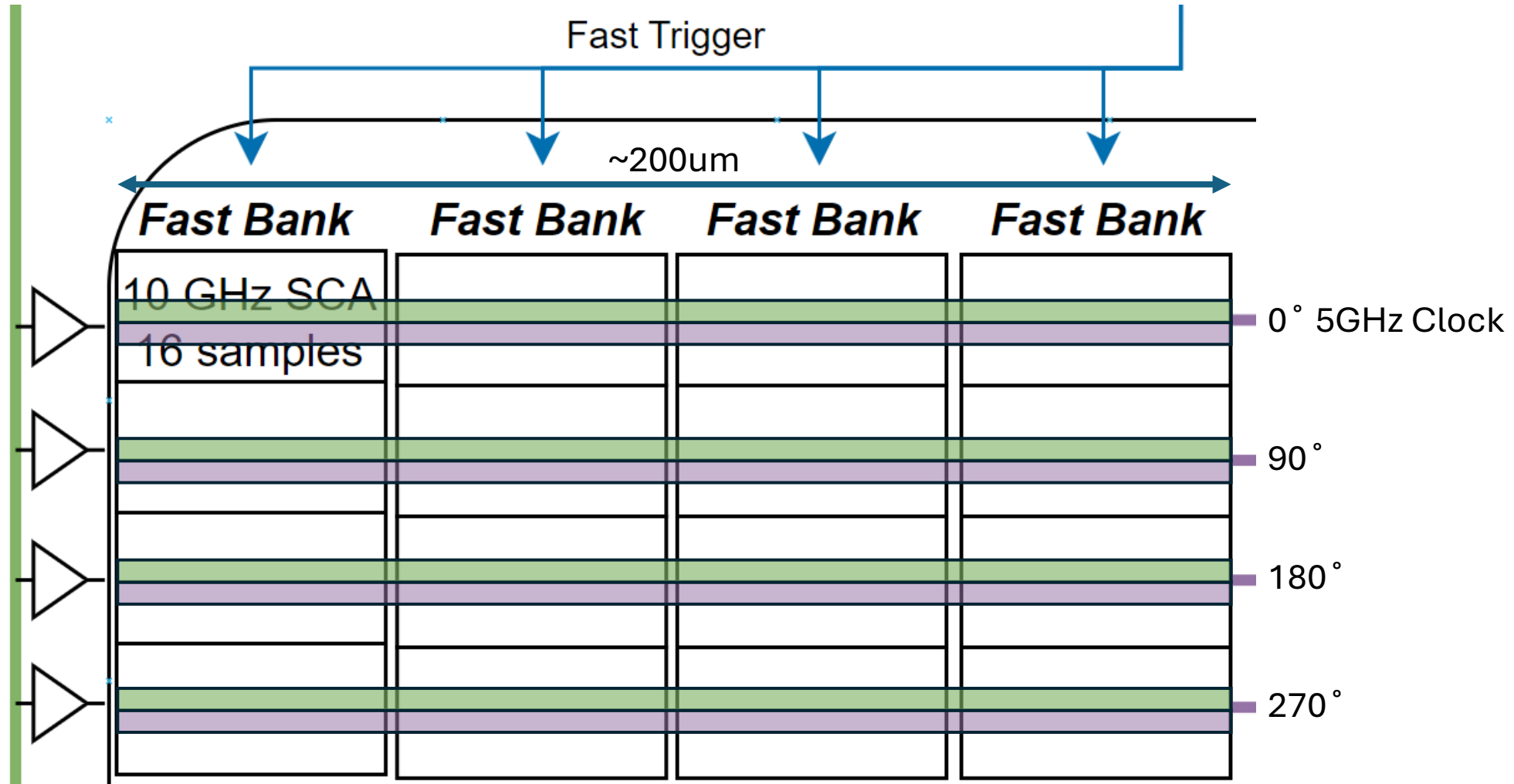
- 64 samples each
- 1.6 ns Buffer length
- Can be configured to run sequentially

## Slow Bank:

- Up to 1024 samples
- 204.8 ns Buffer length
- Captures the entire signal.

Ref. [2] Jinseo Park, Design of an 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS, *PM 2024*

# Fast Bank structure

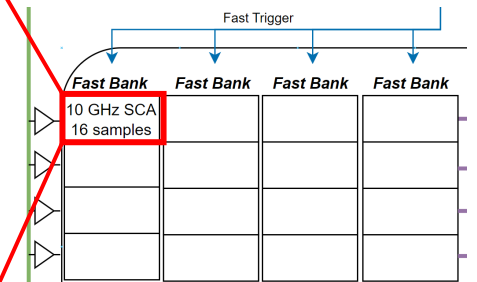


Ref. [2] Jinseo Park, Design of an 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS, *PM 2024*

# Single Column Layout

Size:  $45\mu\text{m} \times 25\mu\text{m}$

Capacitors: 35fF



Sampling Switch  
2.5V NMOS  
Size:  $4\mu\text{m} \times 280\text{nm}$

Ref. [2] Jinseo Park, Design of an 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS, *PM 2024*

# Sampling Switch – why NMOS-2.5v?

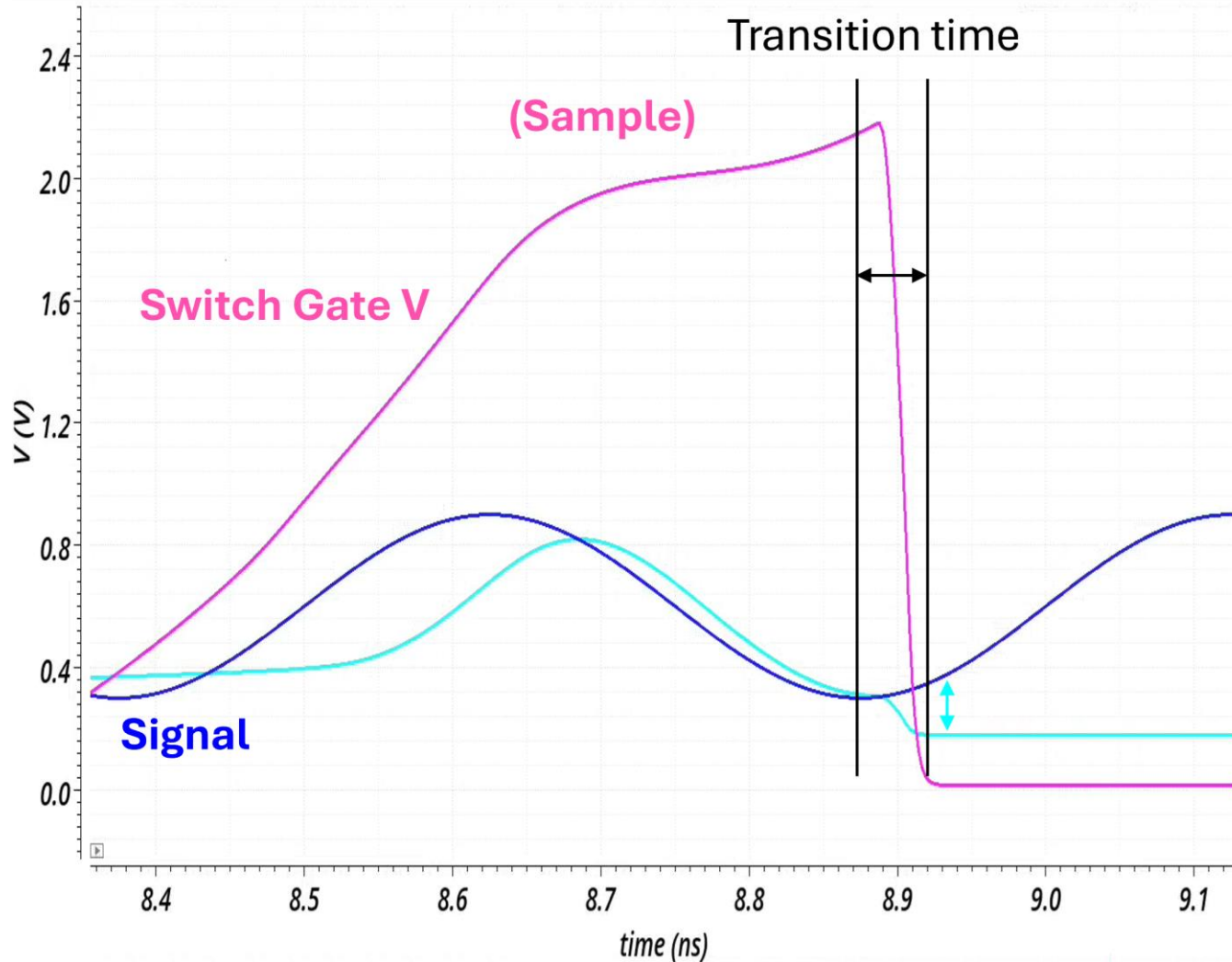
	CMOS	CMOS-2.5 V	CMOS-lvt	NMOS	NMOS-2.5v	NMOS-lvt	NMOS-hvt
V Range	1.2 V	2.5 V	1.2 V	<1.2 V*	<2.5 V*	<1.2 V*	<1.2 V*
Cutoff Freq**	0.6 GHz	3.4 GHz	2.3 GHz	1 GHz	6 GHz	3.4 GHz	<0.1 GHz
Length	60 nm	280 nm	60 nm	60 nm	280 nm	60 nm	60 nm
Hold Time****	68 ns	>10 $\mu$ s	1.7 ns	71 ns	>20 $\mu$ s	2.6 ns	2 $\mu$ s

\*Higher impedance as the signal voltage reaches vdd, noticeable at  $V > 0.6v_{dd}$

\*\* $(\text{Capacitor V Amplitude} / \text{Signal V Amplitude})$  reaches 0.7. ss corner, 0.1 V amplitude, DC bias =  $0.5v_{dd}$

\*\*\*\*ff corner, 10% decay after sampling vdd.

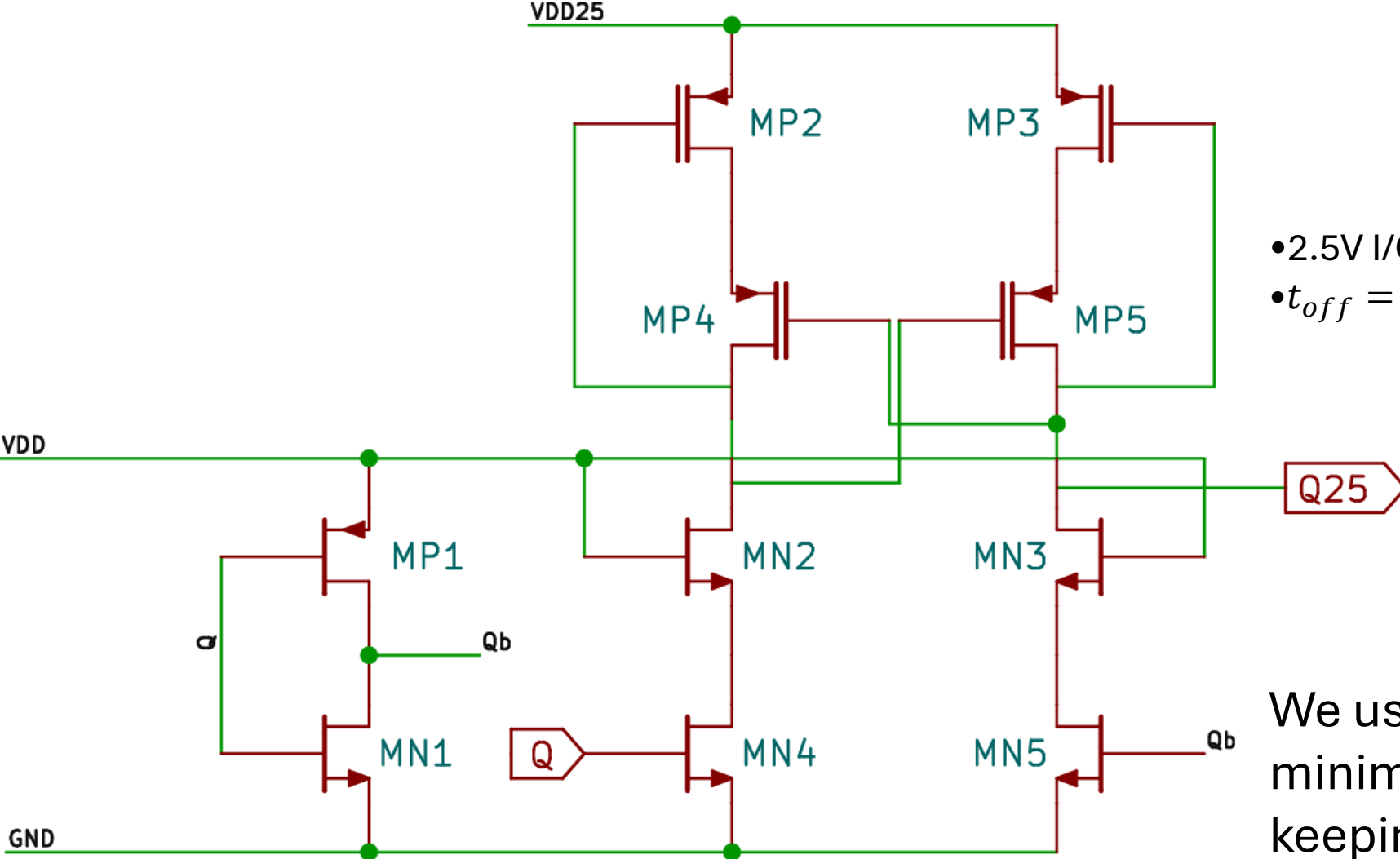
# Switching Drift – Justifying an NMOS sampling switch



- The value of a capacitor **drifts while it switches off** from the signal line.
- Drift consists of **switch gate charge injection**, which is a fixed value and is calibratable, and **resistive drift**, which is dependent on signal V.
- It is essential to keep the **[Sample → Hold]** transition time low.

→ **NMOS instead of CMOS for the sampling switch!**

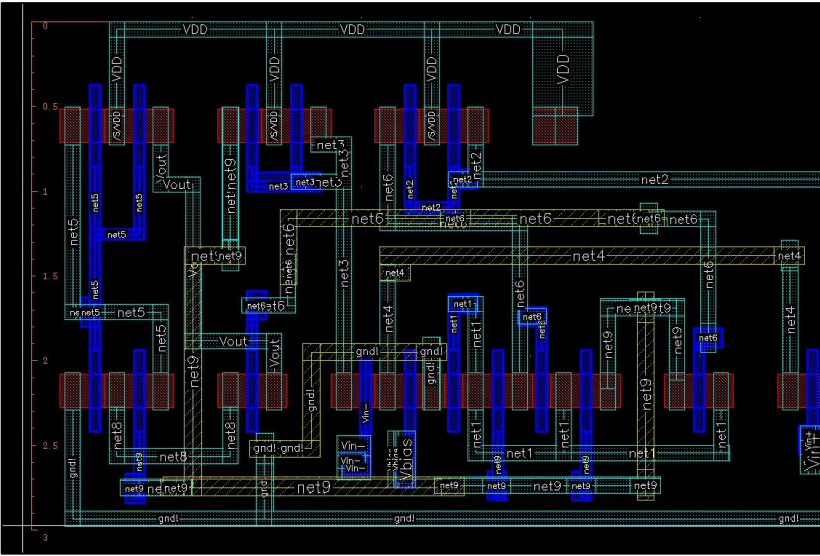
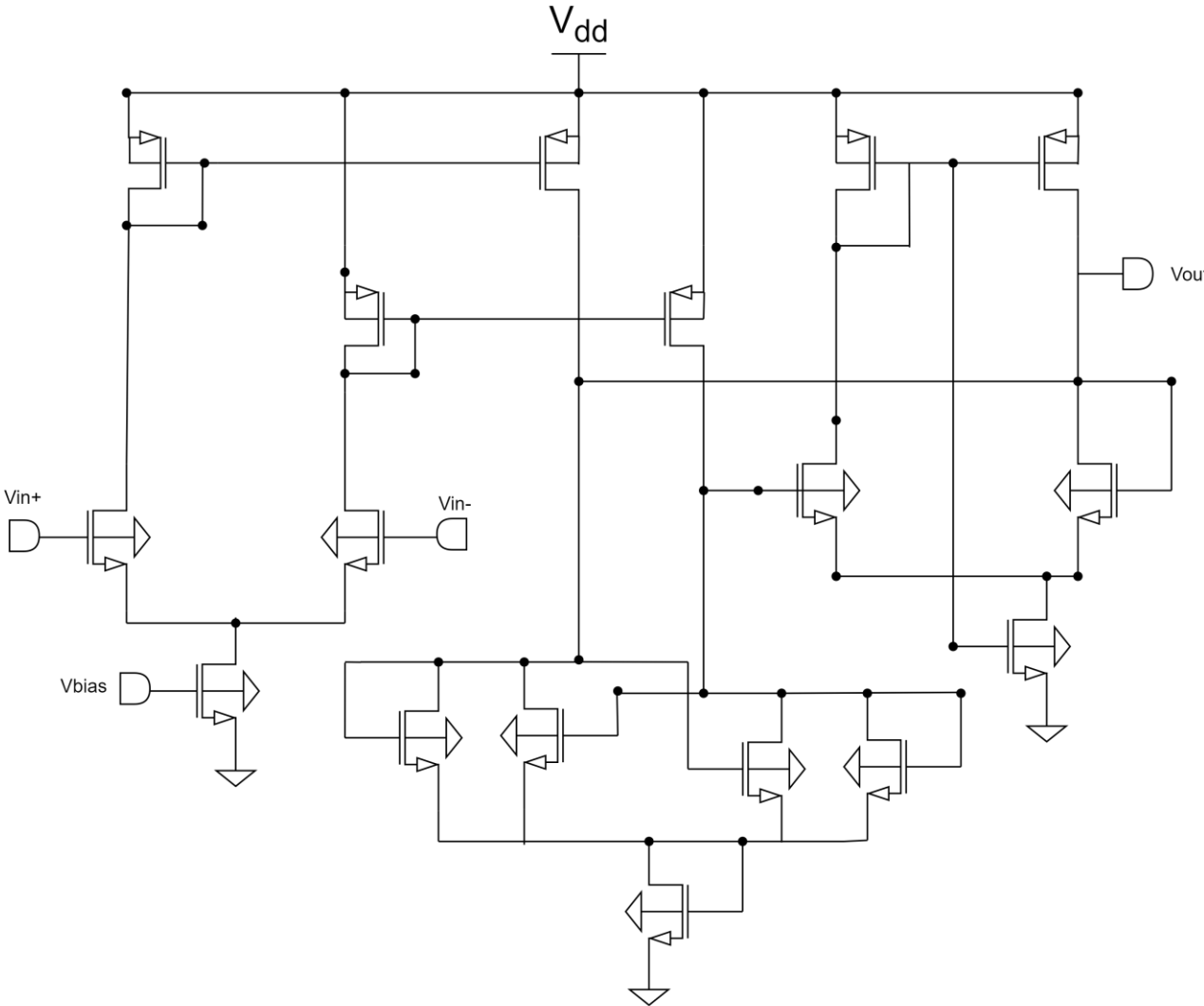
# Minimizing Sampling Switch Resistance



- 2.5V I/O nMOS vs 1.2V core device
- $t_{off} = 15\text{ps (BC)} - 22\text{ps (WC)}$

We use a voltage level shifter to minimize switch resistance while keeping its gate voltage high.

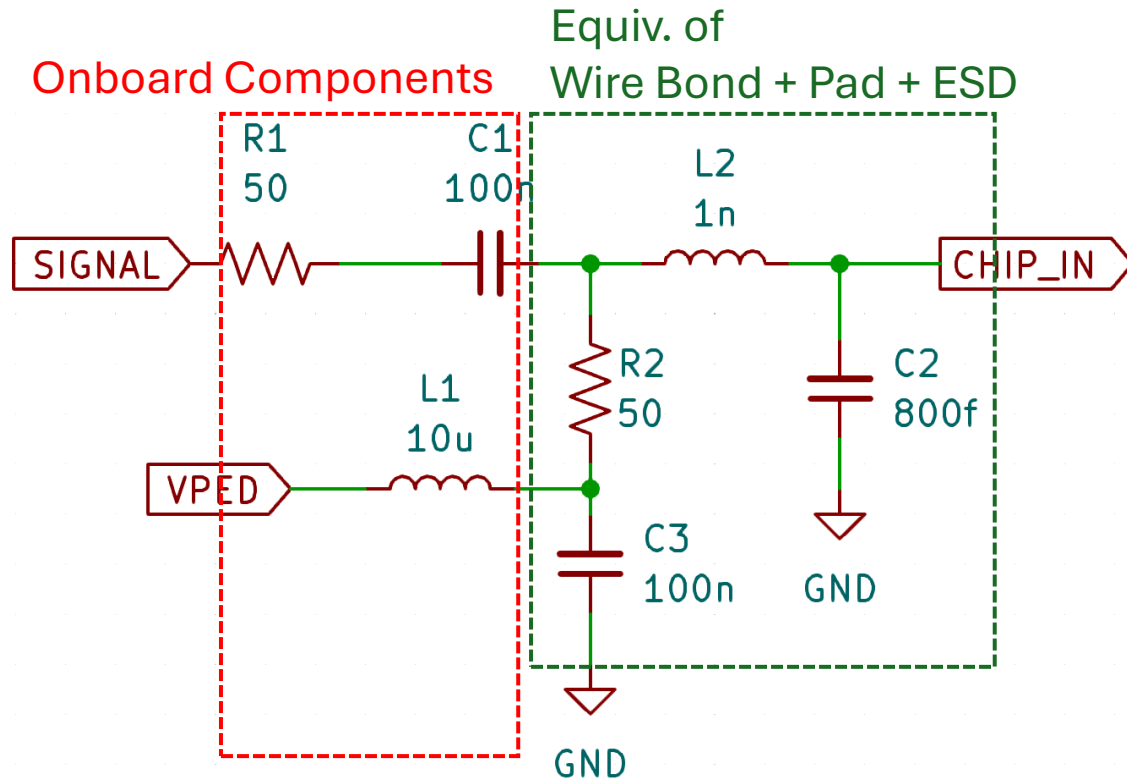
# Discriminator – Triggering for the Fast SCA Banks



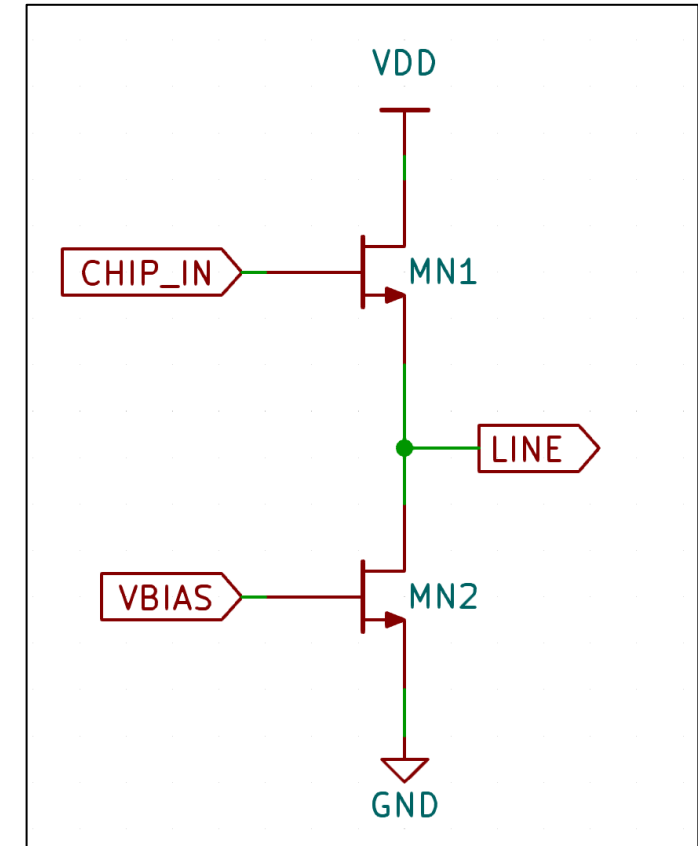
Rising-edge delay is a consistent ~180 ps with <15 ps spread, while falling-edge delay improves from ~310 ps down to ~165 ps as Vped rises, also with ≤15 ps variation

**One discriminator per channel – flips to trigger fast SCA bank**

# Main Signal Path Bandwidth



- $C1$ ,  $C3$ ,  $R2$ ,  $L1$  are components placed on board for capacitive coupling.  $L2$  and  $C2$  are the parasitic inductance and the capacitance of the wire bond and ESD combined
- Pedestal Voltages are controlled by the FPGA



Input Source Follower

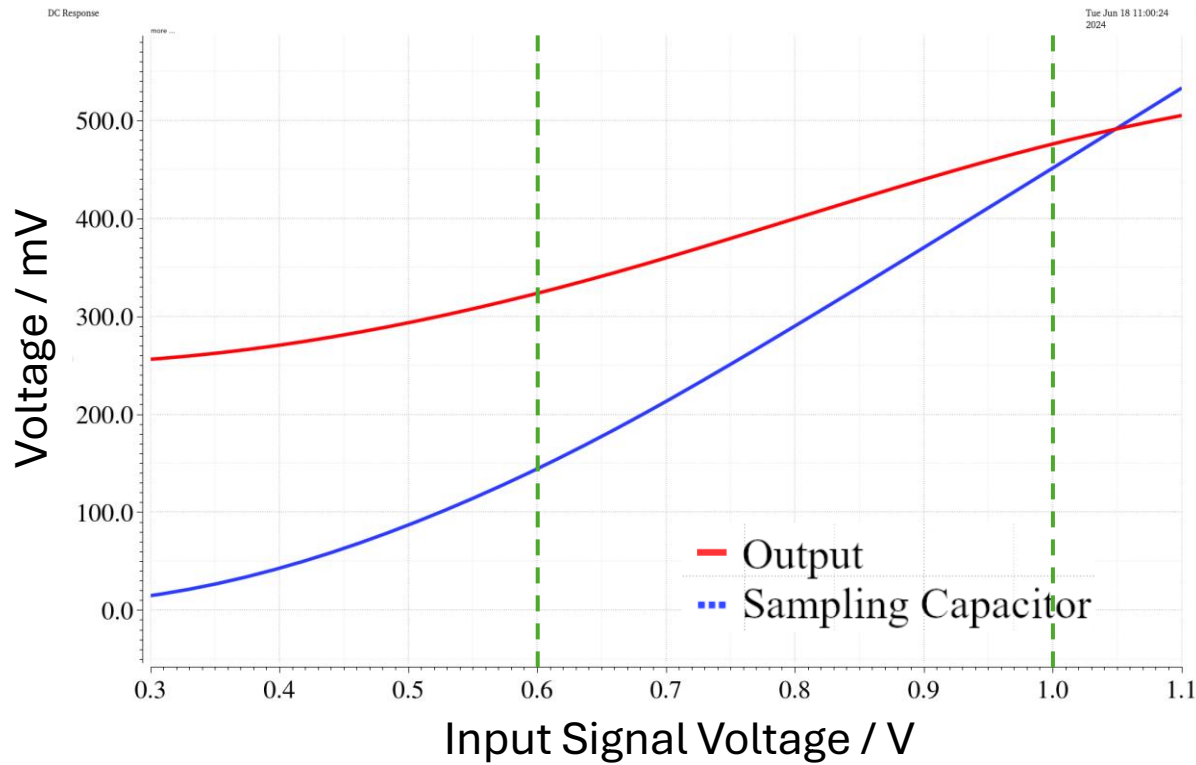
## Key Specs:

- Source Follower Bandwidth 5 GHz
- **Wire-bond Bandwidth 4 GHz**
- Slow Bank Bandwidth 2 GHz

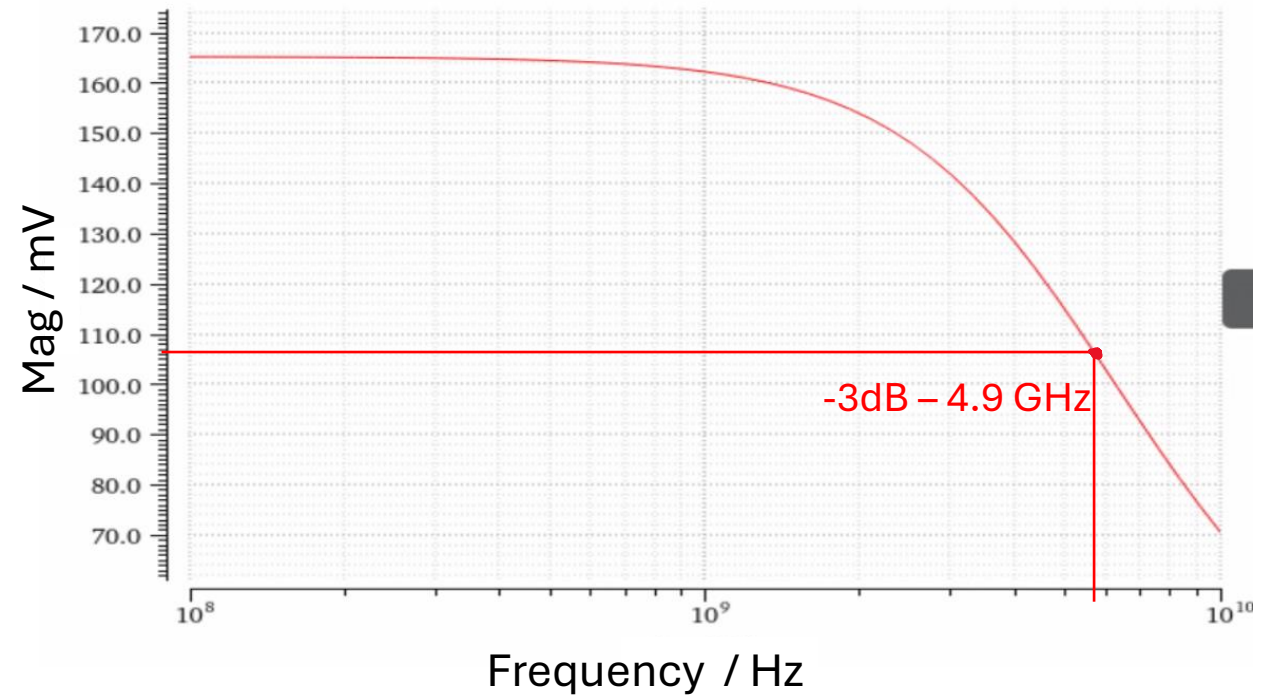
**Overall bandwidth constrained by Wire-bonding: 4 GHz**

# Signal Path performance

## Voltage Linearity Plot

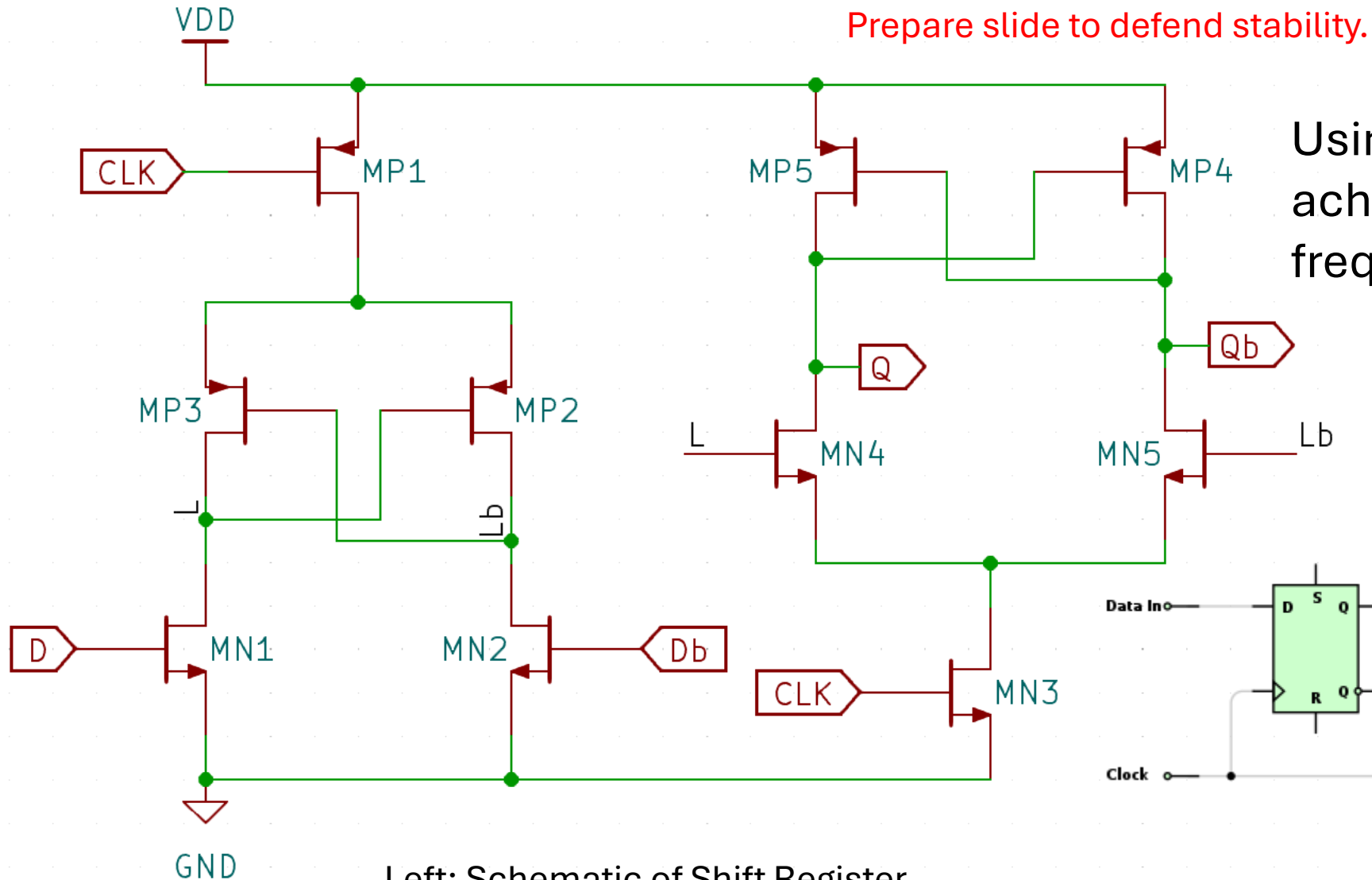


## AC Sweep (100 MHz – 10 GHz) – Input Buffer

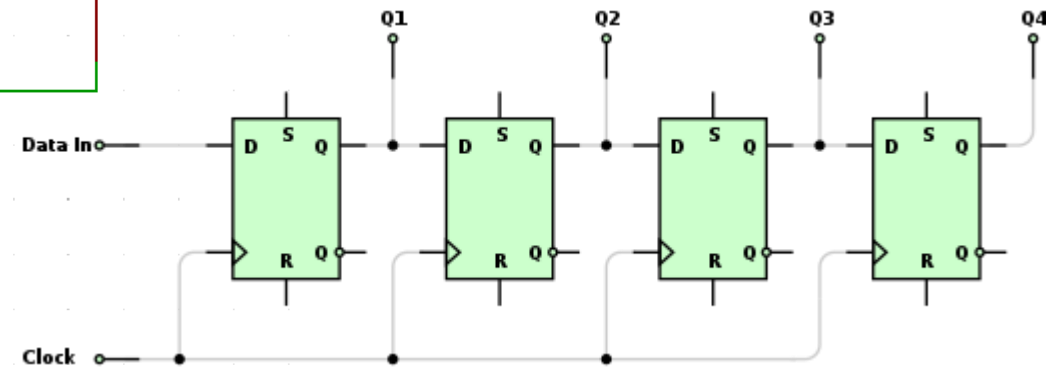


**Buffer Achieves 4.9 GHz input bandwidth**

# Reducing Clock Power: 40GS/s without 10GHz clk



Using both clock edges, we can achieve 10 GS/s with half the frequency



Left: Schematic of Shift Register

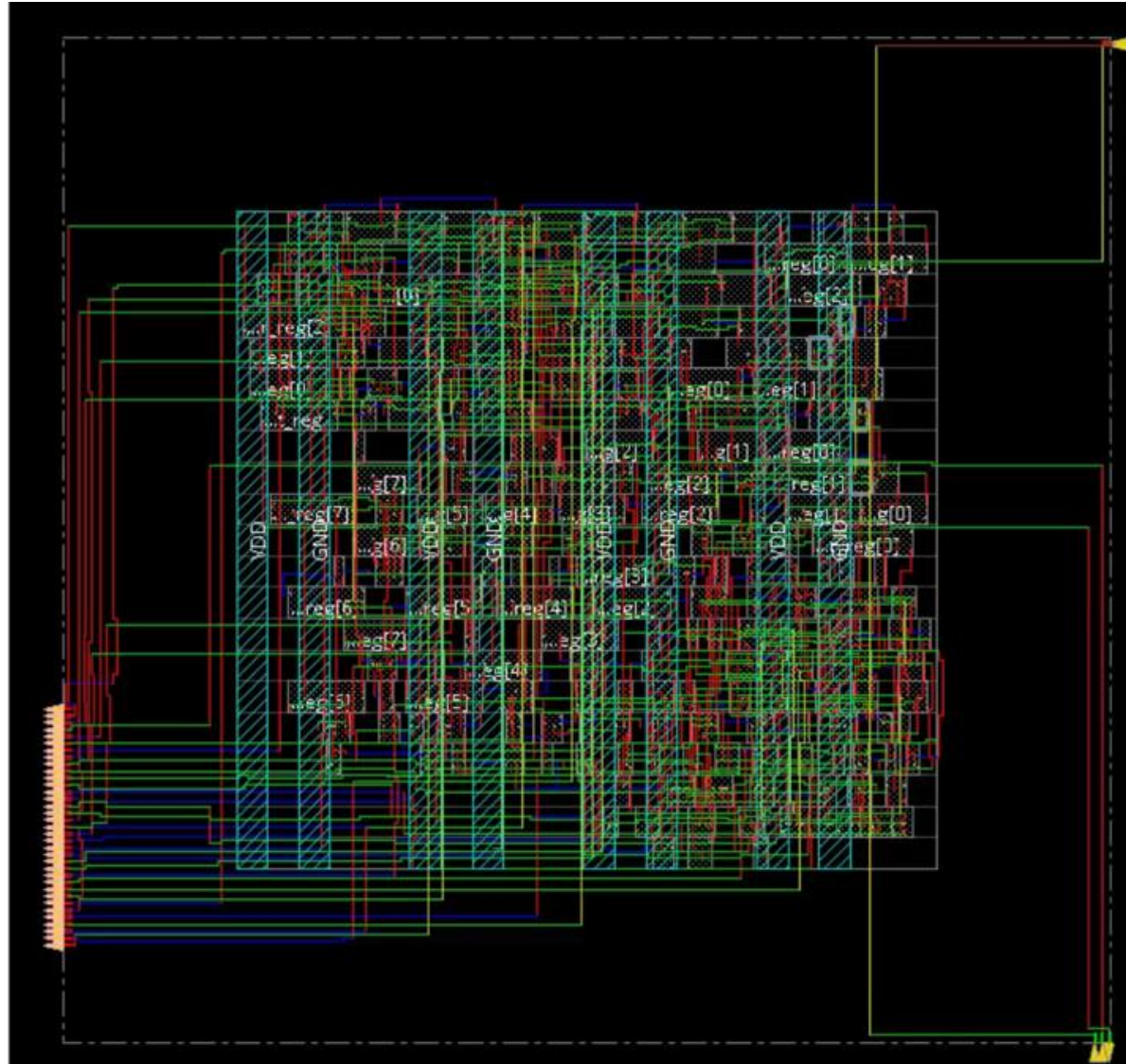
# Digital Block

## Layout

Total size:  
60x60  
um<sup>2</sup>

Core size:  
40x40  
um<sup>2</sup>

- Mode
- Instruction
- Trigger Channel Mask
- Load Count Ser
- Select Reg



- Rstn
- Internal Clock

Ref. [4] Ahan Datta *Design and Implementation for the Digital Block of PSEC5 CPAD 2024*

- SPI clk
- Serial Out
- Serial In

# SPI Register Table

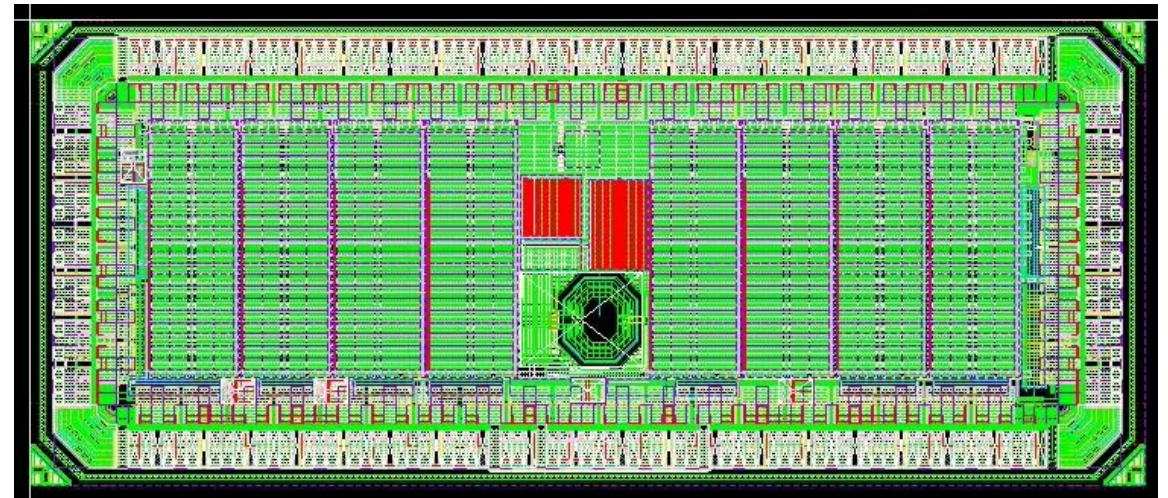
Register Address	Read/Write	Content	Description
0		Reserved	Will read out nothing
1	R/W	Trigger Channel Mask	0: Disabled, 1: Enabled
2	R/W	Instruction (2 bits)	1: Reset, 2: Readout, 3: Start
3	R/W	Mode (2 bits)	00: Use 1 Fast SCA bank to capture an edge, 01: Use 2, 10: Not Used, 11: Use 4.
4-10	R	Counter 0 Values	last 3 bits of reg 10, 17, 24, 31, 38, 45, 52, 59 are not data
11-17	R	Counter 1 Values	
18-24	R	Counter 2 Values	
25-31	R	Counter 3 Values	
32-38	R	Counter 4 Values	
39-45	R	Counter 5 Values	
46-52	R	Counter 6 Values	
53-59	R	Counter 7 Values	
60	R	PLL Locked (1 bit)	Only necessary with onboard PLL
61	R/W	Discriminator Polarity (8 bits)	0: falling Edge. 1: Rising Edge
62	R/W	VCO Digital Band (6 bits)	
63	R/W	PLL Division Ratio(3 bits)	256, <u>128</u> (40MHz), 64, 32, 16
64	R/W	Slow mode (1 bit)	Uses 2.5GHz clock instead of 5GHz clock
65	R/W	Trigger Delay (6 bits)	Discriminator output to trigger is delayed by this amount of clock cycles. (Max 31)

Table 1: SPI Register Map. All registers are 8 bits long.

# Schedule – boards are being fabricated

Schematic / Simulation	Sep. 2023
Layout	Mar. 2024
Post Layout Simulation	Apr. 2024
Layout Optimization	Jul. 2024
Tapeout	Sep. 2024
DUT Board Assembly	May. 2025
Control Board Assembly	May. 2025

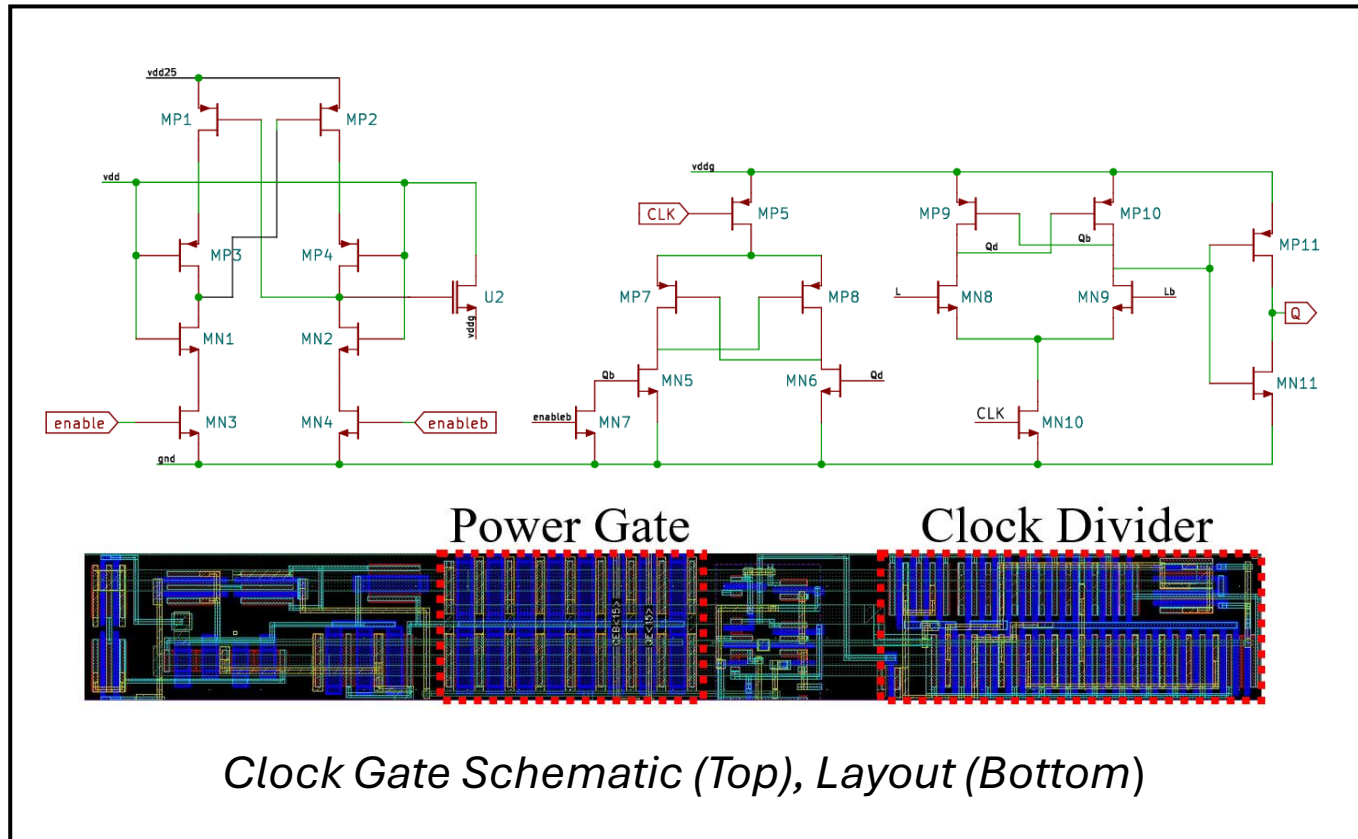
Testbench	June 2025
Implementation at FTBF	TBD 2026



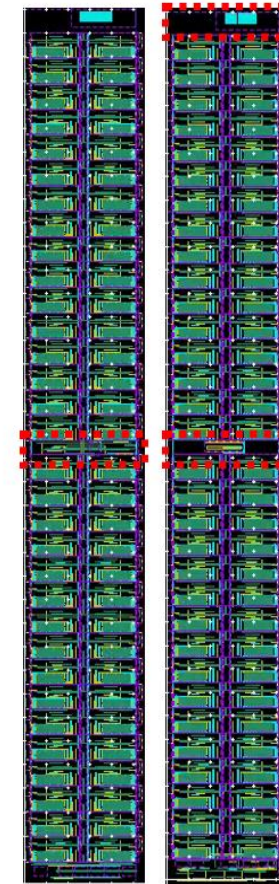
# High bandwidth with low power consumption?

	Worst Case	Best Case
Input Source Follower [mW/Ch]	9.2	4.0
SCA (Sampling) [mW/Ch]	16.6	13.9

Table 1: Power consumption



Clock Divider / Gate



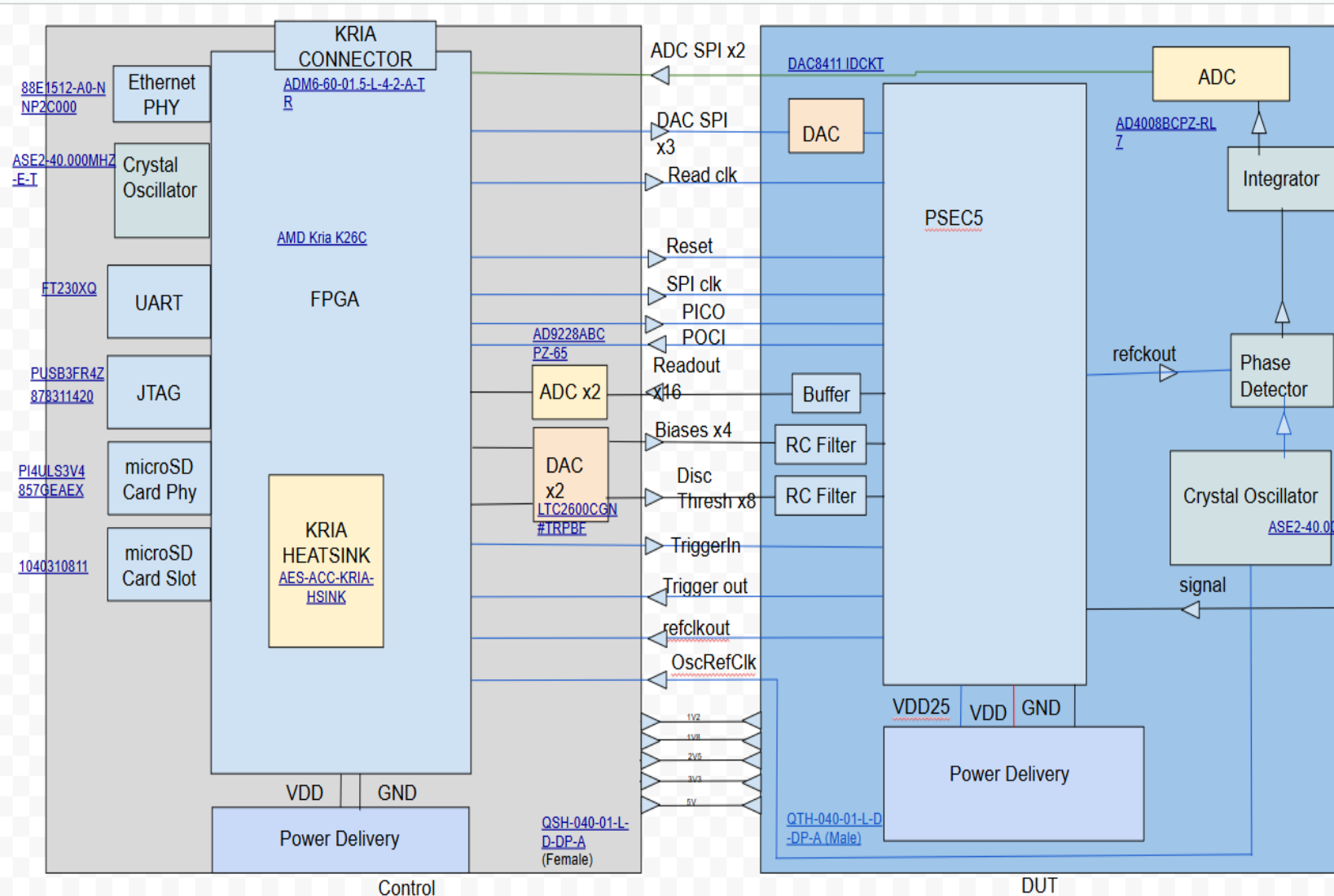
Output Source Follower

(Fast) Input Source Follower

*Left: Slow SCA, Right: Fast SCA*

20 mW/Channel achieved by: Clock Gate, Source Followers and Voltage shifters

# Objectives and Compromises

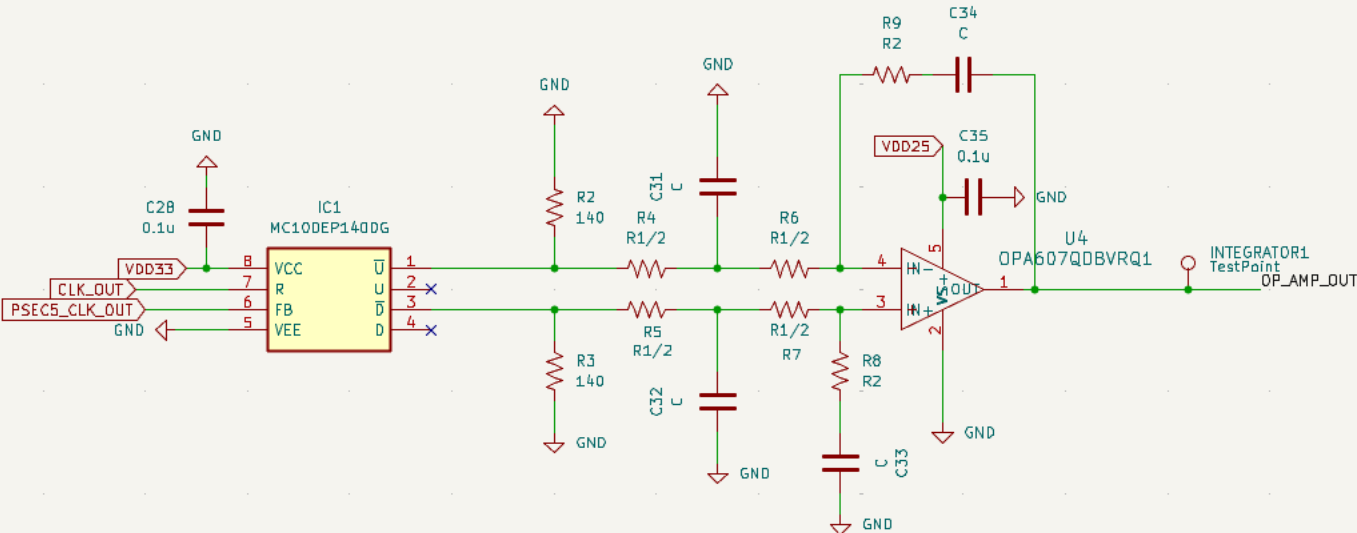


<b>Process</b>	<b>TSMC 65 nm</b>
Dynamic range	10 bits
Sampling Rate	40 GSa/s
Buffer Length	6.4 ns(204.8 ns)
Analog Bandwidth	>4 GHz
Channels/Chip	8
Area	2.4 mm <sup>2</sup>
Multi-Hit Capability	<b>Yes</b>
Customizable Buffer	<b>Yes</b>
On-Chip 10 GHz PLL	<b>No</b>
On-Chip ADC	<b>No</b>

**These components do not exist in 65nm CMOS - A test board is used to fill in the missing features**

See **Andrew Arzac's** talk *A Modular Test System for the PSEC5 40 GS/s waveform-sampling ASIC, Fast 2025*

# Compromise 1: "PLL" on board



$$R_1 = \frac{K_\phi K_V}{N * \omega_n^2 * C}$$

Where:

$$R_2 = \frac{2 * \zeta}{\omega_n * C}$$

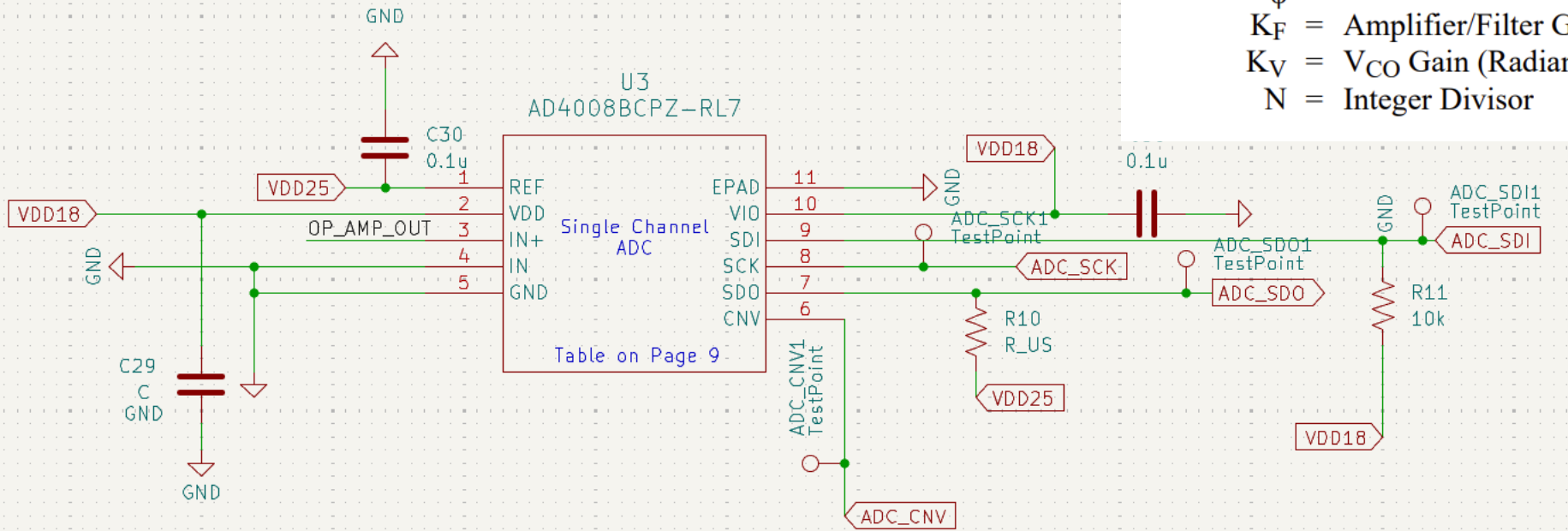
$$C = \frac{K_\phi K_V}{N * \omega_n^2 * R_1}$$

$$K_F = \frac{1 + T_1(s)}{T_2(s)}$$

Where

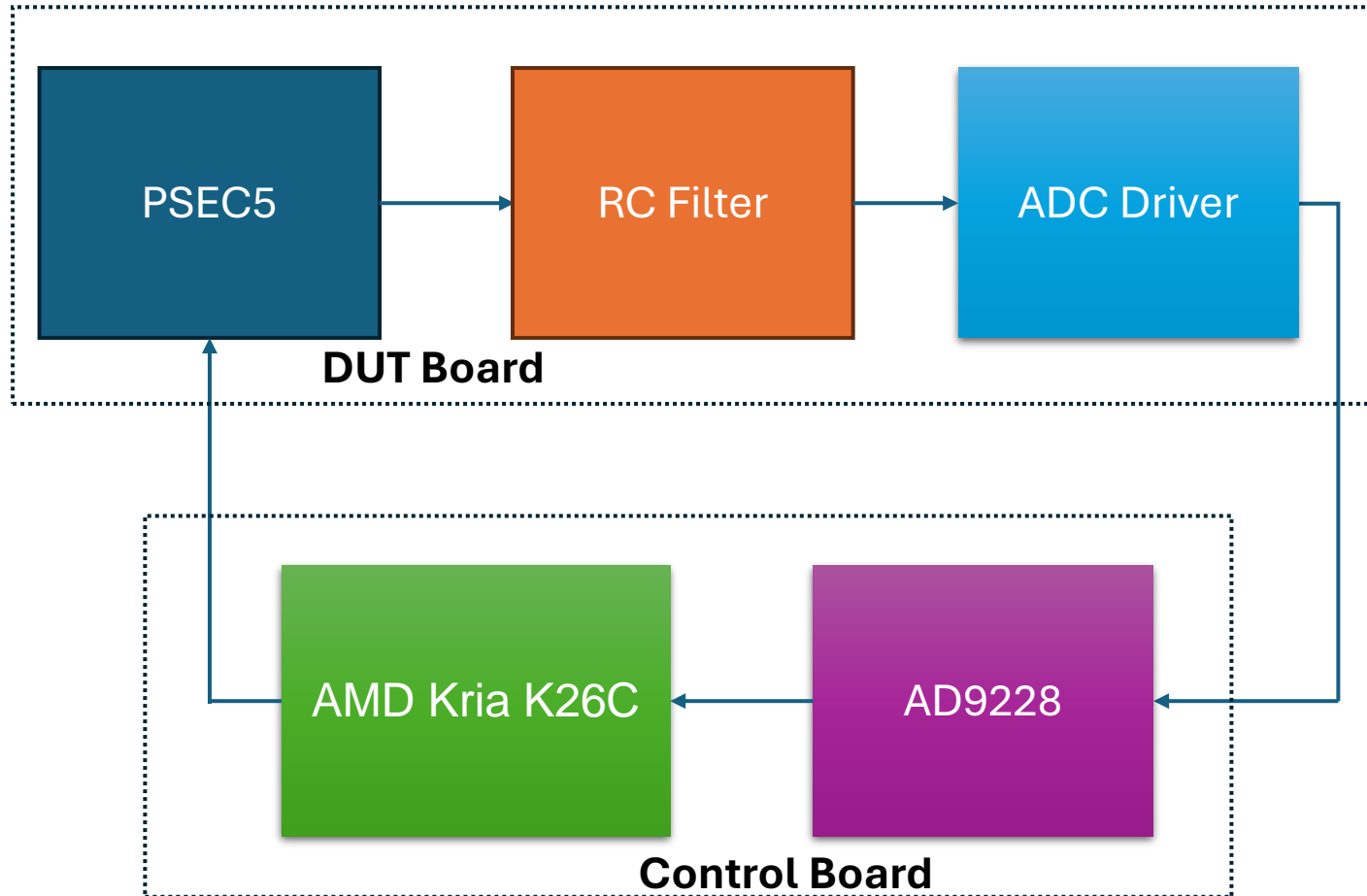
- $K_\phi = 1.2 \text{ mV/Deg}$  – Phase detector gain
- $K_F$  – Amplifier/Filter Gain: Unity
- $K_V = 400 \times 10^6 \text{ Hz/V}$  -  $V_{CO}$  Gain
- $\zeta \sim 1$  – damping ratio
- $\omega_n = 1.6 \text{ MHz}$

- $K_\phi$  = Phase Detector Gain (Volts/Radian)
- $K_F$  = Amplifier/Filter Gain
- $K_V$  =  $V_{CO}$  Gain (Radians/Second/Volt)
- $N$  = Integer Divisor



Chip clk is divided by 128, then compared to a 40MHz crystal oscillator

# Compromise 2: Off-chip ADC - AD9228



Parameter	Datasheet Value
<b>ADC</b>	AD9228
<b>Channels</b>	4 (each)
<b>Resolution</b>	12 bits
<b>Max Sample Rate</b>	65 MS/s
<b>Input Bandwidth</b>	315 MHz full-power (-3 dB)
<b>Analog Input Range</b>	2 V p-p differential (with internal 1 V reference)
<b>SNR / ENOB</b>	SNR $\approx$ 70 dB, ENOB $\approx$ 11.3 bits ( $f_1 = 2.4$ MHz)
<b>Power Consumption</b>	119 mW per channel at 65 MS/s (476 mW total for all 4 channels)
<b>Latency</b>	8 pipeline clock cycles $\rightarrow$ 8 / 65 MHz $\approx$ 123 ns

**Two 4-Channel ADCs are used on the test board**

# Summary

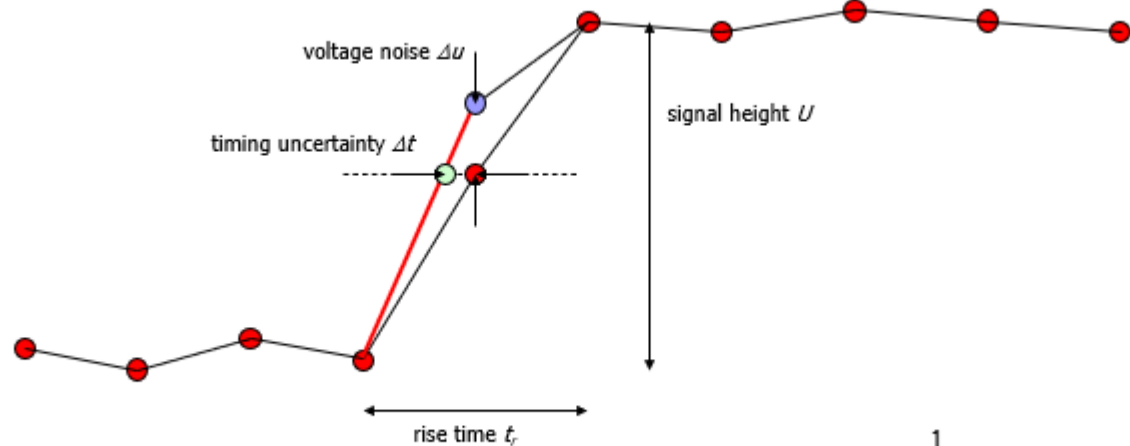
We have designed and taped-out PSEC5 – a **waveform digitizing ASIC** with:

- A goal of **picosecond timing resolution** for precise detector readout
- Dual-mode sampling architecture enabling:
  - 204.8 ns capture window
  - 6.4 ns high-resolution windows for critical timing regions
  - Multi-Hit capability
- Intended for large-scale experiments:
  - **8 channels** per chip
  - 20 mW/Channel power consumption
  - 65nm CMOS TSMC Process

# Supplementary Slides

# How do we achieve picosecond resolution with $\sim 25\text{ps}$ sampling bins

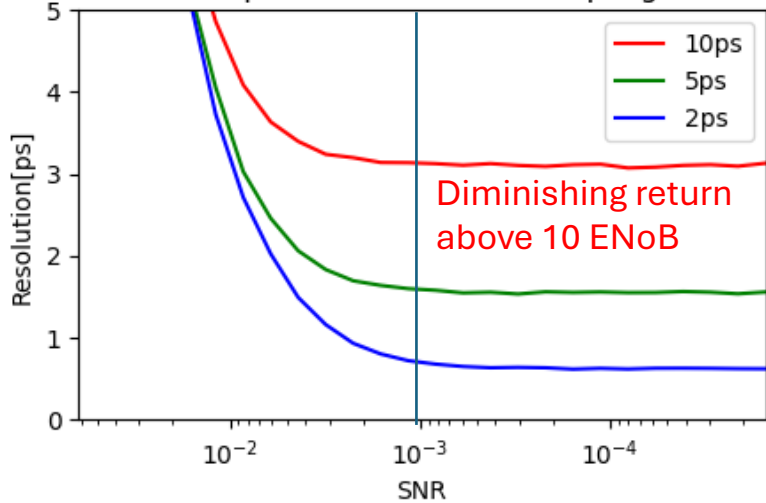
- Multiple samples during the rise time.
- Triggered when the signal reaches the discriminator's output – fast bank takes 64 samples.
- Signal can be interpolated



$$t_r \approx \frac{1}{3f_{3dB}}$$

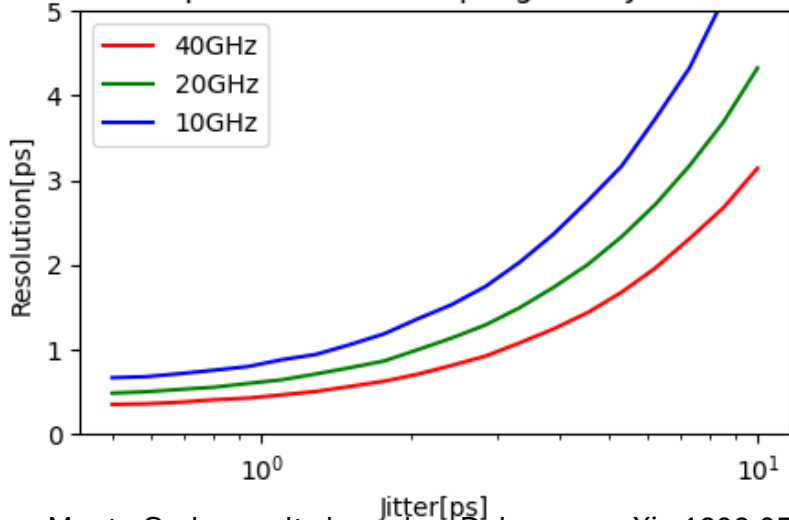
# Sampling Time Uncertainty

Resolution Dependence on SNR, sampling at 40GHz



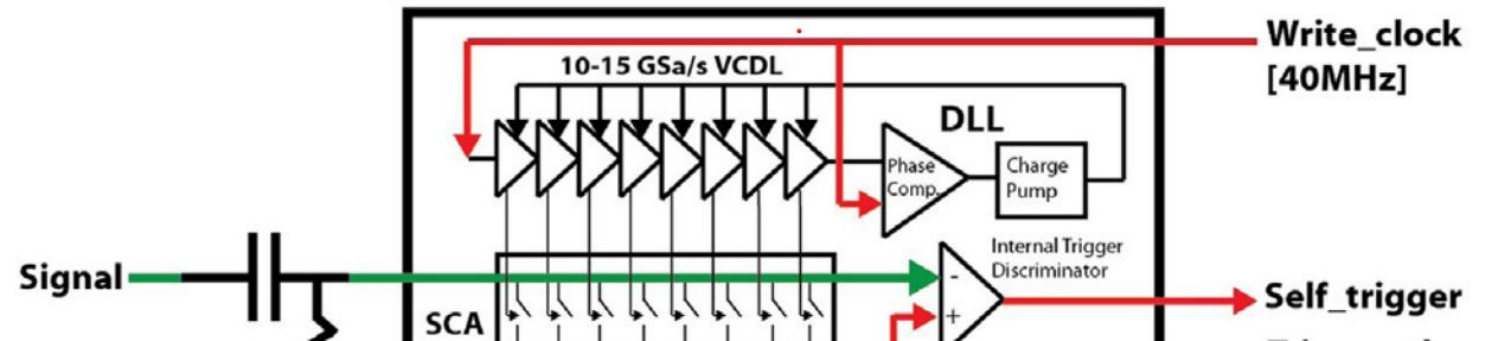
- At  $<1$  ps timing resolution region, it is a **dominant component** of the overall uncertainty.
- Previous Chip PSEC4 employed Delay Locked Loop (DLL) to control sampling switches.
- Process Variation is a major source of systematic timing uncertainty.

Resolution Dependence on Sampling Time Jitter, SNR = 1e-3

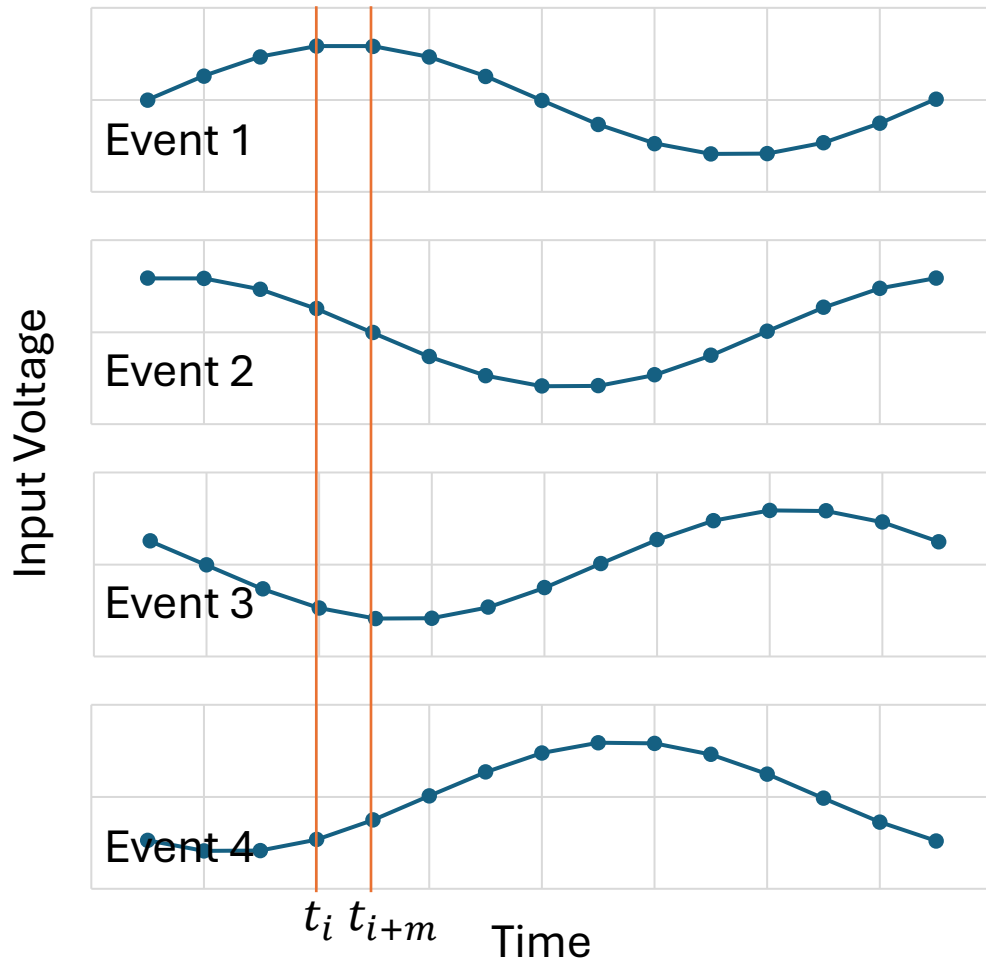


Monte Carlo results based on Delagnes, arXiv:1606.05541

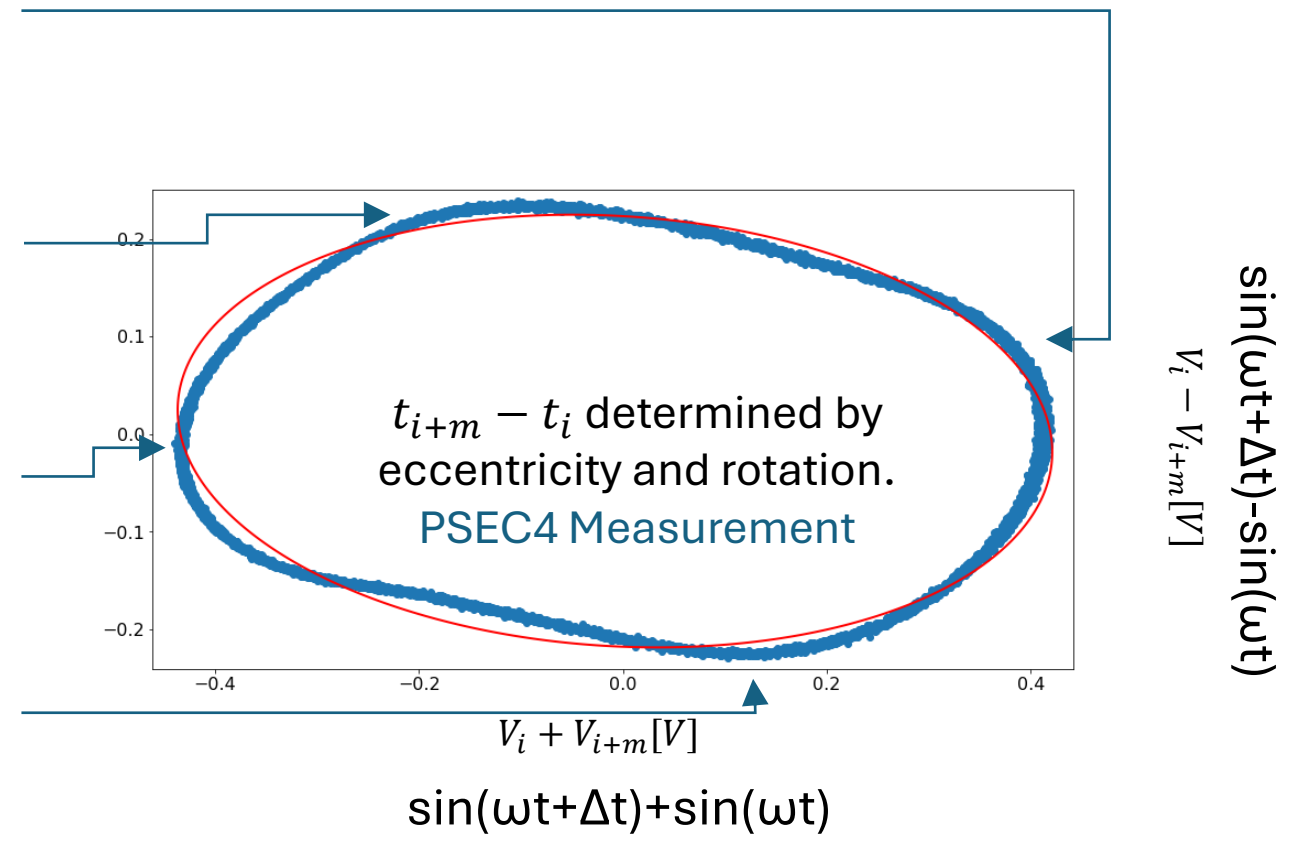
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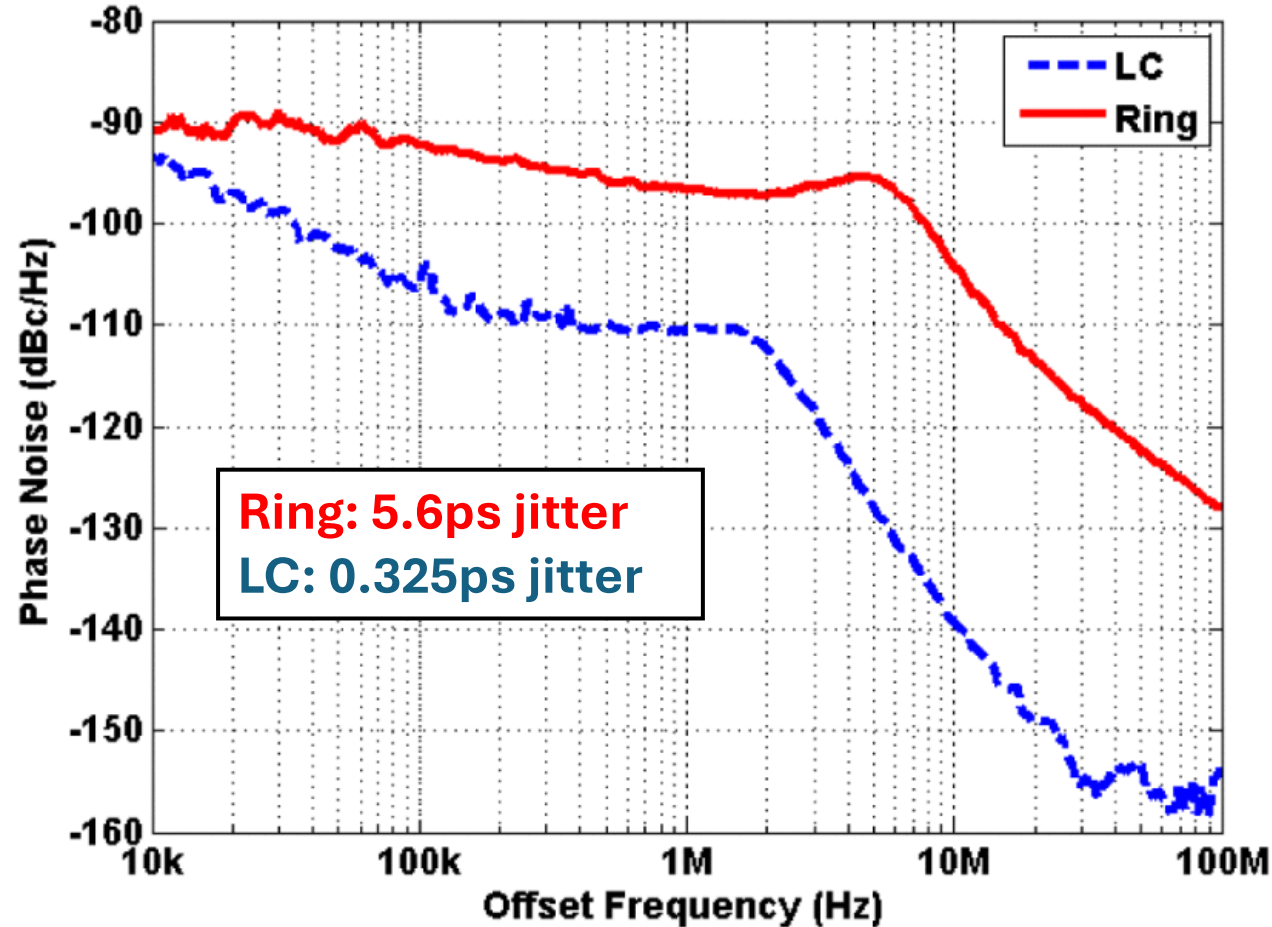
1. Measure many events of a sine wave.
2. Sum vs. Difference of two adjacent samples, over all events, form an ellipse.
3. Time offset can be determined from the coefficients.



Low SNR  $\rightarrow$  fainter, more spread curve.  
 Nonlinearity  $\rightarrow$  distorted curve



# Timing uncertainty reduced by an optimized LC-oscillator based PLL



From abstract:

“Both independent PLLs have identical loop dynamics to allow a fair comparison ...

Furthermore these circuits consume the same amount of power. The PLLs were processed in a commercial 65 nm CMOS technology.”

J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert and P. Leroux, "Comparison of a 65 nm CMOS Ring- and LC-Oscillator Based PLL in Terms of TID and SEU Sensitivity," in *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 245-252, Jan. 2017.

# Post-Implementation Timing Verification

## timeDesign Summary

Setup views included:  
default

Time remaining before  
next clock cycle. Positive  
is good

\*WNS: Worst Negative Slack  
\*TNS: Total Negative Slack

Setup mode	all	reg2reg	reg2cgate	default
WNS (ns):	0.000	24.587	N/A	0.000
TNS (ns):	0.000	0.000	N/A	0.000
Violating Paths:	0	0	N/A	0
All Paths:	48	31	N/A	32

Given the previous constraints, we can verify if our design satisfies them in simulation.