

# A Modular Test System for the PSEC5 40 GS/s waveform- sampling ASIC

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# PSEC5

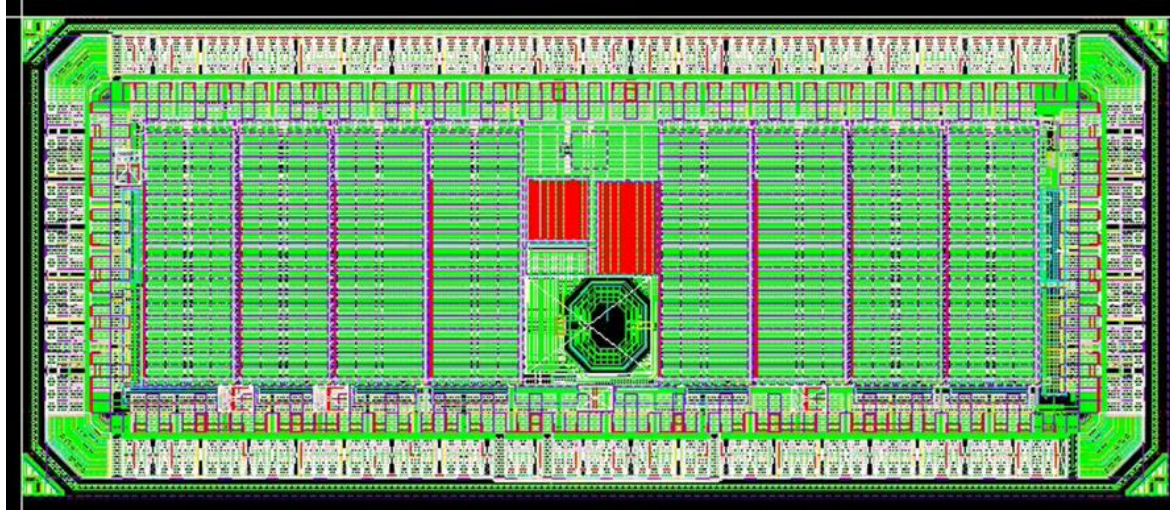
- 8 Channel Waveform Digitizing ASIC
- Multi-hit Capability
- 4 Fast, 1 Slow buffer
- Fast sampling rate and long buffer
- Low power
- Chips arrived

Process	TSMC 65 nm
Dynamic Range	10 bit
Fast Buffer Sampling Rate	40 GSa/s
Slow Buffer Sampling Rate	5 GSa/s
Buffer Length	Fast: 4x1.6ns Slow: 204.8ns
Analog Bandwidth	>4 GHz
Channels/Chip	8
Area	2.4 mm <sup>2</sup>
Power	~ 20 mW / Channel

Goal: < 5 ps time resolution

# Compromises

- The 40 GSa/s sampling makes PSEC5 a very aggressive analog-digital design



*PSEC5  
All Metal  
Layers*

-The chip has an external PLL and ADC, why?

1) A 10GHz PLL design doesn't exist in 65nm CMOS

2) The ADC was judged to be too much work for its added value

PSEC5 is a “pathfinder” chip to prove the multi hit 40 Gsa/s architecture

**See Richmond Yeung's talk Later Today for more detail on PSEC5**

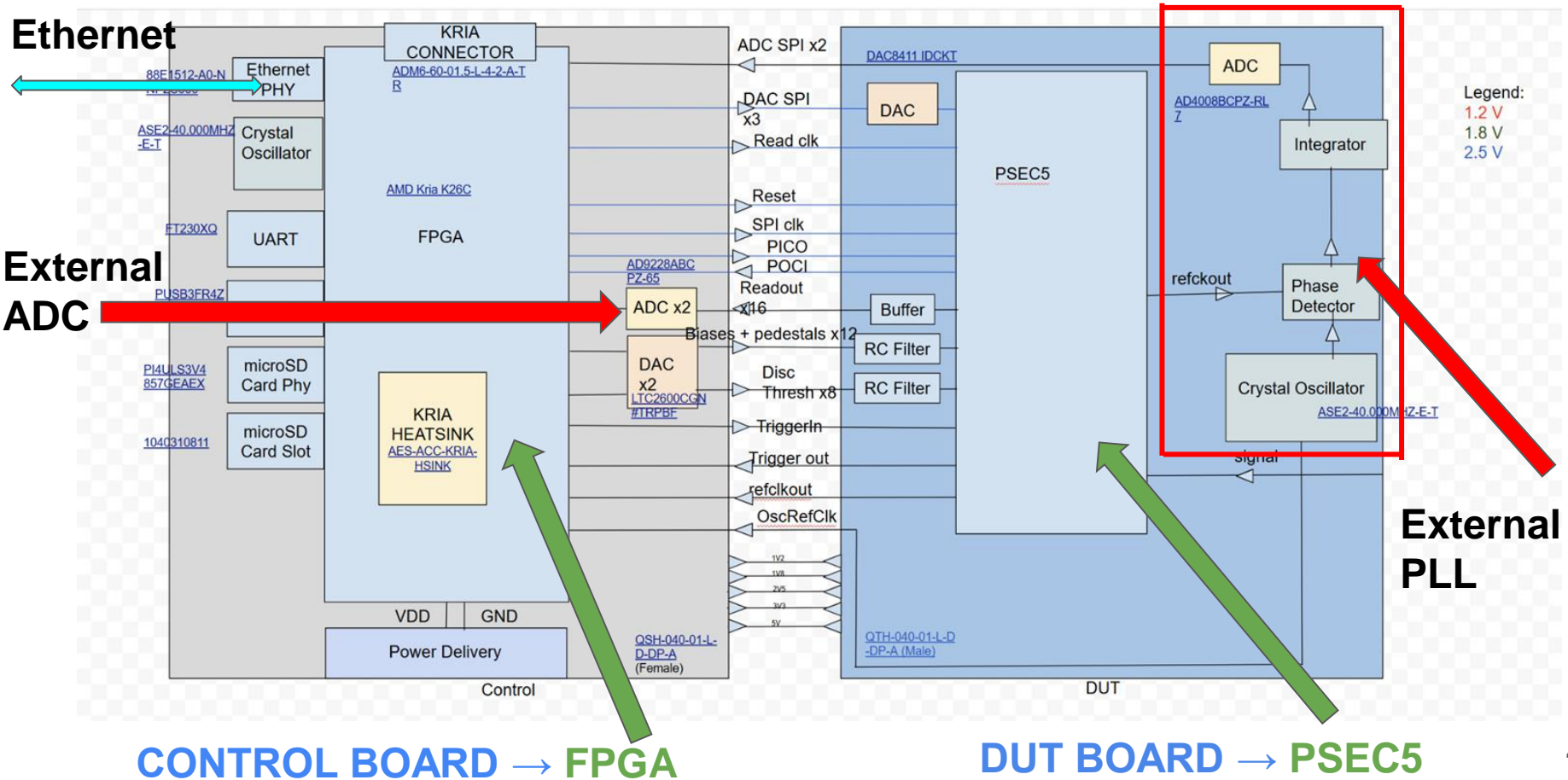
**Design of an 8-Channel 40 GS/s 20 mW/Ch Waveform Sampling ASIC in 65 nm CMOS**

*Mr Richmond Yeung*

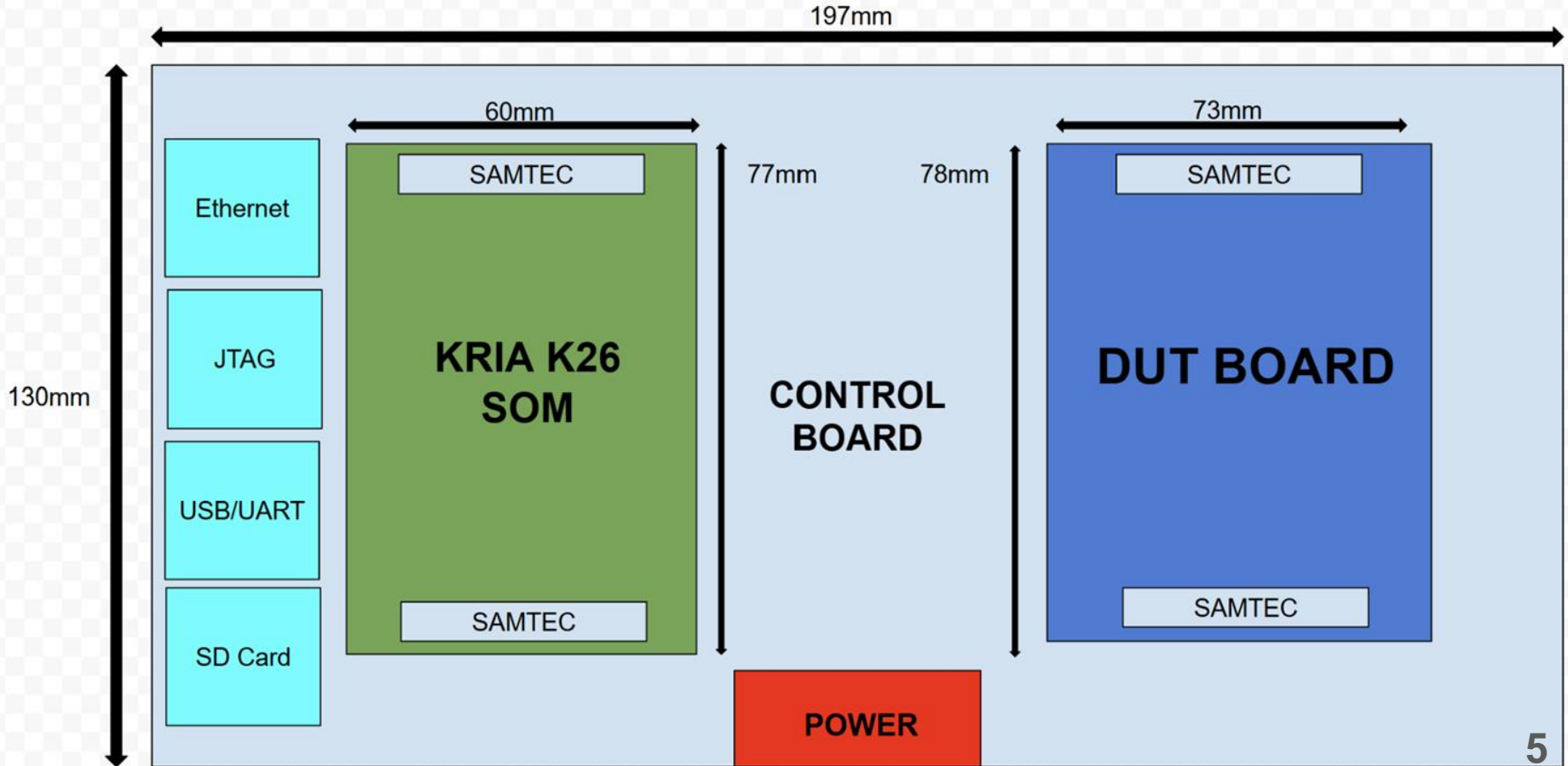
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*Slide idea inspired by Thomas Conneely: Reviewing the Performance of Photek's Single Photon Timing Detectors. FAST 2025*

# Modular FPGA-Based Test System



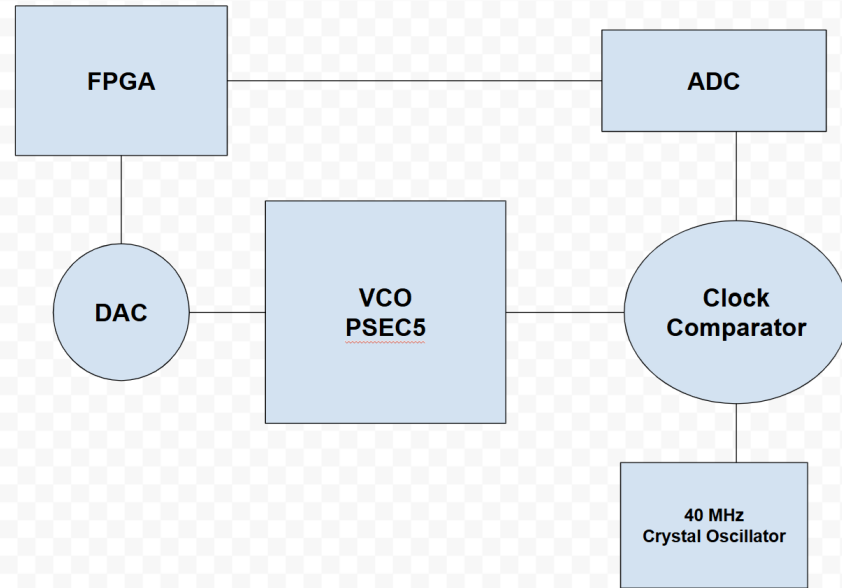
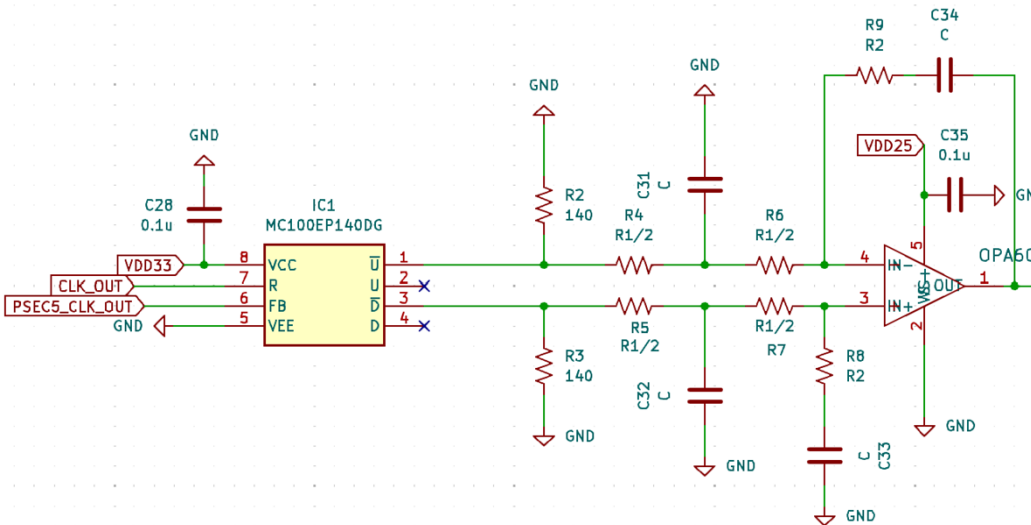
# Physical Layout of the 2 Boards



# Compromise 1: External PLL (DUT Board)

- 10 GHz divided ( $\div 128$ ) to 40 MHz inside the chip
- 40 MHz crystal oscillator as reference clock

Clock Comparator  $\rightarrow$  OP Amp Integrator

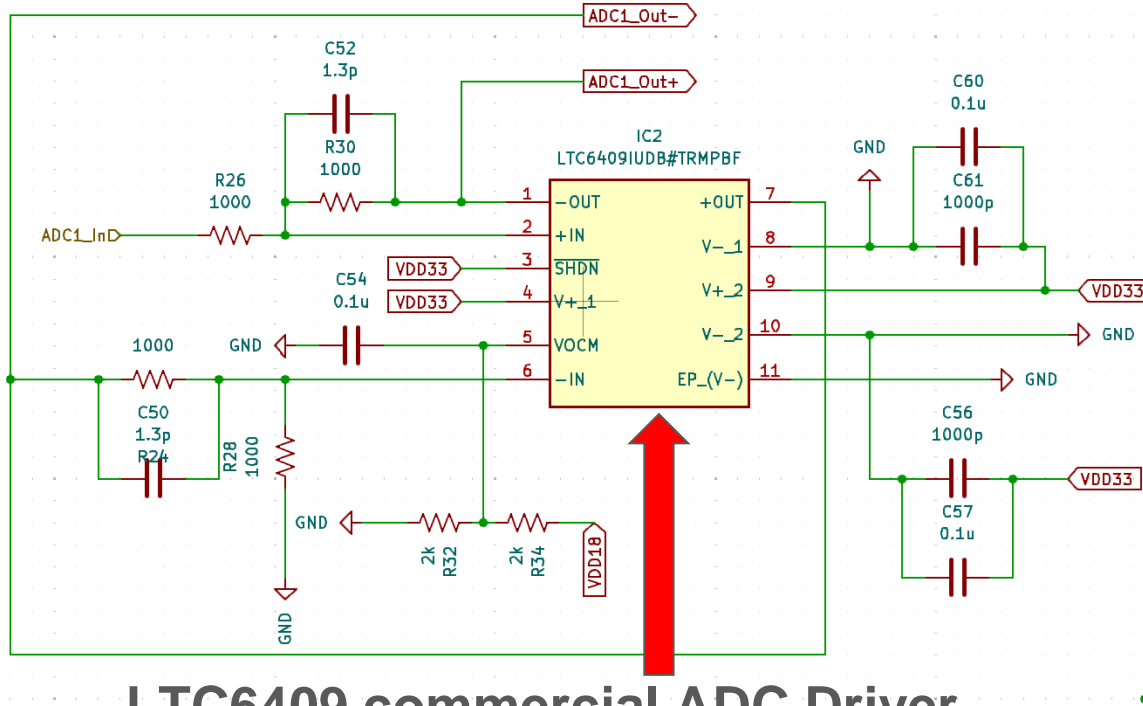


Phase-Locked Loop

# High bandwidth ADC buffer (DUT Board)

- The vendor-recommended buffer had too low bandwidth (500 KSPS)
- Lead to exhaustive search for effective ADC driver,
- Found 10 GHz Gain-Bandwidth, Fully Differential I/O, 3.3V Input Voltage

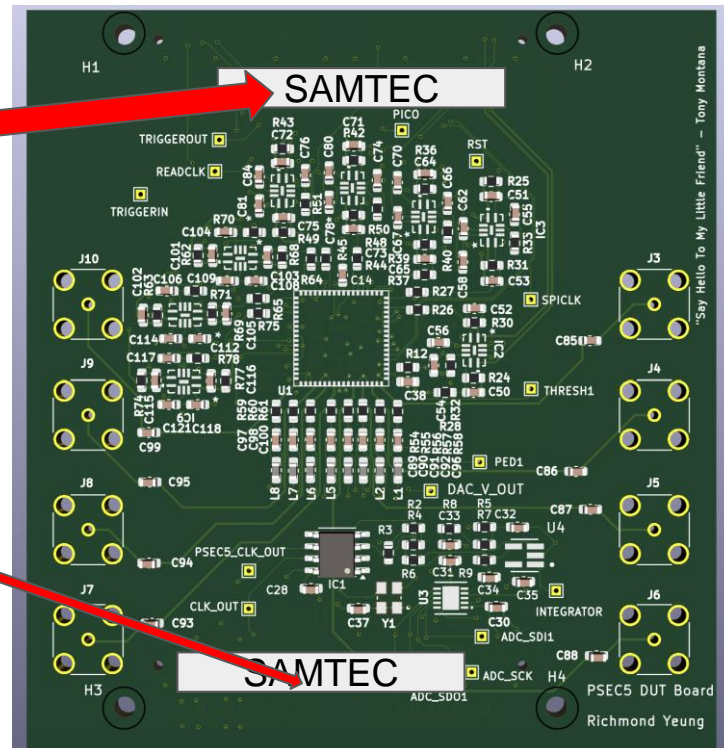
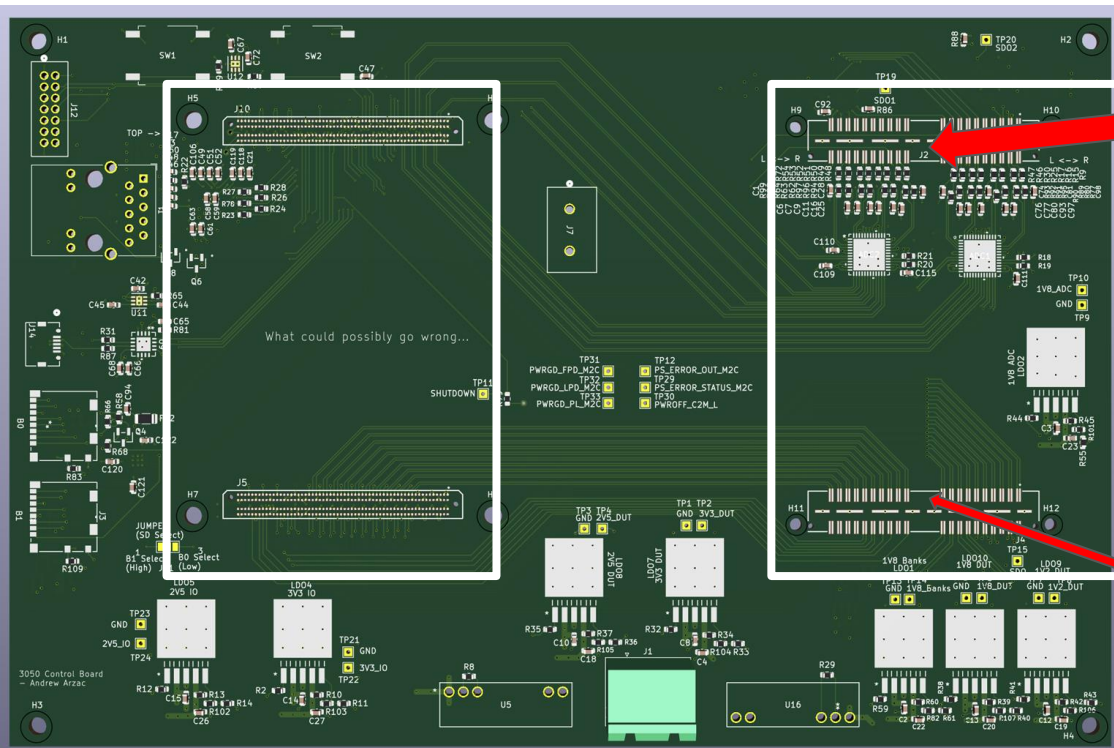
*Schematic of  
ADC Driver*



**LTC6409 commercial ADC Driver**



# 3D Renderings and Connections

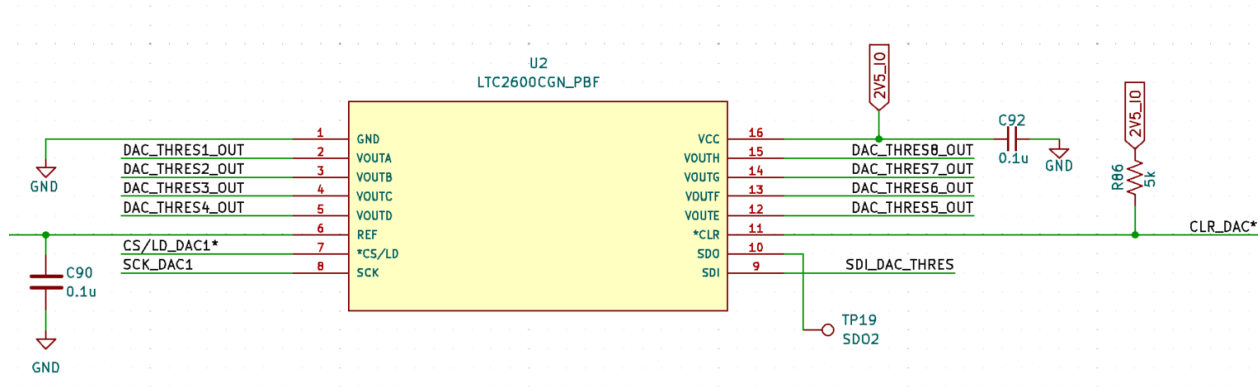


- Control Board
- 10 Layers, 1.2 mm
- Power Connectors, IO plugs, 5V Fan

- DUT Board
- 6 Layers, 1.2mm
- 8 SMA connectors

# Input/Output, Communicating with PSEC5: FPGA

- There are 4 IO forms connected to the Kria FPGA
  - Ethernet → Primary Data Communication
  - SD Card → Secondary boot for firmware and operating system
  - JTAG → Debugging
  - USB → Extra just in case
- SPI protocol is used from the FPGA → DAC → PSEC5



Communication to PSEC5 via DAC's and

# Test Setup Power Consumption

- In order to test the chip, minimizing power consumption wasn't the priority

Location	Device	Typ, Max power consumption
Control Board	FPGA (Kria K26)	7.5 W (typ), 15 W
Control Board	External ADC	119 mW x 8
DUT Board	PSEC5	~ 20mW x 8
Total		~ 9-10 Watts

## *Main Power Drawing Devices*

- Power is distributed from 2 buck regulators (5V and 2.5V) into LDO's at desired voltages

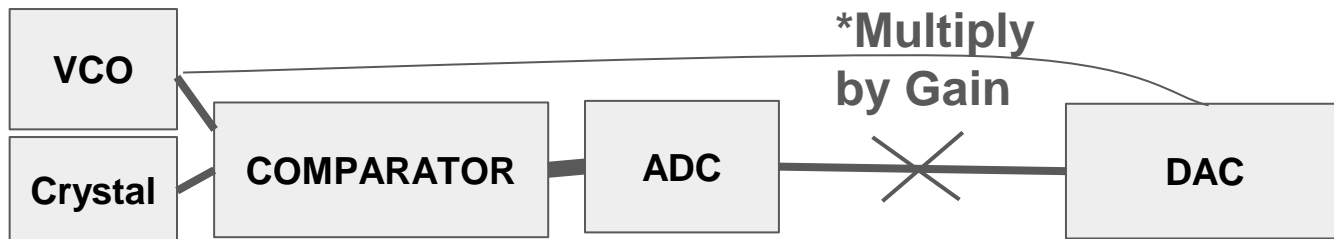


- DUT Board (PSEC5) has its own power rails

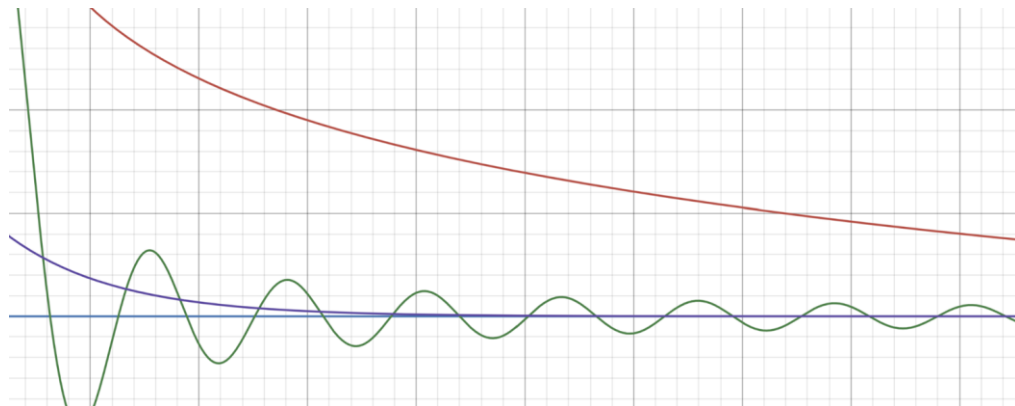
# Firmware: Overview of PLL and Main ADC Signal Path

Firmware Designed by Ahan Datta<sup>a</sup>

- Typical PLL implemented, just externally



\* Gain Determined by FPGA through successive runs



Low Gain: Red (Slow convergence)

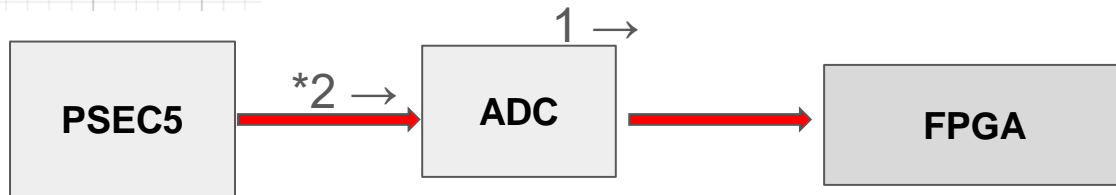
High Gain: Green (Oscillating)

Correct Gain: Purple (Fast Convergence)

*The lines on this graph have no physical value, rather general functions to model slow convergence, fast convergence and oscillatory behaviors*

## Main ADC Signal Path

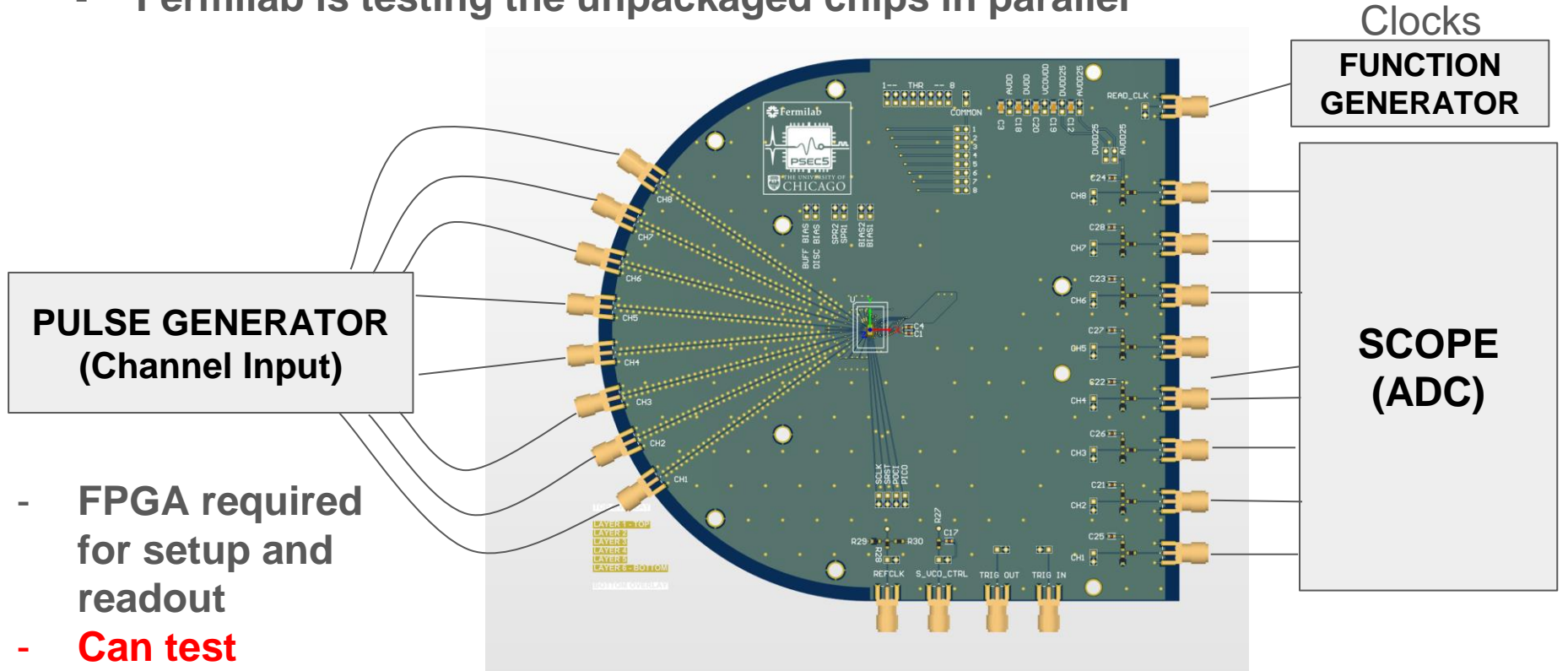
- Serial calling of capacitor values



1 Passing through ADC → \*2 is Called 12

# Testing of unpackaged Chips

- Fermilab is testing the unpackaged chips in parallel

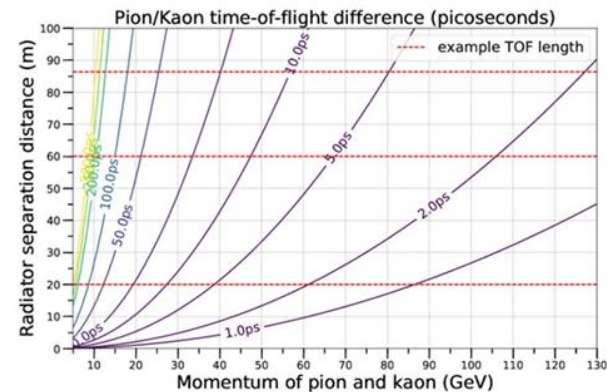
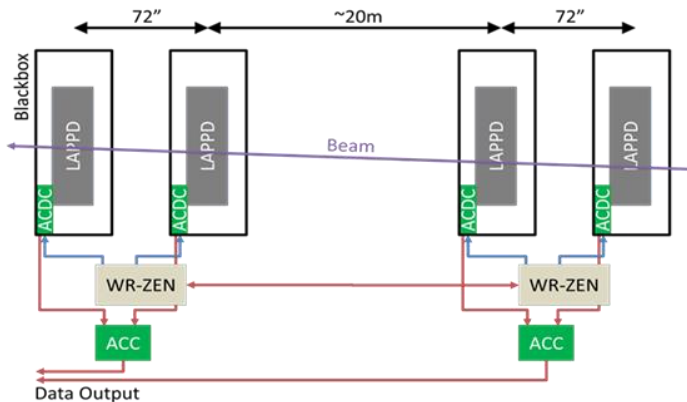
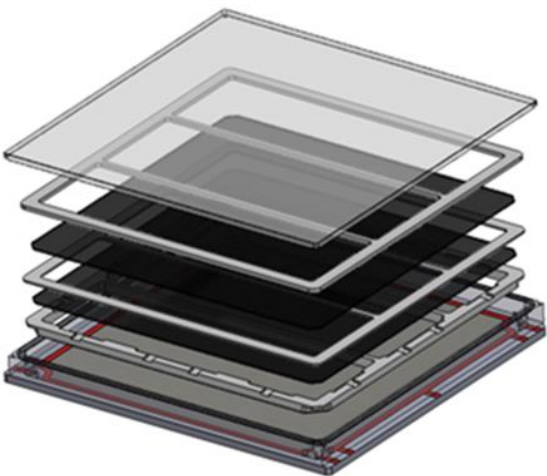


- FPGA required for setup and readout
- **Can test everything except PLL**

3d rendering of COB (Chip on Board)



# Future testing PSEC5 at the Fermilab Testbeam



*Expanded view of LAPPD and its Components*

## Fermilab Test Beam Upgrade

Timing Resolution ~ 5ps

LAPPD - timing Constrained by Electronics

*Modified From Design of an 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS - Richmond Yeung CPAD 2024*

# Conclusion + Current Status

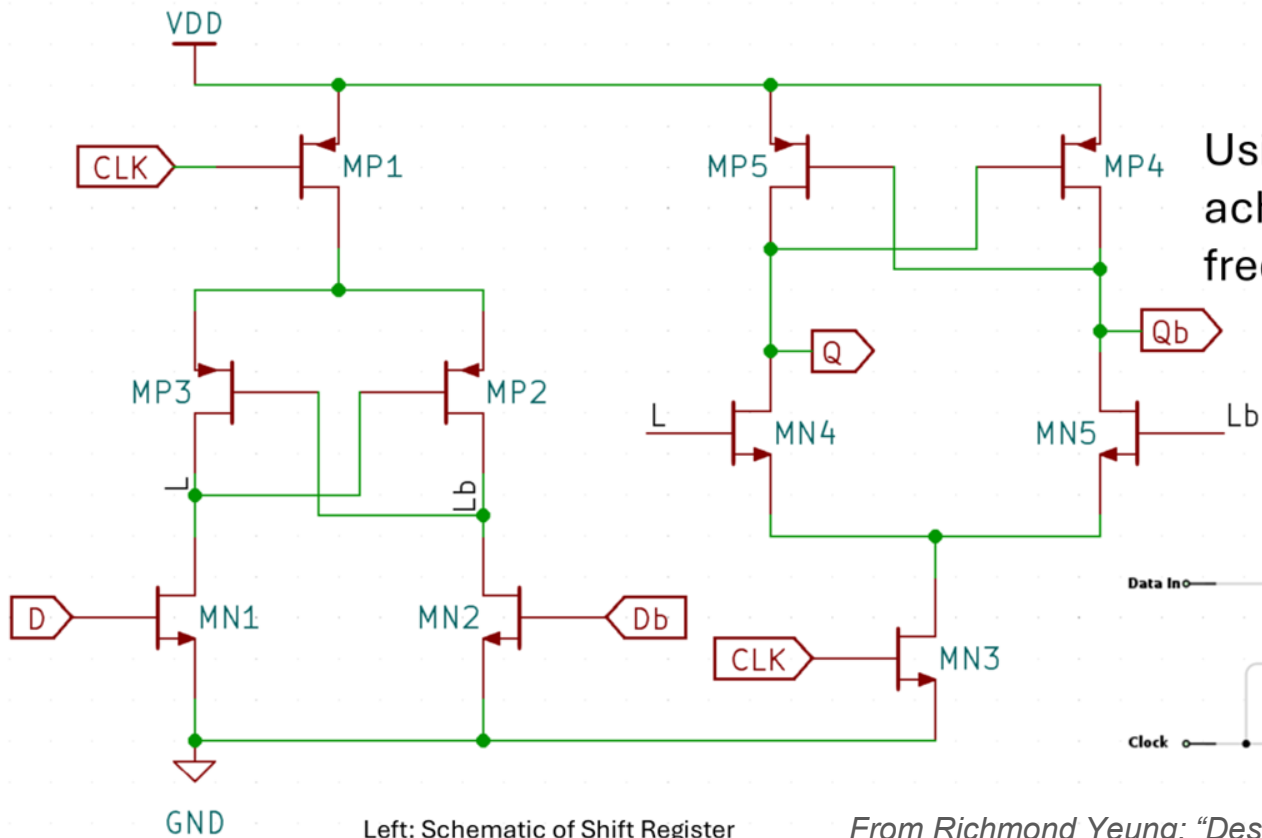
- Full testsetup to test PSEC5 with a control board, DUT board, and an FPGA
- COB board to test bare dies
- PSEC5 full setup to be tested this summer

<b>Board</b>	<b>Status</b>
<b>DUT Board</b>	<b>Arrived and populated</b>
<b>Control Board</b>	<b>ordered</b>
<b>COB</b>	<b>ordered</b>

**Thank you for listening**

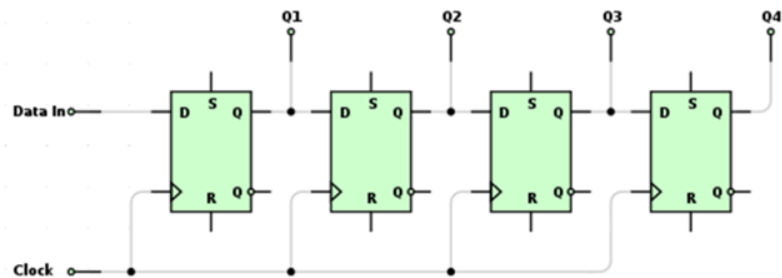
# Extra Slides

# Reducing Clock Power: 40GS/s without 10GHz clk



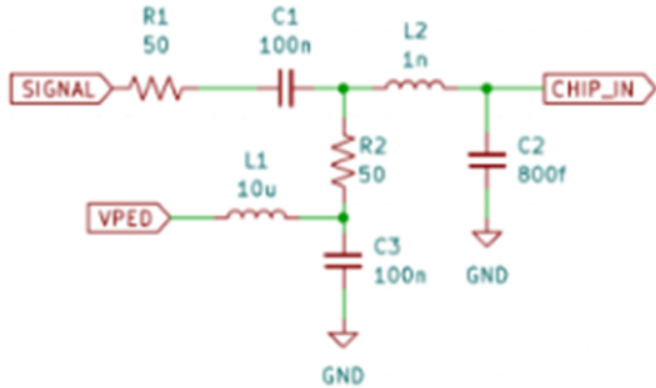
Left: Schematic of Shift Register

Using both clock edges, we can achieve 10 GSps with half the frequency



From Richmond Yeung: "Design of an 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS" CPAD 2024

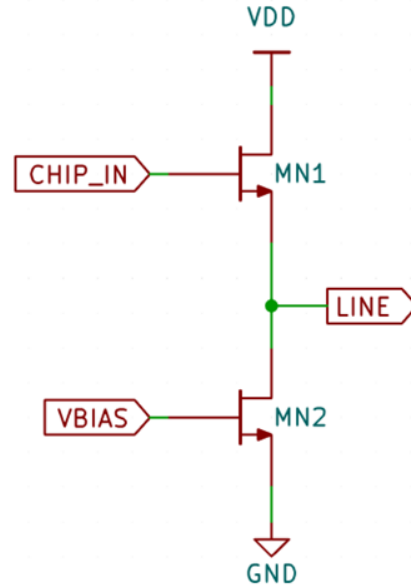
# Signal Path: Bandwidth



- C1, C3, R2, L1 are components placed on board for capacitive coupling. L2 and C2 are the parasitic inductance and the capacitance of the wire bond and ESD combined
- Pedestal Voltages are controlled by the FPGA

Key Specs:

- Source Follower Bandwidth 5 GHz
- Wire-bond Bandwidth 4 GHz
- Slow Bank Bandwidth 2 GHz

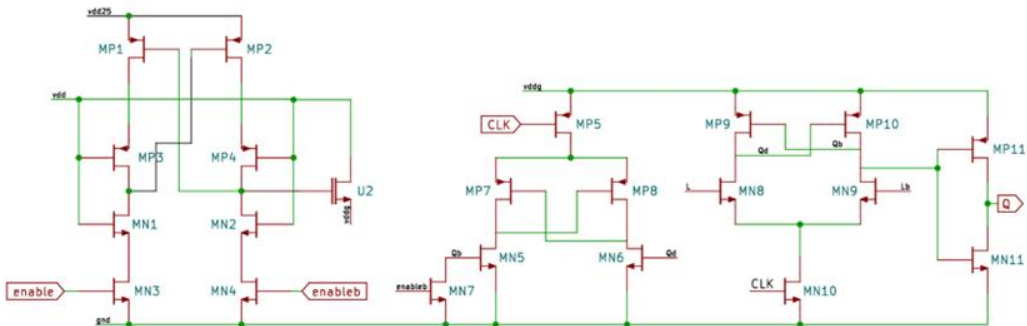


From Richmond Yeung: "Design of an 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS" CPAD 2024

# High bandwidth but Low Power consumption?

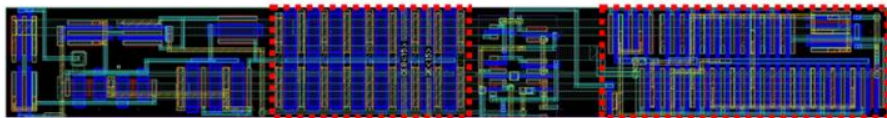
	Worst Case	Best Case
Input Source Follower [mW/Ch]	9.2	4.0
SCA (Sampling) [mW/Ch]	16.6	13.9

Table 1: Power consumption



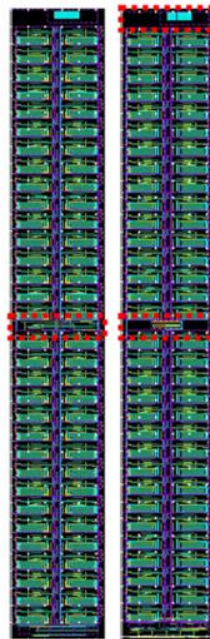
Power Gate

Clock Divider



Clock Gate Schematic (Top), Layout (Bottom)

Clock Divider / Gate



Output Source Follower

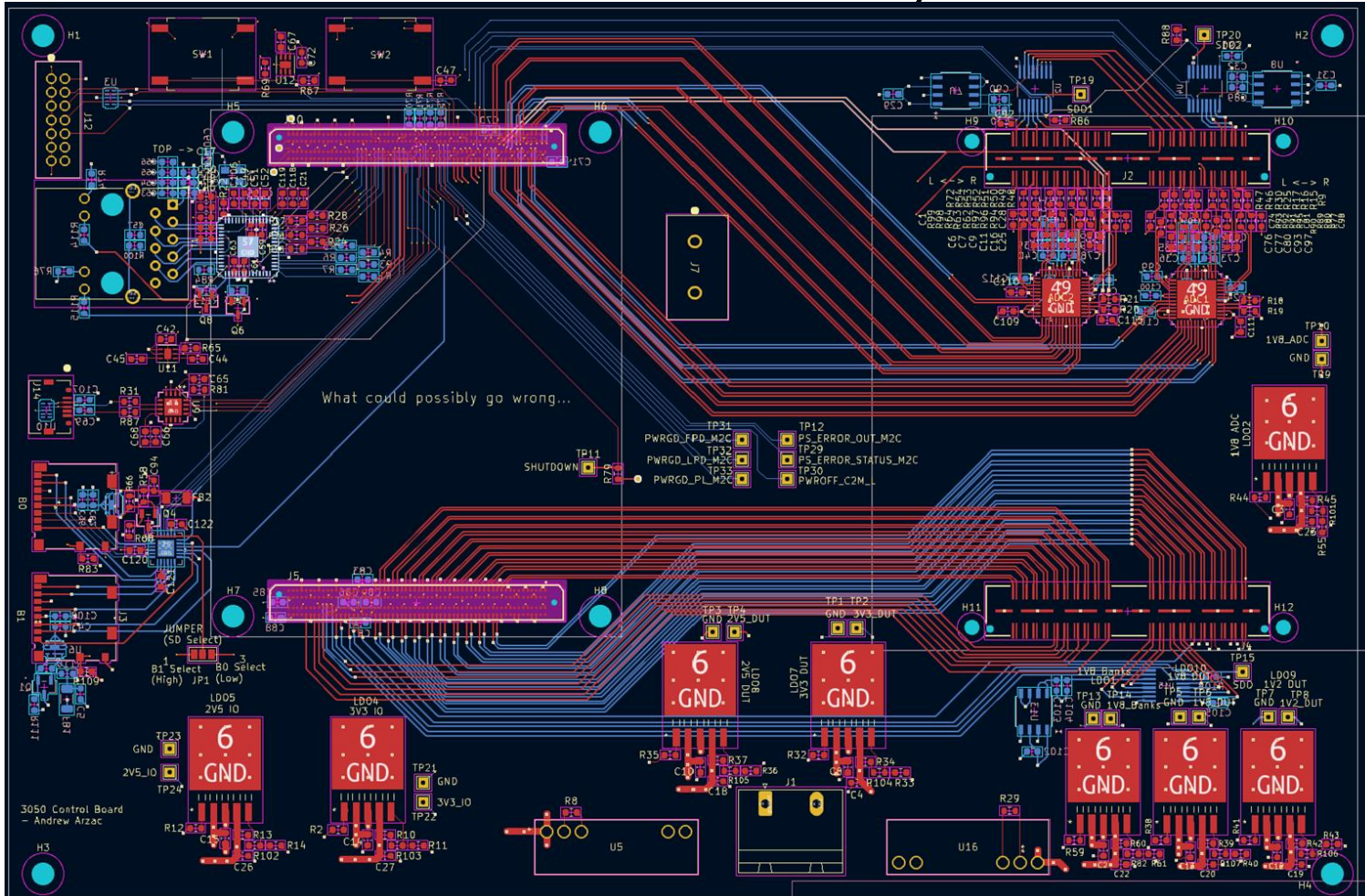
(Fast) Input Source Follower

Left: Slow SCA, Right: Fast SCA

From Richmond Yeung: "Design of an 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS" CPAD 2024

20 mW/Channel achieved by: Clock Gate, Source Followers and Voltage shifters

# Control Board Layout





# ADC Firmware Wave Diagram

