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A Modular Test System for the PSEC5 40 GS/s waveform-sampling ASIC

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We have recently submitted for fabrication PSEC5, an 8-channel mixed-signal waveform-sampling ASIC targeting 1 ps timing resolution, 200 ns buffer length, and multi-hit capability. Here, we describe the architecture and development process of a modular test system for PSEC5. The system consists of two PCBs: a Design Under Test (DUT) Board, and a Control Board. The Control Board is based on the Kria K26 FPGA module. The DUT Board contains PSEC5. The boards are being designed in KiCad; the
FPGA firmware is being written in Vivado. The system has been designed by a team of undergraduates with guidance from experts

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